A Low-Power Recursive I/Q Signal Generator and Current Driver for Bioimpedance Applications

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***Abstract*—This Brief presents a power-efficient quadrature signal generator and current driver application-specific integrated circuit (ASIC) for bioimpedance measurements in an electrical impedance tomography system for monitoring lung function. The signal generator is realized by a digital recursive signal oscillator with the ability of generating quadrature signals over a wide frequency range. The generated in-phase signal is applied to a current driver. It uses a balanced current-mode feedback architecture that monitors the output current through a feedback loop to minimize common-mode voltage build-up at the injection site. The quadrature signals can be used for I/Q demodulation of the measured bioimpedance. The ASIC was designed in TSMC 65 nm technology occupying an area of 0.21 mm^2. The current driver can generate up to 0.7 mA$_{p\text{-}p}$ current up to 200 kHz and consumes 2.7 mW power under ±0.8 V supplies.**

***Index Terms*—ASIC, bioimpedance, current driver, FIR filter, low power, quadrature recursive signal oscillator.**

I. Introduction

Bioimpedance measurements provide low-cost, radiation-free, real-time and wearable means for physiological status monitoring in a range of applications including electrical impedance tomography (EIT) and electrical impedance spectroscopy. Bioimpedance measurements in EIT entail injecting a small ac current across a pair of electrodes from a set of electrodes placed around the circumference of the test subject (the electrodes could be placed on a belt). By measuring the voltage developed between other pairs of electrodes, the bioimpedance of the tissue can be calculated and used to generate a tomographic image [1], [2].

The frequency of the injected current can vary depending on the application. High range frequencies (up to 10 MHz) are usually used where the liquid content of the tissue is more important. Injecting currents with frequencies, as low as a few Hz, results in an impedance representing the shape and volume of the target tissue [3], [4]. Thus, different design approaches are considered for each application according to the specific requirements. In EIT lung function monitoring, an impedance contrast can be detected during the respiration cycle due to the higher resistivity of the air content of aerated lungs [5]. This variation can be monitored by measuring the voltage resulting from the injection of a current over a relatively low frequency range, typically 50–200 kHz (the system presented in this Brief was designed to conform to this frequency range).

Wearable EIT systems can be realized using battery, inductively coupled link or RF-antenna-based wireless transfer. The power consumption of the front-end (current injecting and voltage recording) circuits implemented on an EIT belt must be minimized to prolong the battery lifetime or feature a small size for the coil or antenna. The motivation for this work is to implement low-power solutions for EIT systems. In particular, to design a low-power quadrature signal generator and current driver that are key components in an EIT system for performing bioimpedance measurements (i.e. injecting a known current and demodulating the measured voltage as shown in Fig. 1).

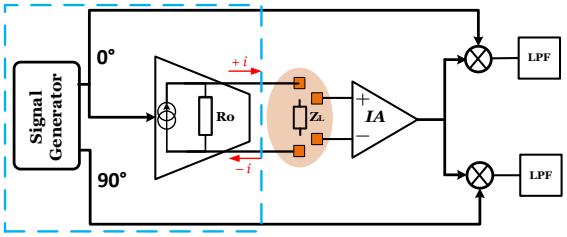

Fig. 1. Current injection and bioimpedance measurement with I/Q demodulation using tetrapolar electrode configuration (the parts designed and implemented in this work are inside the dashed box).

Bioimpedance is a complex value; its amplitude and phase can be extracted by multiplying the recorded voltage by signals in-phase (I) and quadrature-phase (Q) with respect to the injected signal [4]. A conventional topology for current driver designs is the Howland current pump introduced in 1962 [6]. It consists of a single operational amplifier and a resistive bridge. The transconductance of the driver depends on the resistance in the bridge and the output impedance of the driver itself. This requires tight matching of resistors usually implemented with discrete components that add a parasitic capacitance to the output, potentially limiting the bandwidth of the driver.

A current conveyor-based current driver was proposed in [7] with an output current in the frequency range of 100 Hz to 10 MHz. The design is based on buffering the applied sinusoidal voltage across a resistor and converting it to current. This current is mirrored to the load using a current-controlled current source implemented with a cascode output stage with gain boosting amplifiers. To ensure no extra dc voltage is applied to the tissue, a dc blocking capacitor is used together with a dc servo loop that monitors the output voltage. Using a cascode structure for the driver requires a relatively high supply and consequently larger power consumption. The design in [7] uses 3.3 V supply voltage and generates 1.2 mA current.

A nonlinear feedback current driver was presented in [8] which minimizes the phase delay of the current driver to less than 3° at high frequency. It comprises two parallel loops with similar architectures, one to set the output current amplitude and the other to adjust the phase. They were realized by measuring the output signal through nonlinear feedback topologies. In one loop, this signal is down-converted by an I signal, and the resulting dc voltage is compared with a control voltage to set the current amplitude. In the other loop, the phase delay is controlled by demodulating the output with a Q signal and comparing the resultant dc voltage with zero. The circuit uses an external function generator to provide the required I and

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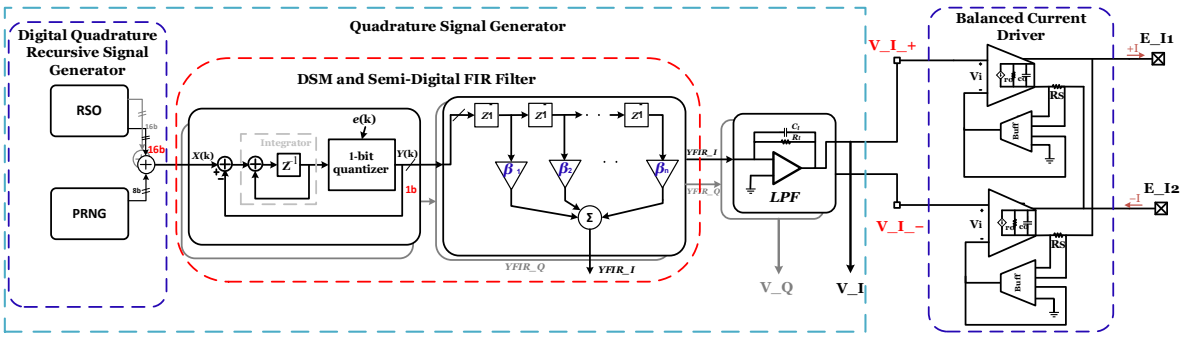

Fig. 2. Top-level system architecture of the designed signal generator and current driver.

Q signals. It generates up to 1.8 $mA_{p\text{-}p}$ using a supply voltage of ±2.5 V and occupies an area of 1.2 mm^2.

As shown in Fig. 2, the present work employs a quadrature recursive signal oscillator (QRSO) aiming to achieve low power consumption and low area while generating a high-quality differential current with a relatively wide linear range of up to 0.7 $mA_{p\text{-}p}$. Designing a compact QRSO with a semi-digital weighted-tabs FIR filter for I/Q signal generation provides the required signals for both the current injection and I/Q demodulation at the voltage recording side. The current driver uses current feedback with only one amplifier stage on the main path and with all the input differential pairs operating in weak inversion to minimize the power consumption.

The rest of this Brief is organized as follows. Section II describes the semi-digital signal generator that generates the I and Q signals. Its design features a QRSO and a delta-sigma modulator (DSM) with added dither that works in conjunction with a semi-digital FIR filter and an analog reconstruction filter to convert the digital signal into analog. The generated I signal is applied to the current driver which is detailed in Section III. Measured results from the ASIC and conclusions are provided in Sections IV and V.

II. Semi-Digital Signal Generator

As shown in Fig. 2, the digital signal generator comprises a 16-bit QRSO, a pseudorandom number generator (PRNG) block, a DSM and a semi-digital FIR filter.

A. 16-bit QRSO

A conventional and relatively simple digital approach to generate sinusoidal signals uses direct digital frequency synthesis. In this method, one cycle (or a half or a quarter cycle) of the signal is stored in a look-up table; the reading speed from the table defines the output signal frequency. To achieve larger frequencies, some of the stored datapoints in the memory are truncated which results in harmonic spurs in the output signal. The SNR depends on the length of the memory and the memory size increases exponentially with respect to the required SNR [10]. An alternative approach to generate I/Q signals relies on recursive signal oscillation (RSO). The principle behind RSO is to estimate the new sample of the signal based on the previous steps [11]:

$$x[n+2] = ax[n+1] - x[n], \tag{1}$$

where $x[n+2]$ represents the new step and $x[n+1]$ and $x[n]$ correspond to samples at one and two previous iteration(s), respectively. Also, a is a coefficient determined based on the trigonometric sum and difference of the angle identities.

An RSO that generates equi-amplitude quadrature signals has been adopted here; the generated signal can be used for both current injection and demodulation of the recorded signal. An important consideration factor in the choice of QRSO is to minimize the number of multipliers as they can considerably affect the computation and hardware cost. One method for quadrature signal generation is the modified coupled-form QRSO, where updating one sequence is dependent upon the other. As shown in Fig. 3, this can be implemented with only two multipliers [9].

The rotation matrix of this configuration is:

$$A = \begin{bmatrix} 1-k^2 & k \\ -k & 1 \end{bmatrix}. \tag{2}$$

Based on (2), the amplitudes of the I and Q signals are equal. However, the quadrature relation between $x_I[n]$ and $x_Q[n]$ is only applicable for small values of the multipliers' k coefficient, defined as:

$$k = 2\,sin(\theta/2). \tag{3}$$

Given the sample frequency (i.e. clock frequency), θ can determine the frequency of the output signals generated by the oscillator:

$$\theta = 2\pi f_{out}/f_s. \tag{4}$$

Assigning $2+b$ bits to k (one bit for the sign, one bit for the integer part and the rest for the fractional part), the frequency range of the oscillator can be calculated based on the word length of k. With b-bits allocated to the fractional part of k, its largest value would be $2-2^{-b}$ and, therefore, the minimum and maximum values of θ are:

$$\theta_{min} = 2\,sin^{-1}[(2^{-b})/2] \tag{5}$$

$$\theta_{\max} = 2\,\sin^{-1}[(2-2^{-b})/2].$$

In this design, the coefficient k is a 16-bit input (14 bits for the fractional part) serially sent through a UART to the QRSO,

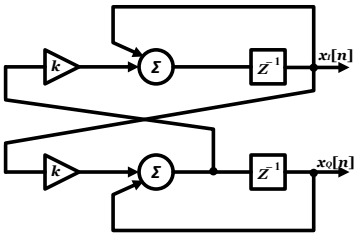

Fig. 3. Network diagram of the incorporated equi-amplitude coupled-form oscillator based on [9].

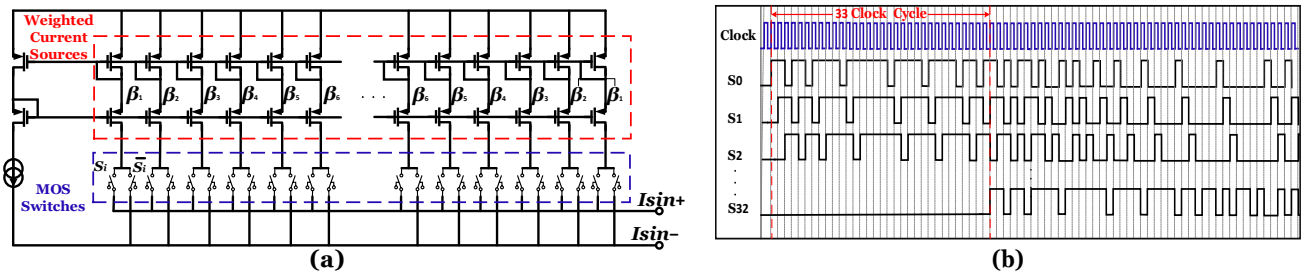

Fig. 4. Schematic of the semi-digital FIR filter with the current mirror transistors' aspect ratio being set by the filter's coefficients that are symmetrical about the center **(a)** and the switches' control signals coming from the digital DSM **(b)**.

and f_s is 12 MHz. This enables the QRSO to generate up to 6-MHz signals.

B. PRNG, DSM and FIR Filter

The digital signals need to be converted into analog for use in the subsequent analog stages. As shown in Fig. 1, a first-order DSM is used to convert the 16-bit input to only 1 bit using a noise shaping block [12]. Condensing bit numbers to one can add significant quantization noise to the signal. However, most of the energy of this noise is well beyond the signal bandwidth and can be removed with a reconstruction filter [13]. To eliminate the appearance of periodic spurious tones in the DSM output, a PRNG implemented with an 8-bit shift register is used to add dither to the 16-bit I/Q signals prior to the DSM block [12], [14]. Considering the target bandwidth of 200 kHz, setting the clock frequency to 12 MHz results in an oversampling rate of more than 30 while keeping the power consumption at a low level.

In order to relax the requirements for the analog reconstruction filter, the delta-sigma modulated signal is first low-passed filtered using a semi-digital filtering. An FIR filter smoothens the signal by taking the weighted average of its sequence for a finite interval of $M+1$ (0 to M) as denoted by its transfer function:

$$H(Z) = \sum_{k=0}^{M} \beta_k Z^{-1}, \qquad (6)$$

where Z^{-1} represents delay units that can be implemented by an $M+1$-bit digital shift register (in this work M = 32) and the coefficients (β_k) can be multiplied by the signal at each tab of the filter using switched current sources as shown in Fig. 4. The current sources are implemented with MOS transistors in current mirror configuration with their size (W/L) proportional to the FIR filter coefficients. The signal amplitude can be set by adjusting the current at the branch with the smallest coefficient. The switches are complementary MOS switches with added dummies to minimize charge injection, controlled by the signals from the DSM, and the consecutive delayed versions of them (S_i and $\bar{S}_i$). A 32-tab linear-phase FIR filter based on the frequency sampling technique was designed in MATLAB with a 3-dB cut-off frequency of 370 kHz (Fig. 5). The filter coefficients are symmetrical about the center. Following the FIR filter circuit, another stage of a first-order LPF with a cut-off frequency of 240 kHz is used (with off-chip R_l and C_l values of 30 kΩ and 22 pf) to further smoothen the generated signal and remove the higher-order harmonics.

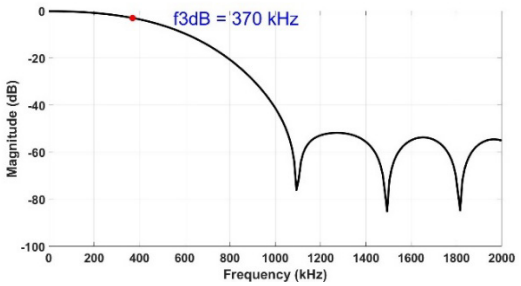

Fig. 5. Transfer function of the FIR filter designed based on the frequency sampling technique.

III. Current Driver

To ensure that the current is well delivered to the target tissue via the electrodes, a current driver with a high output impedance is required. Any mismatch in the injected and collected current to and from the tissue would flow to the large output impedance of the driver and lead to a common-mode voltage at the same frequency as the signal [15]. The current driver topology used is shown in Fig. 6. It is based on a balanced, closed-loop architecture previously introduced in [16]. The objectives were to have a low-power driver with high precision and wide dynamic range. The designed driver uses a supply of ±0.8 V and can generate a balanced current of up to 0.7 $mA_{p\text{-}p}$. As shown in Fig. 6, the main path consists of an operational transconductance amplifier (OTA) and a differential difference amplifier (DDA) as a buffer. The input differential pairs in both circuits are biased in weak inversion to minimize power consumption while reducing the input referred noise within the 200 kHz bandwidth of the amplifiers. The simulated power consumptions of the OTA and the DDA buffer are 0.87 mW and 0.2 mW, respectively. Employing a balanced driver with negative current-mode feedback in a structure similar to that shown in Fig. 2, the driver's output current can be monitored through the sense resistor R_s. If the current exceeds a threshold, the input voltage of the amplifier reduces through the buffer in the feedback loop that can subsequently adjust the output current. The transconductance of the current source (upper) path of the driver in Fig. 2 can be calculated using [17]:

$$G_{driver} = G_m/\left(\frac{r_o+R_L+R_S}{r_o} + (R_L+R_s)c_o s + G_m R_S\right), \qquad (7)$$

where G_m, r_o and c_o are the open loop transconductance, output resistance and parasitic capacitance of the main path OTA, respectively. At low frequencies, if r_o is sufficiently large, the derived transconductance can be approximated as $1/R_s$. The G_m in this design is 2.5 mA/V and the sense resistance was set to 500 Ω resulting in an overall transconductance for both the current source and sink paths of ~2.22 mA/V. From simulations, an overall differential gain of 2.27 mA/V was achieved for the driver. The output resistance for each path of

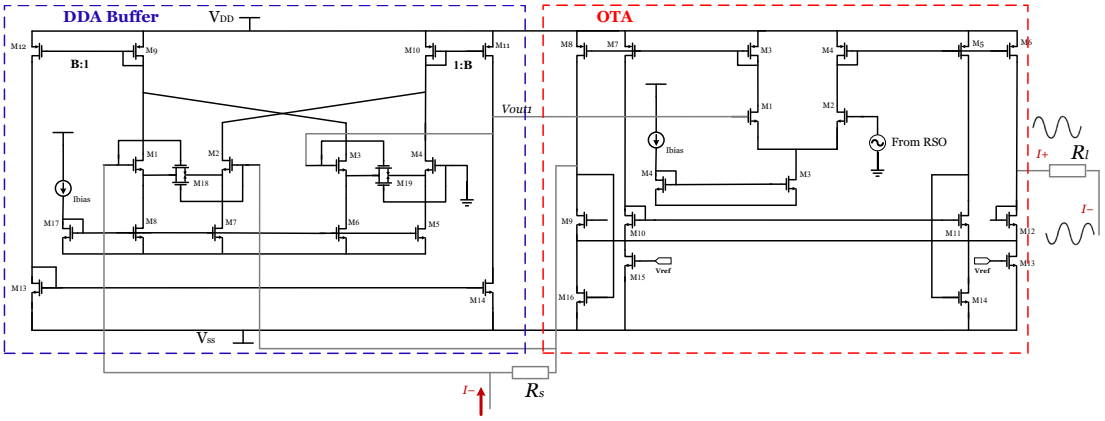

Fig. 6. Schematic of the symmetrical OTA and the DDA-based buffer in the current driver.

the current driver (sink or source) can be calculated as:

$$R_{out} = R_{out(OTA)} + R_s(1 + G_m R_{out(OTA)}), \qquad (8)$$

where $R_{out(OTA)}$ is the output impedance of the OTA (40 kΩ). G_m = 2.5 mA/V, R_s = 500 Ω and the simulated overall output impedance of the current driver is 41 kΩ up to about 30 kHz, reducing to 33 kΩ at 200 kHz. Changing the load from 100 Ω to 5 kΩ, the driver's transconductance only changes by 0.1 mA/V.

IV. Measured Results

The system comprises a QRSO that can generate I and Q signals up to about 240 kHz frequency and a current driver with an output up to 0.7 mA_{p-p}. The digital block, including the QRSO, the two DSMs, PRNGs and 33-bit shift registers (one for each I and Q signal) consumes 0.8 mW and operates with a 1.2 V power supply. The entire analog part consisting of the FIR filters, LPFs and current drivers for both I and Q signals consumes a total of 5.36 mW with a 1.6 V supply (consequently, the power consumption for a single current generator path would be this figure divided in half). Fig. 7 (a) and (b) show the measured I and Q signals from the output of the reconstruction filter at 45 kHz and 180 kHz frequencies, respectively. The linear phase nature of the designed FIR filter results in signals that undergo a non-frequency dependent delay. The measured phase difference between the I and Q signals only varies from 90.72° at 45 kHz to 92.19° at 90 kHz and 92.34° at 180 kHz. Fig. 8 and Fig. 9 show the FFT and time-domain voltage recorded from the output of the current driver applied to a 1-kΩ load when it is driven by a 180-kHz signal from the on-chip oscillator. This is equivalent to injecting 506 μA_{p-p} symmetrical current to the load. Fig. 10 shows the chip micrograph with the digital and analog module highlighted.

V. Conclusion

In this Brief the design and implementation of a low-power digital signal generator and a current driver – with the ultimate aim of being incorporated in an EIT lung function monitoring device – have been presented. An ASIC has been fabricated in TSMC 65 nm technology with the digital and analog parts operating with 1.2 V and ±0.8 V power supplies, respectively. While most of the similar available designs only provide I signals, this system incorporates recursive signal oscillation to generate quadrature signals in a wide range of frequencies that can be used for I/Q demodulation of a recorded bioimpedance. The generated I signal is applied to a current driver with current feedback that incorporates low-power design techniques and minimizes the output common-mode voltage, generating up to 0.7 mA_{p-p} current. Table I provides a comparison between the designed current generator and other published state-of-the-art drivers. Compared to previous work, the present design has a wide linear range for a low supply voltage and a high bandwidth.

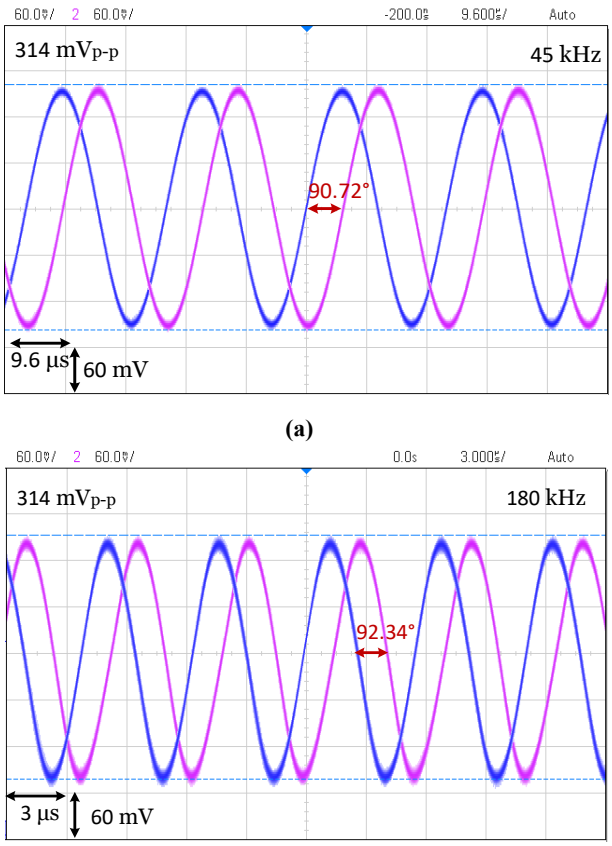

Fig. 7. Measured in-phase and quadrature-phase outputs from the signal generator for **(a)** 45 kHz and **(b)** 180 kHz.

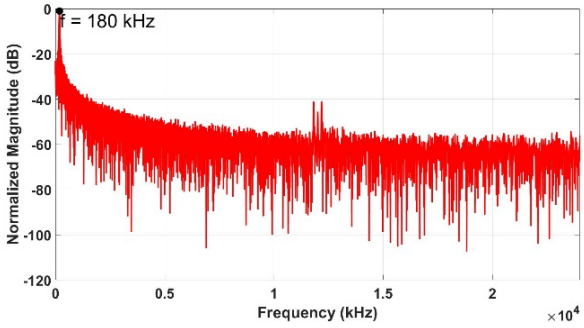

Fig. 8. FFT spectrum of the signal measured from the current driver's output at 180 kHz.

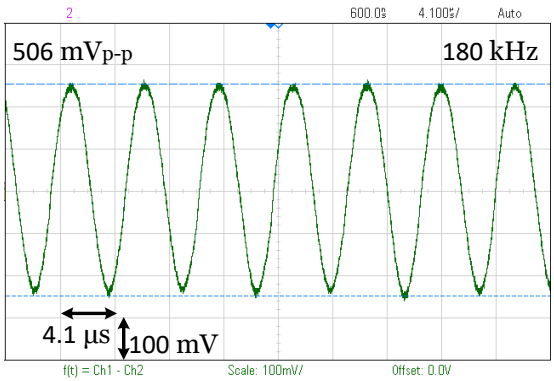

Fig. 9. Differential voltage recorded at the output of the current driver applied to a 1 kΩ load resistance, equivalent to 506 $\mu A_{p\text{-}p}$ current.

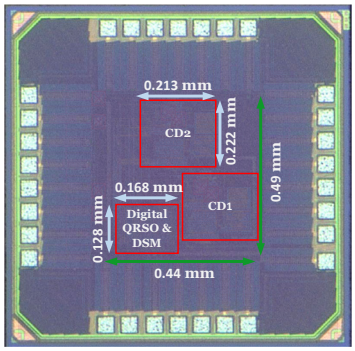

Fig. 10. The ASIC micrograph of the QRSO and current drivers (CDs).

TABLE I
CURRENT DRIVER PERFORMANCE COMPARISON

Tech. (nm)	Sup. (V)	Max I_{out} (mA)	R_{out} (kΩ)	P (mW)	BW (M Hz)	Ref.
65	±0.8	0.7	40 @ 30 kHz	2.7	0.2	This work
65	0.5	0.002	2	0.0062	0.02	[18]
180	1.2	0.16	55 @ 160 $\mu A_{p\text{-}p}$	0.055 @ 40 $\mu A_{p\text{-}p}$	0.02	[12]
180	±1.65	1	750 @ 500 kHz	N/A	0.5	[17]
180	3.3	2.7	300 @ 1 MHz	13	40	[19]
350	±2.5	1.8	1×10^3 @ 3 MHz	15	3	[8]

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