An 89.3% Current Efficiency, Sub 0.1% THD Current Driver for Electrical Impedance Tomography

Jiayang Li, *Student Member, IEEE*, Dai Jiang, *Senior Member, IEEE*, Yu Wu, *Member, IEEE*, Nazanin Neshatvar, *Member, IEEE*, Richard Bayford, *Life Senior Member, IEEE*, and Andreas Demosthenous, *Fellow, IEEE*

***Abstract*—Accurate electrical impedance tomography (EIT) measurements require a current driver with low total harmonic distortion (THD) and high output impedance. Conventional EIT current drivers attain good performance for these parameters but at the expense of low current efficiency. This Brief presents a differential current driver based on a current feedback structure with isolated common-mode feedback, achieving very low THD, high output impedance and high current efficiency. In addition, it uses current DACs to remove any dc offsets at the output nodes. The current driver was fabricated in a 65-nm CMOS technology with 3.3 V supply. Measured results demonstrate a THD of 0.05% and 0.1% at 80 kHz, for 1 mA_{p-p} and 1.375 mA_{p-p} output current, respectively. The total current consumption is 1.54 mA, resulting in a maximum current efficiency of 89.3%. The measured output impedance is 1.023 MΩ at 500 kHz and 568 kΩ at 1 MHz.**

***Index Terms*—Common-mode feedback, current driver, current feedback, electrical impedance tomography (EIT), high current efficiency, low THD.**

I. INTRODUCTION

THERE has been growing popularity in electrical impedance tomography (EIT) to provide real-time monitoring. As a low-cost and radiation-free imaging technique, EIT has been widely used in biomedical applications, for example, continuous respiratory monitoring, breast cancer detection, cardiac imaging, and brain activity monitoring [1]. EIT images the variation of electrical bioimpedance inside a volume of interest by applying an ac current and measuring the induced voltage via an array of surface electrodes surrounding the volume. To achieve high accuracy, the current driver must have accurate transconductance, low total harmonic distortion (THD) and high output impedance [2]. The biomedical application may require current amplitudes of a few milliampere [3]. In addition, as advanced EIT hardware tends toward miniaturized, wearable systems [4], [5], high efficiency current driver design is necessary.

Most current drivers for EIT and bioimpedance measurements use voltage-to-current (V-I) converters. Several V-I current drivers having linear feedback have been reported [6]-[10]. They achieve good transconductance, low THD and high output impedance but at the expense of low current efficiency, typically less than 50% due to the complex feedback structures used (for providing an accurate transconductance) and the need for good linearity. In contrast, DAC-based current drivers utilizing an open-drain current mirror for output current drive [11] can provide high current efficiency and acceptable THD, but their output impedance is usually low, thus unsuitable for EIT.

This Brief describes a differential V-I current driver based on current feedback architecture for EIT with an 89.3% current efficiency and sub 0.1% THD, featuring well-defined transconductance and high output impedance. Current feedback is commonly applied to instrumentation amplifier design for its good linearity and well-defined transconductance. However, in a differential current driver for EIT or bioimpedance measurements the use of current feedback can significantly degrade the output impedance due to the added common-mode feedback resistors. In [10], to increase the output impedance, the current driver employs pseudo resistors in the common-mode feedback, but they greatly limit the output voltage range to tens of mV, and it has low current efficiency (<30%). In the proposed design, an isolated common-mode feedback architecture [12] is realized enabling the current driver to attain high output impedance (>1 MΩ) and large output voltage range (5 V differential) suitable for EIT. The current driver also has calibration current DACs to eliminate dc offsets in the output ac current.

The rest of this Brief is organized as follows. Section II describes the circuit architecture and operating principles. It also examines the tradeoff between THD and current efficiency to provide an optimized design. Measured results from the fabricated current driver chip are presented in Section III. Comparison with other work and concluding remarks are detailed in Section IV.

II. CIRCUIT DESIGN

A. Current Driver Architecture

The simplified schematic of the current driver is shown in Fig. 1. It comprises three parts: (a) a degenerated fully-differential transconductance stage (transistors M1 to M6, M15 to M18, resistor R_{in}) that converts the differential input sinusoidal voltage, V_{in}, into current; (b) an output cascode stage (transistors M7 to M14) with an isolated common-mode feedback loop (buffer amplifiers A_1, A_2 A_3, resistors R_1, R_2)

Manuscript received 1 April. 2023; revised 13 June 2023, and 02 July 2023. The authors are with the Department of Electronic and Electrical Engineering, University College London, Torrington Place, London WC1E 7JE, UK. E-mail: jiayang.li.21@ucl.ac.uk; a.demosthenous@ucl.ac.uk.

This work was supported by the UK Research and Innovation (UKRI) under EPSRC grant no. EP/T001259/1.

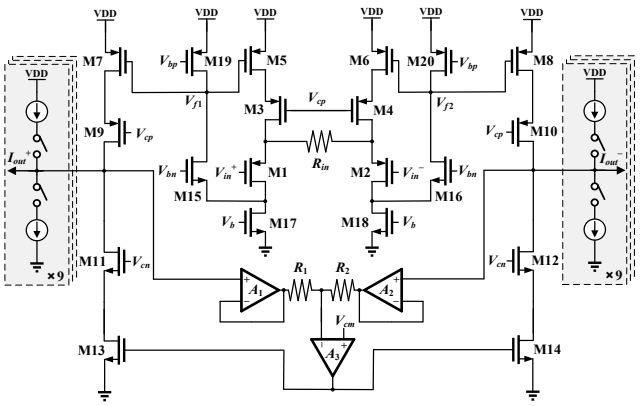

Fig. 1. Simplified circuit schematic of the proposed current driver.

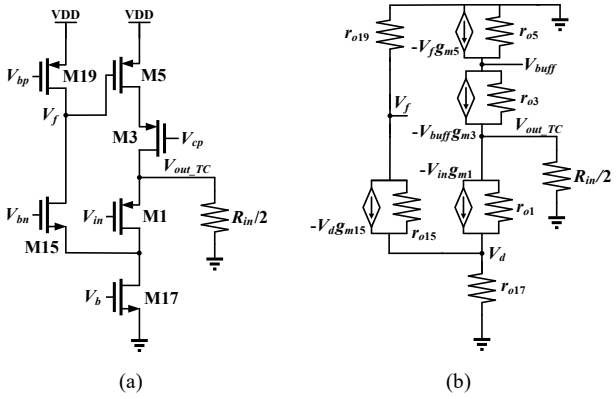

Fig. 2. (a) Half circuit of the transconductance stage and (b) its equivalent small signal model.

for differential current output (I_{out}); and (c) two 9-bit sink-source current DACs for offset calibration. The isolated common-mode feedback loop stabilizes the common-mode voltage at the output nodes without decreasing the output impedance of the current driver. When blocking capacitor are inserted in series with the output nodes and the electrodes, the current DACs are used to minimize any residual dc offset to avoid saturation.

B. Transconductance Stage Analysis

The half circuit of the transconductance stage and its equivalent small signal model are shown in Fig. 2. The V-I conversion is achieved by forcing a voltage drop across resistor R_{in}. A flipped-voltage follower, which has improved linearity compared with traditional source followers, provides this voltage drop. As shown in Fig. 2(a), M1, M17 and M5 are input, current source and feedback transistors, respectively. The auxiliary common-gate amplifier composed of M15 and M19 operates as a drain regulator, forcing the drain voltage of M17 to a constant dc value. The regulated drain voltage and the defined gate voltage of M17 forms a high-quality current source. The open loop gain V_f/V_{in} is given by

$$\frac{V_f}{V_{in}} = [g_{m15}(r_{o15} \parallel r_{o19})] \cdot \left(\frac{g_{m1}}{1+g_{m1}(\frac{R_{in}}{2} \parallel (g_{m3}r_{o3}r_{o5}))}\right) \cdot \{[r_{o1}g_{m1}(\frac{R_{in}}{2} \parallel (g_{m3}r_{o3}r_{o5}))] \parallel r_{o17} \parallel (\frac{1}{g_{m15}} + \frac{r_{o19}}{g_{m15}r_{o15}})\} \quad (1)$$

where the symbols have their usual meaning.

For closed-loop analysis, M3 can be considered as a current buffer and its impact can be ignored. The equivalent transconductance of the input transistor M1 is expressed as

$$G_{m\_M1} = \frac{g_{m1}}{1+g_{m1}(\frac{R_{in}}{2} \parallel (g_{m3}r_{o3}r_{o5})} + \frac{V_f}{V_{in}} g_{m5}. \quad (2)$$

The equivalent output impedance from node V_{out_TC} is

$$R_{out\_TC} = \left(\frac{1}{g_{m1}} + \frac{\left(\frac{1}{g_{m15}} + \frac{r_{o19}}{g_{m15}r_{o15}}\right) \parallel r_{o17}}{g_{m1}r_{o1}}\right) \parallel \frac{1}{\frac{V_f}{V_{in}}g_{m5}} \parallel \frac{R_{in}}{2} \parallel r_{o5}. \quad (3)$$

Since the open loop gain V_f/V_{in} is very large, the equivalent output impedance can be simplified to

$$R_{out\_TC} \approx \frac{1}{\frac{V_f}{V_{in}}g_{m5}}. \quad (4)$$

Thus, the voltage gain of the transconductance stage is

$$\frac{V_{out\_TC}}{V_{in}} = G_{m\_M1} \cdot R_{out_{TC}} = \frac{\frac{g_{m1}}{1+g_{m1}(\frac{R_{in}}{2} \parallel (g_{m3}r_{o3}r_{o5})} + \frac{V_f}{V_{in}}g_{m5}}{\frac{V_f}{V_{in}}g_{m5}} \approx 1. \quad (5)$$

Since the voltage gain is equal to 1, the input differential voltage will be copied across resistor R_{in} and generate a current equal to $2V_{out\_TC}/R_{\text{in}}$. By amplify this current at the output stage, the transconductance of the current driver is given by

$$G_{m\_current\_driver} = \frac{2V_{out\_TC}}{R_{in}} \cdot \frac{K}{2V_{in}} = \frac{K}{R_{in}} \quad (6)$$

where K is the ratio of the current mirrors M5-M7 and M6-M8 in Fig. 1. In this design the feedback loop does not need any compensation due to the dominant pole formed by the gate parasitic capacitances of M5-M6 and M7-M8.

C. Tradeoff Between THD and Current Efficiency

The current efficiency of a current driver is defined as the maximum output current over the total current consumption. To maximize current efficiency, the maximum output current of the current driver should be set as close as possible to the total current consumption. At this point, the bias current at one of the differential branches will significantly decrease when the output current reaches its peak value. In state-of-the-art feedback current drivers [7]-[9], decreased bias current will significantly decrease the loop gain, which will result in unwanted distortion in the output current and inaccurate transconductance of the current driver. In the proposed design in Fig. 1, this limit is relaxed, because the bias current of the input transistor M1 (and M2) and auxiliary common-gate amplifier M15, M19 (and M16, M20) are constant. As a result, the input transistor transconductance g_{m1} and the common-gate amplifier voltage gain $g_{m15}(r_{o15} \parallel r_{o19})$ are constant. By keeping these two terms large enough, the open loop gain V_f/V_{in} in (1) is still large enough even when the output current reaches the peak value and the small signal analysis in (1) to (6) is still valid.

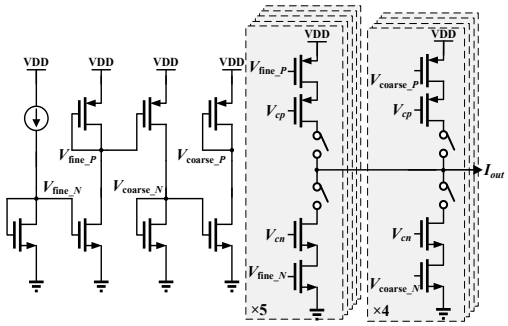

Fig. 3. Simplified circuit schematic of the calibration DACs with coarse and fine resolution bits.

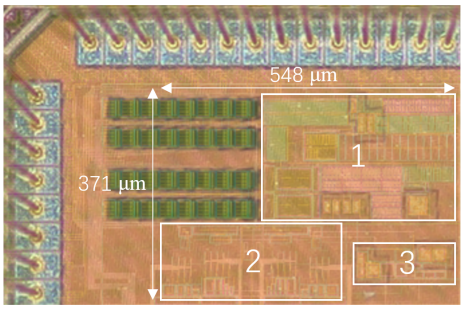

Fig. 4. Chip micrograph of the current driver with (1) core circuit of the current driver, (2) calibration DACs and (3) bias blocks.

In order to achieve low THD at large output currents while maximizing current efficiency, the current mirror ratio K in (6) should be as large as possible. However, there are two limitations. Firstly, the transconductance of the input transistor of transconductance stage and the voltage gain of the common-gate amplifier should be sufficiently large as discussed above. Secondly, the bandwidth of the transconductance stage should be much wider than the signal frequency. Since the conversion from the current $2V_{out\_TC}/R_{\text{in}}$ to V_{f1}, V_{f2} (see Fig. 1) is non-linear, it contains high order harmonics. These high order harmonics are necessary for high-fidelity sinusoidal current reconstruction at M7 and M8. This non-linear conversion becomes more significant when the peak amplitude of the output current is close to the bias current at the output stage. The upper limit of K should be identified for these two limitations. Following experimental simulations, in the proposed design the bandwidth of the transconductance stage was chosen to be 10 times higher than the signal frequency and the ratio K was set to 11.

D. Isolated Common-Mode Feedback

In traditional current feedback instrumentation amplifiers, the common-mode voltage at the output is defined by two small common-mode feedback resistors, contributing to low output impedance [13]. In EIT measurements, a current driver with megohms output impedance is typically required to guarantee the accuracy of the output current magnitude against load variation (from a few hundreds of ohms to a few tens of kilo-ohms). Implementation of resistors in the mega-ohm range are not realistic for a fully integrated design. An isolated common-mode feedback scheme is adopted to address this issue. As shown in Fig. 1, instead of using two resistors directly connected to the output nodes, unity-gain buffers, A_1 and A_2, are added between the output nodes and the feedback resistors to isolate them. Buffer A_3 provides the feedback. The input of the unity-gain buffer is a high impedance node and does not reduce the output impedance of the current driver. The differential voltages at the output nodes are copied by the buffers and used to extract the common-mode signal from the two feedback resistors R_1, R_2. Each unity-gain buffer is a basic five-transistor operational transconductance amplifier with a 10 µA tail current. The transistors in the buffers are biased in the subthreshold region to increase the input range. The value of the feedback resistors R_1 and R_2 in this design is 170 kΩ.

E. dc offset DACs

In clinical applications any dc current through the electrodes is undesirable. Medical device regulations specify a safe limit of 100 µA for current flow between electrodes at frequencies below 1 kHz [14]. A common practice is to insert blocking capacitors in series with the electrodes. This results in very high impedance nodes for dc current at the current driver outputs, which may saturate its output stage due to process and mismatch variations. To address this issue, two 9-bit sink-source current DACs are implemented to calibrate the dc current offset. As shown in Fig. 3, the current DAC has a 5-bit fine-resolution stage with a least significant bit (LSB) of 50 nA and a 4-bit coarse-resolution stage with an LSB of 1.25 µA. A current driver with a dc output impedance of 2 MΩ, using a a 50 nA LSB, the maximum residual dc voltage offset at each side of its differential output is 50 mV, which is acceptable for most applications. The LSB current in the coarse-resolution stage is designed to be lower the sum of all the fine-resolution stages to avoid missing codes during calibration. The current DAC can provide a maximum calibration current of 20.25 µA at each side. This covers all the 370 cases in Monte-Carlo simulation.

III. Measured Results

The current driver chip was fabricated in TSMC 65 nm CMOS technology with 3.3 V supply. As shown in Fig. 4, the current driver occupies a total area of 0.2 mm^2. The circuit design, simulation and layout were developed in Cadence Virtuoso. Five chips were tested. An APX555 Audio Analyzer (Audio Precision, USA) and a KEYSIGHT 33600A Waveform Generator (Keysight, USA) were used to provide the differential input sinusoidal signals. The output signals were measured on a KEYSIGHT MSOX3024T Mixed-Signal Oscilloscope (Keysight, USA). All the data calculations were processed in MATLAB. The measured current consumption at the maximum output current of 1.375 mA$_{p\text{-}p}$ is 1.54 mA.

A. Output Impedance

The measured output impedance of the current driver over the frequency range of 10 kHz to 1 MHz is shown in Fig. 5. The method proposed in [4] was used to remove the impact of the PCB stray capacitance. Five chips were measured, and their results were averaged. The current driver achieves an output impedance of 1.023 MΩ at 500 kHz and 568 kΩ at 1 MHz, which is sufficient for most EIT applications.

TABLE I. COMPARISON OF CURRENT DRIVERS

Parameter	[7]	[8]	[9]	[10]	[11]	This work
Topology	V-I	V-I	V-I	V-I	Current DAC	V-I
CMOS Process	350 nm	180 nm	65 nm	65 nm	180 nm	65 nm
Supply Voltage	±2.5 V	1.5 V	1.2 V	0.5 V	1.2 V	3.3 V
Max Output Current	1.8 mA_{p-p}	350 μA_{p-p}	400 μA_{p-p}	2 μA_{p-p}	160 μA_{p-p}	1.375 mA_{p-p}
Current Consumption	3 mA	1.33 mA	2.02 mA	8.76 μA_p	207.8 µA	1.54 mA
Output Impedance	1 MΩ @ 3 MHz	>100 kΩ @ 1 MHz	1 MΩ @ 1 MHz	331 kΩ @ 20 kHz	55 kΩ @ 20 kHz	>1MΩ @ 500 kHz
THD	0.4% @ 1 mA_{p-p}	<1% @ 250 μA_{p-p}	0.5% at 400 μA_{p-p}	0.088% @ 2 μA_{p-p}	<0.4% at 160 μA_{p-p}	0.1% @ 1.375 mA_{p-p}
Current Efficiency	60%	26.2%	19.8%	22.8%	76.9%	89.3%
FoM[a]	251[b]	2.62	39.6	1.71	0.211	457

[a] $\text{FoM} = \frac{\text{Current Efficency (\%)} \times [\text{Output Impedance (M}\Omega) \times \text{Frequency of Measured Output Impedance (MHz)}]}{\text{THD @ Max Output Current (\%)}}$; [b] Current efficiency at the measured THD was used for calculation.

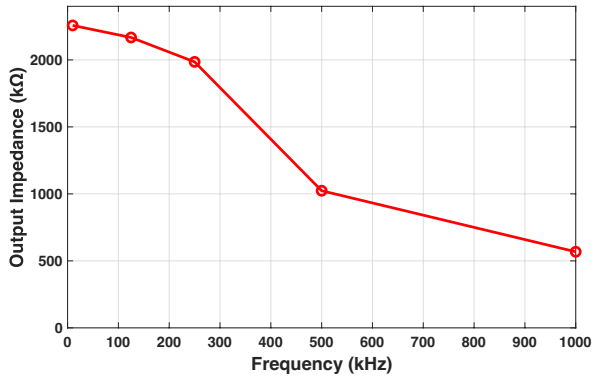

Fig. 5. Measured output impedance of the current driver from 10 kHz to 1 MHz averaged over five chips.

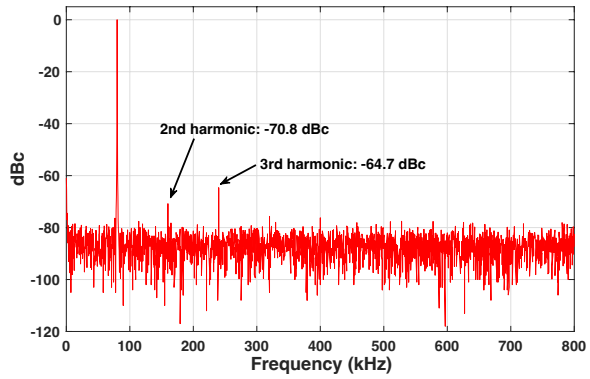

Fig. 6. FFT analysis of the output voltage of the current driver with 1.25 mA_{p-p} current output and 2 kΩ load at 80 kHz, measured with APX555.

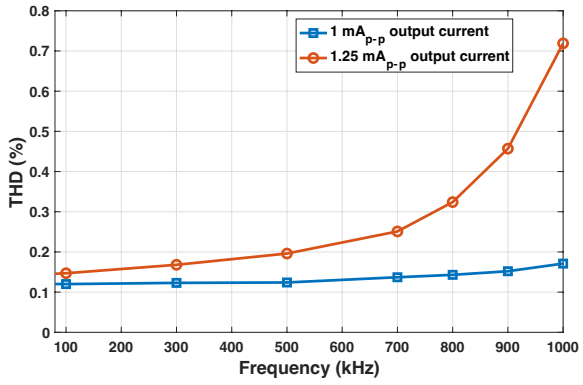

Fig. 7. THD performance of the current driver versus frequency at 1 mA_{p-p} and 1.25 mA_{p-p} output current with 2 kΩ load, measured with KEYSIGHT 33600A.

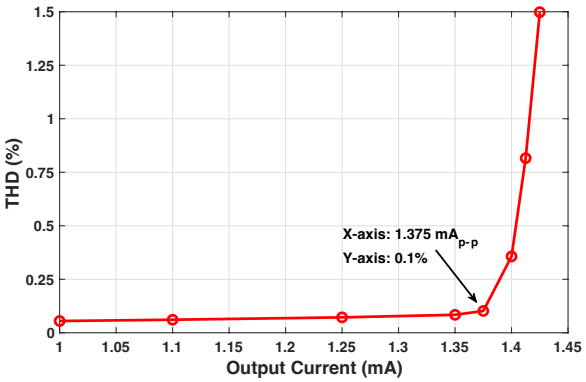

Fig. 8. THD performance versus output current magnitude with 2 kΩ load at 80 kHz, measured with APX555.

B. THD Performance

For precise THD measurement, the input differential sinusoidal signal must be pure enough to guarantee it will not generate distortion at the output. The APX555 Audio Analyzer, which has an intrinsic THD of 120 dBc, was used to provide accurate THD analysis. One of the five chips was selected to present the THD measurements. Fig. 6 shows the fast Fourier transform (FFT) analysis of the output voltage with a 2 kΩ resistor load and 1.25 mA_{p-p} output current at 80 kHz. The current driver achieves a THD of 0.07% under this condition.

The KEYSIGHT 33600A waveform generator was used for wideband measurements due to the limited bandwidth of the APX555 analyzer (80 kHz). However, it has an intrinsic THD around 55 dBc, which would significantly degrade the measured THD performance. A second-order differential passive low pass filter with a bandwidth of 80 kHz was used between the waveform generator and the input of the current driver to reduce the THD contributed by the waveform generator. The consistency of the magnitude of the current driver's input voltage at different frequencies was achieved by adjusting the magnitude of the output voltage of the signal generator. After the low pass filter, the THD of the voltage generated by KEYSIGHT 33600A is roughly reduced by 0.05%, but still around 0.08% larger than that generated by APX555. The measured THD versus frequency for a 2 kΩ load is shown in Fig. 7.

C. Current Efficiency and THD

According to the analysis in Section II, the requirement of

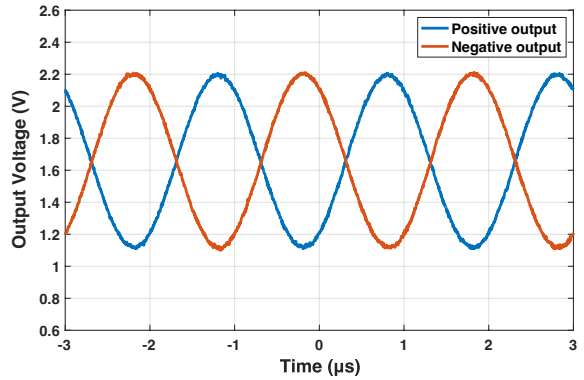

Fig. 9. Differential output voltages at 500 kHz. The DAC calibration removes dc offsets at the current driver output nodes when using blocking capacitors.

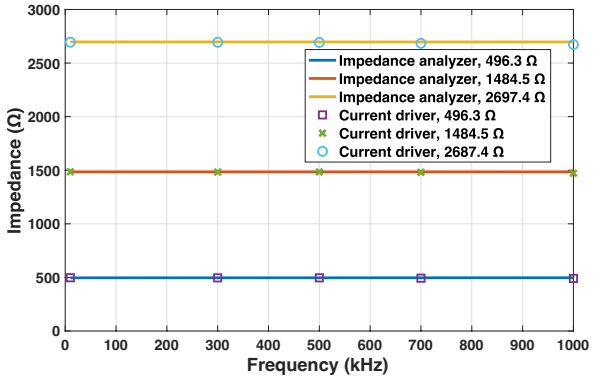

Fig. 10. Measured impedance of the current driver versus impedance analyzer.

good THD performance severely limits the current efficiency of state-of-the-art current drivers. For consistency, the same chip used to present the THD performance was also chosen to present the current efficiency performance. The measured THD versus different output currents is shown in Fig. 8. The results were obtained with the APX555 analyzer at 80 kHz and a 2 kΩ load impedance. The current driver has a THD performance of 0.1% with a maximum output current of 1.375 $mA_{p\text{-}p}$, resulting in a current efficiency of 89.3%.

D. Calibration DACs

Fig. 9 shows the measured differential output voltages with a 2 kΩ load impedance of a typical chip; 10 nF blocking capacitors were used for current drive at 500 kHz frequency. The dc offset was effectively removed by the calibration DACs.

E. Impedance Measurements

Fig. 10 compares impedance measurements using the current driver against a WAYNE KERR 6500B impedance analyzer. The tested loads varied from 500 Ω to 2.7 kΩ. The impedance data of the current driver were calculated from the measured output voltage divided by the output current. The fabricated current driver chip provides well-matched impedance measurements for different load impedances and frequencies.

IV. Comparison and Conclusion

A current driver with current feedback has been designed to provide high-fidelity output differential current with very low THD and high current efficiency. It has high output impedance, high output currents and wideband operation. Table I provides a comparison with state-of-the-art current drivers. The current driver in this work has one of the lowest THD and highest current efficiency. It achieves the best tradeoff (figure-of-merit; FoM) between current efficiency, output impedance, bandwidth and THD amongst the state-of-the-art current drivers.

References

[1] Y. Wu, F. F. Hanzaee, D. Jiang, R. H. Bayford and A. Demosthenous, "Electrical impedance tomography for biomedical applications: Circuits and systems review," *IEEE Open J. Circuits Syst.*, vol. 2, pp. 380-397, 2021.

[2] Y. Wu, D. Jiang, R. Yerworth, and A. Demosthenous, "An imaged based method for universal performance evaluation of electrical impedance tomography systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 3 pp. 464–473, 2021.

[3] I. Frerichs, "Electrical impedance tomography (EIT) in applications related to lung and ventilation: A review of experimental and clinical activities," Physiol. Meas., vol. 21, no. 2, pp. R1–R21, 2000.

[4] Y. Wu, D. Jiang, A. Bardill, S. de Gelidi, R. Bayford and A. Demosthenous, "A high frame rate wearable EIT system using active electrode ASICs for lung respiration and heart rate monitoring," *IEEE Trans Circuits Syst. I: Regular Papers*, vol. 65, no. 11, pp. 3810-3820, Nov. 2018.

[5] J. Lee, S. Gweon, K. Lee, S. Um, K. -R. Lee and H. -J. Yoo, "A 9.6-mW/ch 10-MHz wide-bandwidth electrical impedance tomography ic with accurate phase compensation for early breast cancer detection," *IEEE J. Solid-State Circuits*, vol. 56, no. 3, pp. 887-898, March 2021.

[6] L. Constantinou, R. Bayford and A. Demosthenous, "A wideband low-distortion CMOS current driver for tissue impedance analysis," *IEEE Trans Circuits Syst.: II: Express Briefs*, vol. 62, no. 2, pp. 154-158, Feb. 2015.

[7] N. Neshatvar, P. Langlois and A. Demosthenous, "A non-linear feedback current driver with automatic phase compensation for bioimpedance applications," *IEEE Trans Circuits Syst. II: Express Briefs*, vol. 65, no. 10, pp. 1340-1344, Oct. 2018.

[8] L. Yan, J. Bae, S. Lee, T. Roh, K. Song and H. -J. Yoo, "A 3.9 mW 25-electrode reconfigured sensor for wearable cardiac monitoring system," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 353-364, Jan. 2011.

[9] J. Jang, M. Kim, J. Bae and H. -J. Yoo, "A 2.79-mW 0.5%-THD CMOS current driver IC for portable electrical impedance tomography system," *2017 IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Seoul, Korea (South), 2017, pp. 145-148.

[10] K. Kim, S. Kim and H. -J. Yoo, "Design of sub-10-µW sub-0.1% THD sinusoidal current generator IC for bio-impedance sensing," *IEEE J. Solid-State Circuits*, vol. 57, no. 2, pp. 586-595, Feb. 2022.

[11] S.-K. Hong and D.-W. Jee, "A 0.052 mm2, <0.4% THD, sinusoidal current generator for bio-impedance measurement using a recursive digital oscillator and current-domain FIR filter," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 66, no. 6, pp. 894-898, June 2019.

[12] J. Li, Y. Wu, R. Bayford, D. Jiang and A. Demosthenous, "A low power, low THD current driver with discrete common-mode feedback for EIT applications," *2022 29th IEEE Int. Conf. Electronics, Circuits Syst. (ICECS)*, Glasgow, United Kingdom, 2022, pp. 1-4.

[13] A. Worapishet, A. Demosthenous and X. Liu, "A CMOS instrumentation amplifier with 90-dB CMRR at 2-MHz using capacitive neutralization: analysis, design considerations, and implementation," *IEEE Trans Circuits Syst. I: Regular Papers*, vol. 58, no. 4, pp. 699-710, April 2011.

[14] W. R. B. Lionheart, J. Kaipio and C. N. McLeod, "Generalized optimal current patterns and electrical safety in EIT," *Physiol. Meas.*, 22 85, 2001.