TITANIUM CONTACTS ON N-TYPE SILICON

by

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ABSTRACT

The current transport mechanism usually assumed to be valid for metal silicon Schottky barriers is thermionic-emission. However, Crowell and Beguwala, using a thermionic-diffusion model, suggested that significant deviations from the behaviour predicted by the thermionic-emission theory should be observed on low barriers, especially those formed on silicon of low impurity concentration. The barrier height of titanium on n-type silicon is 0.50 volt which is lower than most other metals, and should make the effects predicted by the thermionic-diffusion theory more important for titanium contacts.

Titanium contacts were prepared on n-type silicon with impurity concentration from 2×10^{20} m^{-3} to 3×10^{21} m^{-3}. Most of the diodes showed nearly ideal behaviour at low applied voltages and the current-voltage characteristics could be represented by the relationship

$$I = I_s \exp\left(\frac{qV}{nkT}\right)\left\{1 - \exp\left(\frac{-qV}{kT}\right)\right\}$$

with n values as low as 1.01. It was concluded that tunnelling, interfacial layer and surface effects were insignificant for such diodes. However, at higher current densities, many of the same diodes exhibited deviations from ideal behaviour which were equivalent to n values as high as 1.25, or which could be interpreted in terms of a rapidly decreasing saturation current I_S.

Similar effects were observed on magnesium and aluminium contacts on silicon, but at higher applied voltages, corresponding to the higher barrier heights of 0.55 and 0.72 volts.

The main features of the experimental results agreed well with the predictions of the thermionic-diffusion theory for band bending between $\beta = 9$ and $\beta = 2$. At the upper value of β, the predictions of the thermionic-emission and thermionic-diffusion theories were

almost identical and the diode behaviour was closest to ideal with $n = 1.01$. The lower value of β represents the limit of agreement between the measurements and the thermionic-diffusion theory. Two possible mechanisms are outlined which could explain the discrepancy below $\beta = 2$. These are phonon scattering of electrons between the barrier maximum and the metal, and the effect of the reserve layer on the shape of the potential barrier at very low band bending.

The results demonstrate the conditions under which the thermionic-diffusion theory rather than the thermionic-emission theory should be applied, and suggest a practical lower limit on β for the range of applicability of the thermionic-diffusion theory.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The work described in this thesis is concerned with the preparation of titanium contacts on n-type silicon, the measurement of their properties, and the explanation of their properties in terms of the existing theory. This chapter surveys the historical development of the theory of metal-semiconductor barriers and their fabrication, and relates this work to previous results in the same field. The importance of titanium contacts in present day microelectronic devices is outlined.

1.2 HISTORICAL SURVEY

Since 1874, when Braun reported the rectifying behaviour of metal point contacts to various semiconductor crystals[1], the papers published concerning metal-semiconductor device research have been so numerous that an exhaustive list will not be attempted. However, in this survey the reader will be referred to several thorough reviews which have been made by previous authors.

Henisch, in his book Rectifying Semiconductor Contacts[2], reviews the experimental and theoretical developments up to 1956. Following the formulation of semiconductor transport theory, based on the band theory of solids, by Wilson[3], theories of the transport of electrons over the barrier were developed. Wagner[4] and Schottky and Spenke[5] proposed that the current was limited by the processes of diffusion and drift through the barrier region where a surface potential barrier was present due to stable space charge in the semiconductor[6]. Bethe[7] suggested the alternative that the current was limited by the

rate of emission of electrons over the barrier from the semiconductor into the metal. Bardeen's work[8] suggested that the presence of surface states on a semiconductor would reduce the dependence of the barrier properties on the difference between the thermionic work functions of the metal and the semiconductor. Schultz[9] formulated a model of current transport across the barrier which linked the thermionic-emission model of Bethe with the diffusion model of Wagner, Schottky and Spenke.

In 1966 Mead[10] published a review paper surveying many of the recent experimental results for barriers formed on freshly cleaved semiconductors, but he did not include details of barriers formed on chemically cleaned surfaces, although there were a vast number of papers being published at that time. The influence of surface preparation on barrier properties was demonstrated by Turner and Rhoderick[11], and Smith[12] in 1968.

Meanwhile, on the theoretical side, Scharfetter[13] had predicted levels of minority carrier injection which were largely verified by the experimental work of Yu and Snow[14]. Crowell and Sze[15] presented a synthesis of the thermionic-emission and diffusion theories of carrier transport which incorporated image force lowering of the barrier and quantum mechanical tunnelling scattering of carriers. Their paper also included a quantitative check between the theoretical and experimental values for the Richardson constant[39] for emission of electrons over the barrier, and a treatment of the influence of an interfacial layer on the barrier properties.

The tunnelling of carriers, especially important through the narrower barriers formed on more heavily doped semiconductors, was discussed in many papers by Stratton and Padovani[16], and Rideout and Crowell[17] between 1966 and 1970. Perhaps the most complete treatment was given by Chang and Sze[18] who also included the effects of carrier

diffusion expected for barriers on lightly doped semiconductors.

The review paper by Rhoderick[19] showed that by 1970 a more accurate comparison of experiment and theory was possible because of the fabrication of diodes with near-ideal characteristics. This was the result of using the guard ring technique[20, 21] to minimise edge effects[22] and the formation of metal silicide-silicon junctions to remove the problems associated with an interfacial layer.

In the book 'Semiconductors and Semimetals'[23], Padovani gave a complete review of the mechanisms of carrier transport across metal-semiconductor barriers, particularly with regard to the thermionic field-emission and field-emission regimes. However, some of his predictions about the diffusion of carriers through the barrier region were revised by Crowell and Beguwala[24] who used different boundary conditions.

In 1973 Jäger and Kosak[25] experimentally demonstrated the importance of minority carrier effects at high forward current densities. Green and Shewchun[26] used a numerical method to solve the two carrier problem including recombination with the same boundary conditions as the thermionic-diffusion model of Crowell and Sze[15]. Using different boundary conditions, Demoulin and van de Wiele[27] presented an analytical solution of the same problem, whilst Card and Rhoderick[28] showed that the influence of minority carriers would be enhanced by the presence of an interfacial layer.

Of particular relevance to the present work are those papers concerned with titanium-silicon barriers and those which deal with contributions to the diode ideality factor or 'n value' and its variation as a function of the external bias voltage applied across the barrier. Atalla[29] first mentioned the use of titanium as a barrier metal. Zettler and Cowley[21] used several metals, including titanium in guard ring devices, and Cowley[30] later analysed the behaviour of titanium diodes on both n and p-type silicon in terms of the thermionic-emission

model of current transport. However, Cowley did not fabricate devices on high resistivity silicon. Saltich[31] measured barrier heights on n-type silicon of various impurity concentrations, and Saltich and Terry[32] fabricated titanium diodes on both n and p-type silicon, and showed that the barrier height was very dependent on the presence of an interfacial oxide layer. Burton, Portnoy and Leedy[33] used an unusual fabrication technique which gave anomalous results with several contact metals including titanium. Diodes fabricated by the Plessey Company[34] had characteristics which, for the most part, could be explained in terms of the thermionic-emission theory although there were some unresolved anomalies.

Contributions to the diode 'n value' come from image force lowering[15], edge effects[22], the influence of an interfacial layer[35], carrier recombination in the barrier[22], diffusion effects reducing the current below that expected from thermionic emission[24], and, for diodes on heavily doped silicon, from the influence of tunnelling[18, 36]. Demoulin and van de Wiele suggested that minority carrier injection would reduce the apparent n value.

1.3 SCOPE OF THE PRESENT WORK

The work described in this thesis includes the measurement of the barrier height of titanium on phosphorus doped n-type silicon of impurity concentration between 2×10^{20} m^{-3} and 3×10^{21} m^{-3}. The accuracy of the barrier height determination from the current-voltage characteristics is estimated as $\pm$ 5 mV with a total range over all the diodes measured of 25 mV. Although Saltich[31] investigated the barrier height over a similar range of impurity concentration, he used the capacitance-voltage characteristics to determine the barrier height and quoted the accuracy of his results as $\pm$ 20 mV with barrier height values ranging over 60 mV.

A particular feature of the present work is the detailed investigation of the theoretical contributions to the diode ideality factor or n value. Most of the mechanisms contributing to non-ideality are strongly dependent upon the applied voltage and the impurity concentration in the silicon. The experimental results reported here show that it is possible to deduce which mechanisms are dominant by studying the voltage and impurity concentration dependence of the n value.

For most of the diodes measured in this work, the current-voltage characteristics are well described by the thermionic-diffusion model of current transport with the addition of image force lowering of the barrier height. The formulation of thermionic-diffusion theory used in this work is very similar to that given by Crowell and Beguwala[24]. From the measurements, which extended to current densities as high as 4×10^5 Am^{-2}, deductions are made about the regions of applicability of the thermionic-emission and thermionic-diffusion models. The previous work by Cowley[30] on titanium barriers used a maximum current density of the same order, but his measurements were confined to silicon of impurity concentration greater than 5×10^{21} m^{-3}.

1.4 IMPORTANCE OF TITANIUM CONTACTS IN MICROELECTRONIC DEVICES

The traditional metal for the formation of contacts and interconnections on silicon integrated circuits is aluminium, which has a high conductivity and good adhesion to the silicon dioxide surface. However, two defects of the aluminium metallisation system are electromigration, and the formation of etch pits when aluminium diffuses into silicon[76]. These problems are overcome in modern high performance integrated circuits by using a barrier metal, such as titanium, between the silicon and the aluminium[77,34]. Titanium is also used in the high reliability beam lead process[78] because of

its good adhesion to silicon dioxide and silicon nitride.

The relatively low barrier height of titanium n-type silicon diodes has led to their consideration as power rectifiers, because they have a lower forward voltage, at a given current density, than most other metal contacts .

CHAPTER 2

THEORY OF THE METAL SEMICONDUCTOR BARRIER

This chapter will discuss the physical model of the metal n-type semiconductor barrier with particular reference to the processes determining the current-voltage characteristics. The theoretical basis for methods of measuring the barrier height and other parameters of the model will be presented.

2.1 FORMATION OF THE SCHOTTKY BARRIER

2.1.1 Ideal Case

The formation of the electrostatic barrier between the metal and the n-type semiconductor can be visualised as follows. When the metal and the semiconductor are electrically neutral and isolated, the energy of an electron at rest outside either solid will be equal to the vacuum level shown in Figure 1a where E_{FS} and E_{FM} represent the equilibrium energy levels inside the semiconductor and metal respectively. When the metal and semiconductor are connected electrically by an external circuit, electrons flow from the semiconductor to the metal until electronic equilibrium is reached when the Fermi levels E_{FS} and E_{FM} are equal. The metal has a net negative charge and the semiconductor has a net positive charge so that there is an electric field in the gap between them, Figure 1b. As the gap is reduced, the charges collect at the surface and, in the case of the n-type semiconductor, the positive charge consists of a layer of uncompensated donor ions which has a thickness related to the doping density and is much thicker than the corresponding layer of negative charge in the metal. As the gap δ decreases the space charge layer in the semiconductor builds up, and the bands are bent

as shown, Figure 1c, so that eventually the majority of the potential difference appears across the space charge region rather than across the gap. If δ is of the order of 1 nm then the gap is essentially transparent to electrons which can tunnel through. For the ideal contact when the gap disappears (Figure 1d) the barrier height ϕ_B is given by $\phi_B = (\phi_M - \chi_S)$ where ϕ_M and χ_S are the metal work function and semiconductor electron affinity as shown in Figure 1a.

2.1.2 Barrier With Surface States

Experimentally it is found that the barrier height ϕ_B can be almost independent of the metal, especially on a freshly cleaved semiconductor surface. In this case the surface states arising from the termination of the semiconductor lattice play a major part in determining the barrier height. Figure 2a shows a semiconductor surface with surface states which are filled up to a level ϕ_{SS} by electrons moving in from the conduction band, causing a depletion region, band bending, and a built in barrier even without the presence of a metal. In this case when the metal and the semiconductor are connected, the Fermi level of the semiconductor must fall relative to that of the metal by an amount equal to $(\phi_M - \chi_s - qV_F)$ as before, but if the density of surface states is high enough to accommodate the additional charge without appreciably altering the occupation level ϕ_{SS}, then the space charge in the depletion region will be largely unaffected. Thus the barrier height will be a property of the semiconductor surface and independent of the metal work function.

In practice the conditions at the surface will be intermediate between the two extreme cases and the barrier height can be expressed in a form such as [37].

$$\phi_B = \alpha(\phi_M - \chi_S) + (1 - \alpha)(E_g - \phi_o) \quad \ldots\ldots (1)$$

Where E_g is the semiconductor energy gap and ϕ_o is the value of ϕ_{SS}

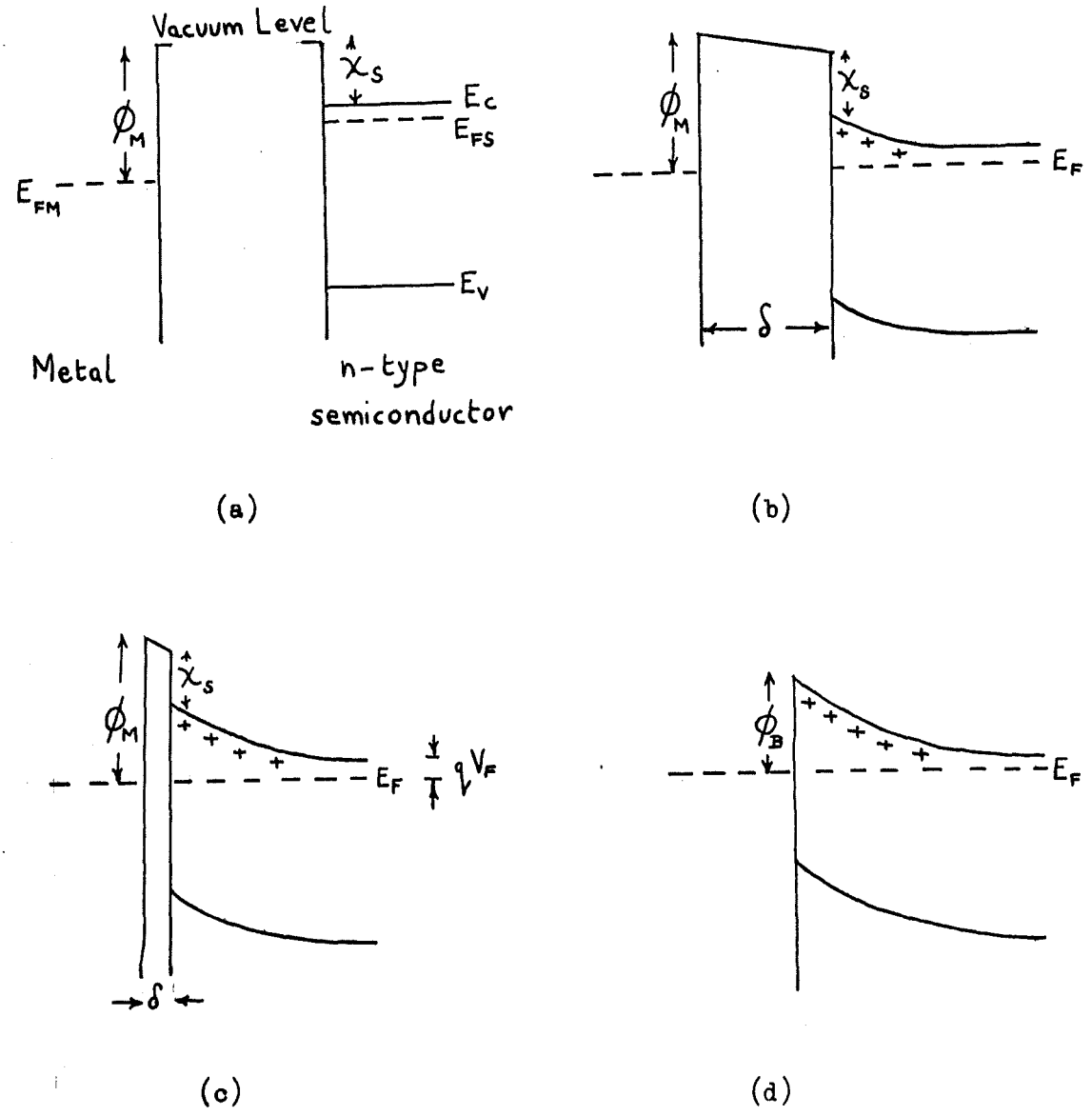


Figure 1 Electron energy levels in the metal and semiconductor during the formation of the barrier.

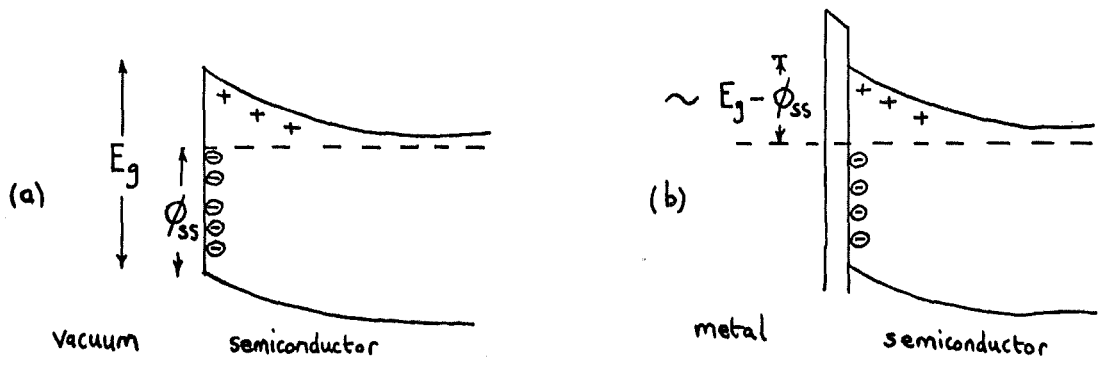


Figure 2 The effect of semiconductor surface states on the formation of the barrier.

which would make the semiconductor surface neutral. In the case where the metal and semiconductor are separated by a thin layer of oxide, thickness δ, permittivity ϵ_{ox} and the depletion layer space charge is much less than the charge in the surface states, then

$$\alpha = \frac{\epsilon_{ox}}{\epsilon_{ox} + q\delta D_s} \qquad \ldots\ldots (2)$$

where D_S is the density of surface states per electron volt per unit area of surface.

2.1.3 Image Force Lowering of The Barrier

The variation in potential through the barrier has been considered as solely due to the semiconductor space charge (Figure 3a), and is given by the expression

$$V(x) = \frac{qN_D}{\epsilon_{si}}\left(\lambda x - x^2/2\right) - V_B \quad \text{for } x \geqslant 0 \qquad \ldots\ldots (3)$$

where V(x) is measured relative to the Fermi level, $\lambda = \left(\frac{2\epsilon_{si}(V_B - V_F)}{qN_D}\right)^{1/2}$ is the width of the depletion region, q is the magnitude of the electronic charge, N_D is the density of donor atoms in the semiconductor, ϵ_{si} is the permittivity of silicon, and V_F is the potential difference between the Fermi level and the bottom of the conduction band.

Expression (3) is obtained by solving Poisson's equation

$$-\frac{\partial^2 V}{\partial x^2} = \frac{\partial \mathcal{E}}{\partial x} = \rho/\epsilon_{si}$$

for the abrupt approximation to the charge distribution that

$$\rho = qN_D \text{ for } 0 < x < \lambda \quad \text{and} \quad \rho = 0 \text{ for } x > \lambda$$

where $\mathcal{E}$ is the electric field in the barrier. In fact there will be a region near $x = \lambda$ where the ionised donor atoms are partially compensated by mobile electrons, which is called the reserve layer where $0 < \rho < qN_D$ and it can be shown [46] that

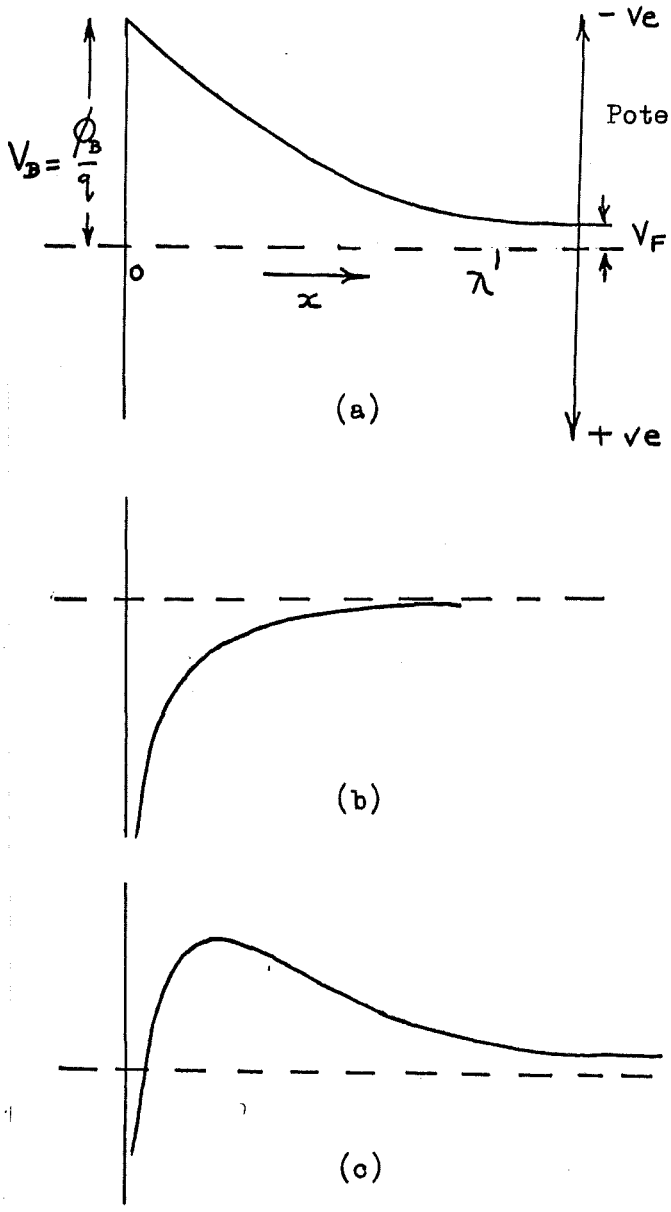


Figure 3
Potential variation through the barrier
(a) due to space charge in the semiconductor
(b) due to image force effect
(c) combined effect of (a) and (b)

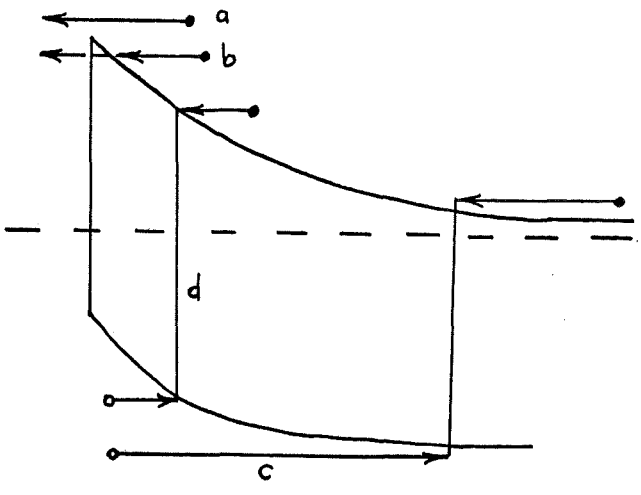


Figure 4
Conduction mechanisms through a Schottky barrier.
(a) Emission.
(b) Tunnelling.
(c) Minority carrier injection.
(d) Recombination and generation.

its effect is to alter the bracketed term in the expression for λ to $(V_B - V_F - kT/q)$ where k is Boltzmann's constant and T is the absolute temperature.

However, when an electron travels through the barrier and approaches the conducting plane of the metal, it experiences an electrostatic field (in addition to the barrier field already discussed) as if there were an equal and opposite charge located at the mirror image point, considering the plane of the metal semiconductor junction as the mirror. The attractive force experienced by the electron is given by $F = \frac{-q^2}{4\pi(2x)^2 \epsilon_{si}}$ which gives an additional contribution to the potential of $V = \frac{q^2}{16\pi \epsilon_{si} x}$ shown in Figure 3b.

The sum of these two potential distributions is shown in Figure 3c and it can be shown [38] that the effect of the image force has been to lower the barrier by ΔV_B which is given by

$$\Delta V_B = \left\{ \frac{q^3 N_D (V_B - V_F - kT/q)}{8\pi^2 \epsilon_{si}^3} \right\}^{\frac{1}{4}} \quad \ldots\ldots (4)$$

at zero applied bias.

2.2 CURRENT TRANSPORT ACROSS THE BARRIER

2.2.1 Summary of Mechanisms

Figure 4 illustrates the most important conduction mechanisms for a Schottky barrier on n-type semiconductor.

(a) Flow of electrons with sufficient energy from the conduction band over the top of the barrier into the metal.

(b) Tunnelling of electrons (with insufficient energy for process (a)) through the barrier.

(c) Injection of holes from the semiconductor surface into the

neutral region (followed by recombination with electrons in the bulk semiconductor or at the ohmic back contact).

(d) Recombination or generation of electrons and holes within the depletion region.

Which of these mechanisms dominates the behaviour of the Schottky barrier will depend upon the semiconductor doping, the barrier height and other parameters resulting from the design and technology used to fabricate the diode. Mechanism (b) is generally insignificant at room temperature for semiconductors of doping density N_D less than 10^{23} m^{-3} and so to a large extent can be neglected for the present study where the maximum doping density is 3×10^{21} m^{-3}.

2.2.2 Flow of Electrons Over The Barrier

There are two possible processes limiting electron flow over the barrier. The diffusion theory [4, 5] suggests that the current is limited by the rate at which the electrons move through the depletion region by the processes of drift and diffusion. The thermionic emission theory[7] assumes that the current is limited by the supply of electrons with sufficient energy to be emitted over the barrier into the metal.

The influence of each limiting process will be determined by the degree of scattering of electrons by other mobile carriers, fixed donor ions, or phonons, as they pass through the depletion region. In the limiting case where the mean free path of electrons is greater than the thickness of the barrier, then the thermionic emission or diode theory will be valid.

2.2.3 Thermionic Emission Theory

The current-voltage (I - V) characteristic, as given by the diode theory, is[2]

$$I = A^* S T^2 \exp\left(-qV_B/kT\right)\left[\exp\left(qV/kT\right) - 1\right] \quad , \quad \ldots\ldots (5)$$

where A* is the Richardson constant and S is the diode area. Assuming the semiconductor has ellipsoidal constant energy surfaces in momentum space, the value of the Richardson constant A* is[39]

$$A^* = \left(\frac{4\pi q k^2}{h^3}\right) \sum (l^2 m_y m_z + m^2 m_z m_x + n^2 m_x m_y)^{\frac{1}{2}} \ldots\ldots (6)$$

where h is Planck's constant; l, m, and n are the direction cosines of the normal to the emitting plane relative to the principal axes of the ellipsoid; m_x m_y and m_z are the components of the effective mass tensor; and the summation has to include all energy surfaces participating in the emission process. This relation is derived from the conservation of electron transverse momentum.

Equation (5) is known as the 'ideal' diode characteristic and it is usual to compare the current-voltage predictions of other models by writing them in the form

$$I = Is \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \qquad \ldots\ldots (7)$$

and then calculating the value of the parameter n, which may be a function of applied voltage. In a similar fashion, when characterising practical diodes, it is usual to plot the logarithm of the forward current as a function of bias voltage and evaluate the 'n value' from the slope of the plot.

Equation (5) predicts that the reverse current will saturate to a constant value when $V \ll -\frac{kT}{q}$. However, the barrier height V_B is dependent upon the external bias through the mechanism of image force lowering. For reverse bias, equation (4) becomes

$$\Delta V_B = \left\{\frac{q^3 N_D \left(V_B - V_F - V - \frac{kT}{q}\right)}{8\pi^2 \epsilon_{si}^3}\right\}^{\frac{1}{4}} \qquad \ldots\ldots (8)$$

and the result is that the reverse current does not saturate but increases slowly for increasing reverse bias. Crowell and Sze[15] showed

that the effect of image force lowering in the forward direction can be included by writing the current-voltage characteristic in the form of equation (7) where the n value is a slowly varying function of the bias voltage

$$n - 1 = \frac{d V_B}{d V} \left[1 - \frac{dV_B}{d V} \right]^{-1} \quad \ldots\ldots (9)$$

In addition to the image force effect, there are other mechanisms causing barrier lowering, of which tunnel penetration of the top of the barrier, and surface state penetration of the barrier have been reviewed by Padovani[23] and the influence of an interfacial layer[37] was discussed in sub-section 2.1.2 . The apparent lowering of the barrier height caused by tunnel penetration of the top of the barrier can be expressed as

$$\Delta V_B = X_C \left[2N_D q \, (V_B - V_F - V - kT/q) / \epsilon_{si} \right]^{\frac{1}{2}} \quad \ldots\ldots (10)$$

where X_C is the tunnelling length.

Surface state penetration of the barrier results in a lowering of the barrier given by

$$\Delta V_B = d \, \mathcal{E}_{max} \, \ln(qNss / \epsilon_{si} \, \mathcal{E}_{max}) \quad \ldots\ldots (11)$$

where Nss is the surface state density, d is the penetration distance of the surface states and $\mathcal{E}_{max}$ is the surface electric field, which for an ideal Schottky barrier is given by [40]

$$\mathcal{E}_{max} = \left[2N_D q \, (V_B - V_F - V - kT/q) / \epsilon_{si} \right]^{\frac{1}{2}} \quad \ldots\ldots (12)$$

Comparison of equations (8), (10) and (11) shows that each barrier lowering mechanism has a different dependence upon electric

field and so, in principle, it should be possible to decide which mechanism is dominant by studying the reverse current-voltage characteristic.

2.2.4 Diffusion Theory

The expression for the current-voltage characteristic derived from the diffusion theory is given by[40]

$$I = \frac{Sq\, N_c\, D_n \left[\exp\left(qV/kT\right) - 1 \right]}{\int_0^{\lambda} \exp\left(-qV(x)/kT\right) dx} \qquad \ldots\ldots (13)$$

where N_c is the effective density of states in the conduction band and $V(x)$ is the potential measured between the conduction band and the Fermi level in the metal. The above relation is derived assuming that the Einstein relation[40] $D_n = \mu_n kT/q$ holds throughout the barrier, where D_n and μ_n are the diffusion coefficient and mobility for electrons. The interesting feature of expression (13) is that it shows that the current-voltage relation is sensitive to the shape of the barrier and the position of the quasi-Fermi level, because of the appearance of the term $V(x)$. Several treatments of diffusion theory [41, 42, 43] have discussed the effect of variation in the shape of the barrier but very few have questioned the assumptions made about the position of the quasi-Fermi level. The quasi-Fermi level is a hypothetical energy level which has the significance that, if inserted in the Fermi-Dirac distribution function

$$F(E) = \left[1 + \exp\left(\frac{E - E_F}{kT}\right) \right]^{-1}$$

it gives the correct concentration of electrons (e.g. $N_c\, F(E_c)$) even

though the system may not be in thermal equilibrium.

Rhoderick[19] has shown that the difference between the diffusion and thermionic emission theories can be more clearly understood by considering the behaviour of the quasi-Fermi level for electrons. Away from the junction, on either side, the quasi-Fermi level would be expected to coincide with the Fermi level in the metal or semiconductor, assuming negligible voltage drop across the bulk metal or semiconductor. The usual assumption made in treatments of the diffusion theory is that the quasi-Fermi level at the junction coincides with the metal Fermi level as shown in Figure 5. On this basis, the conduction electrons just inside the semiconductor are in equilibrium with those in the metal and their concentration does not change when bias is applied. The assumption for the thermionic-emission model is that the quasi-Fermi level remains flat through the junction and so the concentration of electrons at the top of the barrier does change with applied bias. However, the electrons which are emitted over the barrier are not in thermal equilibrium with the conduction electrons in the metal. These 'hot' electrons have a quasi-Fermi level higher than the Fermi level in the metal, but as they move into the metal they lose energy by collisions, so that eventually the quasi-Fermi level and the Fermi level coincide.

Returning to the expression for the current-voltage characteristic given by equation (13), it is possible to evaluate the integral if the quasi-Fermi level at the interface is assumed coincident with the metal Fermi level as discussed above, and if some form of potential distribution through the barrier is assumed. Using the potential distribution derived in sub-section 2.1.3

$$V(x) = \frac{qN_D}{\epsilon_{si}} \left(\mathcal{N} x - x^2/_2 \right) - V_B$$ and neglecting x^2 term

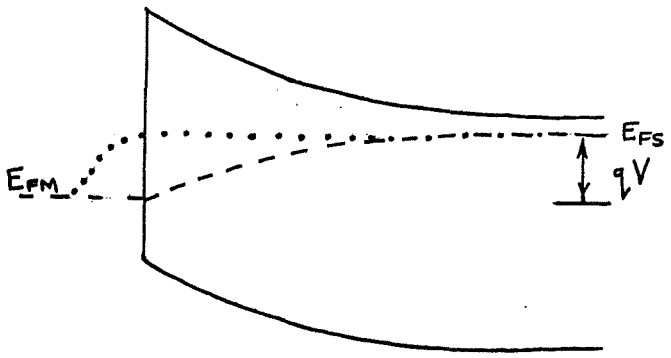


Figure 5
Energy level diagram for a Schottky barrier under forward bias V, showing position of quasi-Fermi level.
- - - - Diffusion theory
..... Thermionic emission theory.

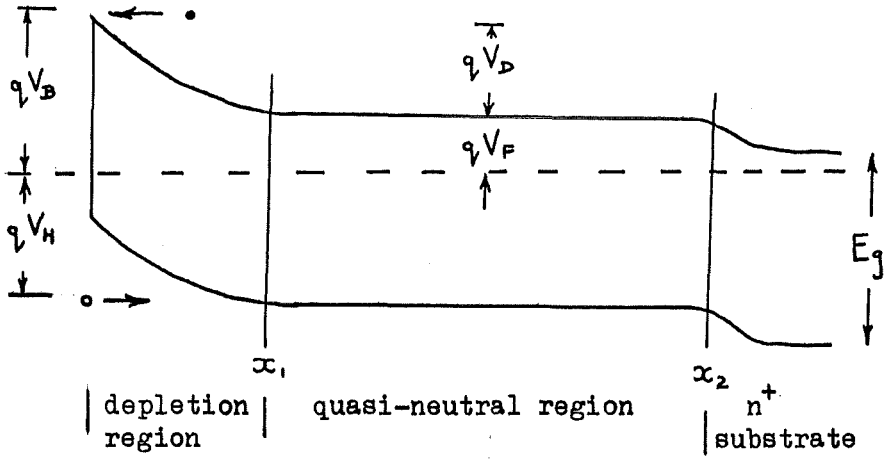


Figure 6 Energy band diagram for an epitaxial Schottky barrier showing hole and electron barrier heights.

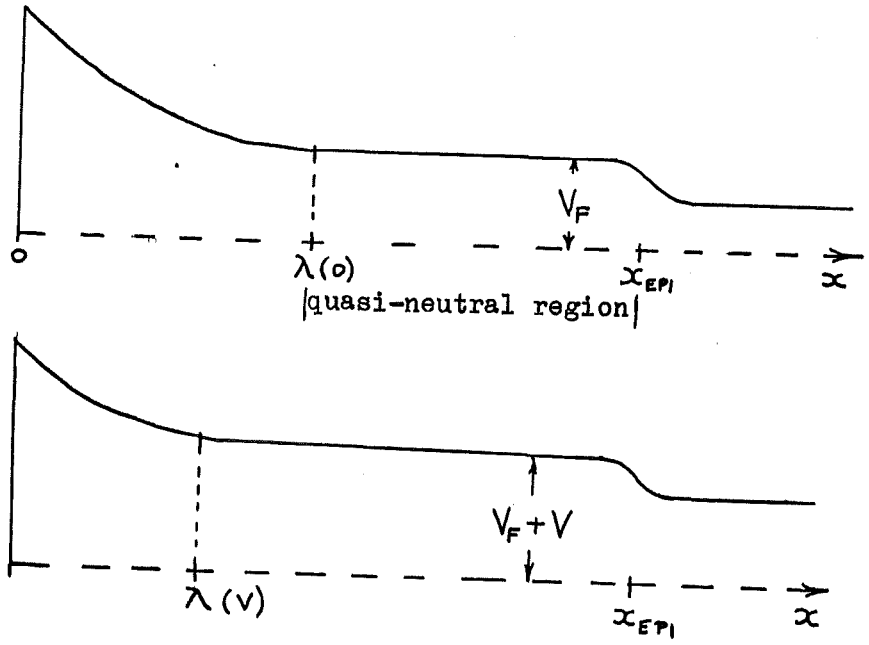


Figure 7 Dependence of quasi-neutral region width upon bias voltage.

equation (13) becomes

$$I = \frac{S q^2 D_n N_c}{kT}\left[\frac{q(V_D - V)\,4N_D}{\epsilon_{Si}}\right]^{1/2} \exp\left(\frac{-qV_B}{kT}\right)\left\{\frac{\exp\left(\frac{qV}{kT}\right) - 1}{1 - \exp\left[\frac{-2q(V_D - V)}{kT}\right]}\right\} \quad \ldots\ldots(14)$$

where $V_D = V_B - V_F - kT/q$. For reverse voltages and small forward voltages $V_D - V \gg kT/q$ and so the exponential term in the denominator can be neglected and equation (14) reduces to

$$I = \frac{S q^2 D_n N_c}{kT}\left[\frac{q(V_D - V)\,4N_D}{\epsilon_{Si}}\right]^{1/2} \exp\left(\frac{-qV_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad \ldots\ldots(15)$$

2.2.5 Thermionic-Diffusion Theory

A synthesis of the thermionic emission and diffusion approaches can be made by using an alternative boundary condition at the metal-semiconductor interface which does not involve assumptions about the position of the electron quasi-Fermi level[9, 24]. A detailed treatment of this approach is given in Appendix A but the main results are presented here.

The current-voltage characteristic is expressed in the form

$$I = \frac{S q N_c v_c}{1 + v_c/v_d} \exp\left(\frac{-qV_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad \ldots\ldots(16)$$

where v_c is an effective collection velocity for electrons reaching the top of the barrier, v_d is the effective diffusion velocity related to the Debye diffusion velocity v_D by $v_d = \frac{v_D}{D(\beta^{1/2})}$ where D is the Dawson function[50, 51] and β is the band bending in units of kT/q.

$$\beta = \frac{q}{kT}\left(V_B - V_F - kT/q - V\right) \qquad \text{(see Addendum)}$$

For high values of β and heavily doped silicon, $v_d \gg v_c$ and equation (16) reduces to the form of equation (5) of the thermionic emission theory if v_c has a value $v_c = \frac{A^* T^2}{q N_c}$. However, consideration of quantum mechanical tunnelling and phonon scattering of electrons in the barrier region suggests that this value of v_c is an upper limit. Image force lowering of the barrier can be included by replacing V_B in equation (16) by the term $(V_B - \Delta V_B)$.

If the current-voltage equation is written in the form

$$I = I_s \exp\left(qV/nkT\right)\left[1 - \exp\left(-qV/kT\right)\right] \qquad \ldots\ldots(16a)$$

it is shown in Appendix A that over a limited range of voltage, I_s can be considered constant and the parameter n has a value given by

$$\frac{1}{n} = \frac{\delta_v + 0.5\beta^{-1/2}}{\delta_v + D(\beta^{1/2})} - \frac{1}{4}\left[\frac{q^3 N_D}{8\pi^2 \epsilon_{Si}^3}\right]^{1/4}\left(\frac{kT\beta}{q}\right)^{-3/4} \qquad \ldots\ldots(17)$$

where $\delta_v = v_D/v_c$ as defined in Appendix A.

2.2.6 Hole Injection

The Schottky barrier current is mainly carried by electrons because (as shown in Figure 6) the effective barrier for electrons is $q V_D = q V_B - q V_F$ whereas the effective barrier for holes is $q V_H = E_g - q V_F$ and in general $q V_B < E_g$.

At high current density, a voltage develops across the resistance of the quasi-neutral part of the epitaxial layer. This increases the minority carrier injection ratio γ (ratio of minority current to total current) because the diffusion of holes across the quasi-neutral region is aided by the electric field which has developed in this region.

For the low injection case, before the drift component of the hole current becomes comparable with the diffusion term, the injection ratio γ is given by[13]

$$\gamma = \frac{J_p}{J_n + J_p} \approx \frac{J_p}{J_n} = \frac{q n_i^2 D_p}{N_D L_p A^* T^2 \exp\left(-\frac{qV_B}{kT}\right)} = \frac{q n_i^2 D_p}{N_D L_p J_s} \quad \ldots\ldots (17)$$

where D_p and L_p are the hole diffusion constant and diffusion length respectively, and n_i is the intrinsic carrier concentration.

At the other extreme when the drift component of the hole current dominates the diffusion term

$$\gamma \approx \frac{J_p}{J_n} = \frac{n_i^2}{N_D^2} \left(\frac{\mu_p}{\mu_n}\right) \frac{J}{J_s} \quad \ldots\ldots (18)$$

The density of holes in the epitaxial region at x_1 is given by $p(x_1) = \frac{n_i^2}{N_D} \frac{J}{J_S}$ if it can be assumed that the hole concentration at the interface is constant, $p(0) = \frac{n_i^2}{N_D} \exp\left(\frac{qV_D}{kT}\right)$ and the quasi-Fermi level for holes is constant through the depletion region. The concentration of holes elsewhere through the epitaxial region depends very much upon the rate of recombination of holes in the bulk and at the epitaxial layer-substrate boundary. A recombining interface at x_2 would require the excess hole concentration to be zero there, while a reflecting boundary requires the minority carrier current to be zero at x_2. The reflecting boundary condition is often taken as an approximation for an n - n^+ epitaxial boundary at low currents. In the limiting case of a perfectly reflecting interface and a bulk lifetime of infinity, the injection ratio drops to zero and the distribution of holes through the epitaxial region is given by

$$p(x) = \frac{n_i^2 J}{N_D J_s} \exp\left[\frac{J(x - x_1)}{q N_D D_n}\right] \quad \ldots\ldots (19)$$

Recent work[28] has shown that the injection ratio can be considerably increased by the influence of a thin interfacial oxide layer. When a voltage is applied to the junction, part of the voltage can appear across the interfacial layer which has the effect of lowering the effective barrier height for holes. If the interfacial layer is thin enough so that the holes can tunnel through, then the hole injection current will increase at the expense of the electron current. Quantitative calculations are difficult but it has been shown experimentally that although the effect is almost negligible for an oxide of thickness δ = 1 nm, it increases dramatically above 1.7nm so that an oxide of thickness δ = 2.8nm can increase γ by a factor of upto 10^3.

2.2.7 Generation and Recombination Currents

Under reverse bias, any hole electron pairs generated in the depletion region will be swept out by the field and contribute to the generation current which is given by[22]

$$I_{gen} = \frac{q n_i \lambda S}{\tau} \qquad \ldots\ldots (20)$$

where τ is the lifetime within the depletion region, and the only voltage dependence is contained in the depletion region width λ so that

$$I_{gen} \propto \left(V_B - V_F - V - {}^{kT}/_{q}\right)^{1/2} \qquad \ldots\ldots (21)$$

As the reverse bias increases, the depletion region widens and the generation current increases. The temperature variation of the generation current follows n_i, the intrinsic carrier concentration $n_i \propto \exp\left({}^{-E_g}/_{2kT}\right)$, and so when the temperature dependence of the reverse current is plotted, if an activation energy of $E_{g/2}$ is found, it suggests that the generation current is dominant. However, for diodes with low barrier height V_B and long lifetime τ, the thermionic

emission current generally dominates the current-voltage characteristics.

In the forward direction, holes and electrons can recombine in the depletion region without needing to cross the whole barrier. This recombination current can be expressed as

$$I_{rec} = \frac{q n_i \lambda S}{\tau} \exp\left(qV/2kT\right) \qquad \ldots\ldots (22)$$

for forward bias greater than $3kT/q$. If the recombination current is dominant then the temperature dependence of the forward current will have an activation energy close to $(E_g - qV)/2$. If the current-voltage relation is written as equation (7), then when recombination currents are dominant, an n value of 2 will be found, whereas pure thermionic emission gives an n value of unity.

2.2.8 The Influence of an Interfacial Layer

When a metal is deposited on chemically cleaned silicon, a thin interfacial layer of oxide generally exists between the two[44,45]. Although this prevents intimate contact, it is usually so thin ($\sim$ 1nm) that carriers can tunnel through it freely. When the voltage across the junction is changed, a small part of the change will appear across the film with the result that the change in current flowing will be smaller than that without the presence of the interfacial layer. Hence the current-voltage characteristic will increase more slowly than exp (qV/kT). If the interfacial layer is so thin that the occupation of the surface states is determined by the position of the metal Fermi level, then the current can be expressed in the form of equation (7) where n has a value[15,35]

$$n = 1 + \frac{\delta \epsilon_{si}}{\lambda(\epsilon_{ox} + q\delta D_s)} \qquad \ldots\ldots (23)$$

δ is the thickness of the oxide layer, ϵ_{ox} is the permittivity of the oxide and D_S is the density of surface states in equilibrium with the metal. The value of n varies slowly with bias because of the voltage dependence of λ, the depletion region width.

The effect of the interfacial layer on minority carrier injection has already been discussed in sub-section 2.2.6.

2.3 MEASUREMENT OF BARRIER HEIGHT

2.3.1 Current-Voltage Measurements

If the diode characteristics follow the thermionic emission model then from equation (5) and including barrier lowering, we can write

$$I = I_S\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \qquad \ldots\ldots (24)$$

where $$I_S = A^* S T^2 \exp\left(-q\frac{(V_B - \Delta V_B)}{kT}\right) \qquad \ldots\ldots (25)$$

Using a theoretical value for A^* we can then calculate $(V_B - \Delta V_B)$ from I_S. An alternative method is to measure the temperature variation of I_S, then plot $\ln (I_S/T^2)$ against $1/T$ and deduce $(V_B - \Delta V_B)$ from the slope. Although this technique does not require the value of A^* to be known, it does assume that thermionic emission is the dominant mechanism throughout the range of temperature measurement and that the barrier height is independent of temperature. In practice recombination or tunnelling currents soon become important as the temperature is lowered, and at higher temperatures the thermionic emission currents become so large that series resistance in the bulk silicon becomes important or diffusion may start to limit

the current.

If the diode behaves like the diffusion or thermionic-diffusion model, then the calculation of barrier height from the current-voltage measurements is not straight forward. If some shape for the potential barrier can be assumed, based on other evidence like capacitance-voltage measurements, then the voltage dependence of the saturation current (defined by equation (24)) can be calculated and the barrier height deduced.

The determination of which voltage dependent barrier lowering mechanisms are operative in the diode is of equal importance to the measurement of barrier height. The relative importance of the mechanisms already discussed (sub-section 2.2.2) can be found by a study of the reverse current-voltage characteristic. If the logarithm of the reverse current I_R is proportional to $(V_B - V_F - {}^{kT}/_{q} - V)^{\frac{1}{4}}$ then image force lowering is dominant. Tunnel penetration of the top of the barrier will cause $\ln(I_R) \propto (V_B - V_F - \frac{kT}{q} - V)^{1/2}$ Recombination generation currents will be proportional to $(V_B - V_F - {}^{kT}/_{q-V})^{\frac{1}{2}}$ and will be difficult to distinguish from the effects of surface state penetration of the barrier, whose dependence upon voltage is given in equations (11) and (12).

2.3.2 Capacitance-Voltage Measurements

Although the depletion region forms a barrier to the flow of mobile charge carriers, small changes in the applied voltage across the barrier cause changes in the charge stored in the depletion region, and the barrier can be treated as a voltage dependent capacitance. In the simplest case of a Schottky barrier where the charge density in the depletion region is constant and due only to the ionised donor atoms, the capacitance is given by $C = \frac{\epsilon_{Si} S}{\lambda}$ where λ is the

depletion region width given by

$$\lambda = \left(\frac{2 \epsilon_{Si} (V_B - V_F - kT/q - V)}{q N_D} \right)^{1/2}$$

Hence

$$\frac{1}{C^2} = \frac{2}{q N_D \epsilon_{Si} S^2} (V_B - V_F - kT/q - V) \qquad \ldots\ldots (26)$$

and from a plot of $1/C^2$ vs. bias V, the donor concentration N_D, and built in voltage $V_D = V_B - V_F - kT/q$ can be obtained from the slope, and intercept on the abscissa respectively. Unfortunately it is not always possible to obtain the linear plot expected from equation (26) and Goodman[46] has treated some deviations from the ideal case given above. Two of the most important causes of non-linearity are a non-uniform doping density N_D, and surface states whose charge varies with applied voltage. Smith and Rhoderick[47] have described a technique for measuring capacitance-voltage characteristics even in the presence of traps which would normally cause a non-linear plot.

2.3.3 Photoelectric Method

When monochromatic light is incident upon the barrier, either through a thin metal layer or from the back surface of the silicon, a photocurrent may be generated if the photon energy is great enough to generate excited electrons in the metal $h\nu > q V_B$, or great enough to generate hole electron pairs in the depletion region $h\nu > E_g$. By measuring the photocurrent as a function of wavelength, the barrier height can be found.

Although this method has been described as the most accurate and the most direct[40], it is also subject to subtle errors[48] if

trapped electrons are present or if photons with an energy much greater than the threshold are used. There is also some doubt as to whether the barrier height measured for the photoelectric process is the same as for the current transport process when no photons are present. For low barriers, even with no illumination the reverse current flowing is large and makes the detection of the photocurrent more difficult, so that this technique was not used in the present study.

2.4 ADDITIONAL BARRIER MODEL PARAMETERS

In order to predict the behaviour of a metal semiconductor diode accurately, not only is it necessary to have a model of the current transport mechanism, as discussed in section 2.2, and a value of the barrier height, but also several other parameters resulting from the practical fabrication of the diode structure, are needed.

The series resistance of the bulk silicon cannot be neglected at high current densities, although its effect may be very small on heavily doped silicon. To minimise its effect on lightly doped silicon, a thin epitaxial layer of the required resistivity is grown on the surface of a heavily doped substrate crystal. Because the width of the undepleted region of the epitaxy (or quasi-neutral region) is a function of voltage, the effective series resistance will be voltage dependent. Figure 7 demonstrates this effect. If $R_S(0)$ is the series resistance value at zero applied bias, then its value at an applied voltage V is given by

$$R_S(V) = R_S(0) \frac{(x_{EPI} - \lambda(V))}{(x_{EPI} - \lambda(0))} \qquad \ldots\ (27)$$

where x_{EPI} is the width of the epitaxial layer.

A second parameter which also becomes important at high current

densities is the thermal resistance of the diode, Θ. For steady state conditions, it is found experimentally that the diode temperature rises linearly as a function of power dissipated, at least up to 10 mW , such that

$$\Delta T = \Theta I V \qquad \text{.....(28)}$$

where $\Delta T = T - T_A$, is the temperature rise.

The thermal behaviour of the diode, including transient effects, is discussed in Appendix D. Knowledge of Θ allows the diode behaviour to be predicted to much higher current levels than is possible using an isothermal approximation.

CHAPTER 3

PREPARATION OF SPECIMENS

All processes during the preparation of the specimens were carried out using chemicals of Electronic Grade under conditions of high cleanliness, which have become commonplace in microelectronic device fabrication. It is not appropriate for this thesis to list all the plant and equipment used in the laboratory during the preparation of the specimens. However where any stage during the processing was considered critical, all relevant information will be given.

The preparation of specimens can be divided into the following headings:-

Silicon wafer preparation

Metal deposition and photoengraving

Post wafer processing

3.1 SILICON WAFER PREPARATION

The various wafers used in the investigation had a surface layers of epitaxially grown silicon of different thickness and electrical resistivity, all of which had a low crystalline defect density and required no mechanical or chemical polishing before use. The wafers were supplied by Texas Instruments, Bedford, except for two supplied by Plessey Company Limited, Allen Clark Research Centre, Towcester.

For fabrication of titanium and magnesium diodes, the silicon wafer preparation consisted solely of a cleaning procedure prior to metal evaporation directly onto the surface of the wafer. However, for aluminium diodes a guard ring structure[20, 21] was fabricated by the procedure below.

3.1.1 Silicon Wafer Cleaning

The purpose of the cleaning procedure was to remove organic and inorganic contamination from the surface of the wafer, and to minimise the thickness of the silicon dioxide layer[44, 45] formed on the surface of the wafer.

(a) Ultrasonically wash wafer in trichlorethylene for two minutes.

(b) Ultrasonically wash wafer in methanol for two minutes.

(c) Rinse wafer in de-ionised water (of resistivity greater than 10 Megohm cm.) and spin dry.

(d) Clean wafer in a mixture of one part concentrated H_2SO_4 and one part H_2O_2 for five minutes.

(e) Rinse wafer in de-ionised water for two minutes.

(f) Dip etch wafer in a mixture of six parts de-ionised water and one part of hydrofluoric acid.

(g) Rinse wafer in de-ionised water and spin dry.

At this stage the wafers were rapidly transferred to the vacuum evaporation system for the deposition of titanium or magnesium metals. Aluminium diodes required the formation of a p-type guard ring structure (Figure 8) in the n-type epitaxial layer and so further process stages were involved as detailed below.

3.1.2 Oxidation of Silicon

The purpose of the initial oxidation described here, was to form a mask on the surface of the n-type silicon wafer, against diffusion of a p-type impurity (boron).

Immediately after stage (g) of the cleaning procedure, the silicon wafers were loaded onto a quartz glass boat and pushed into the centre of a tube furnace at 1080°C (Figure 10). After 15 minutes oxidation in a dry oxygen atmosphere, steam was added to the gas flow through the tube to complete the growth of the silicon

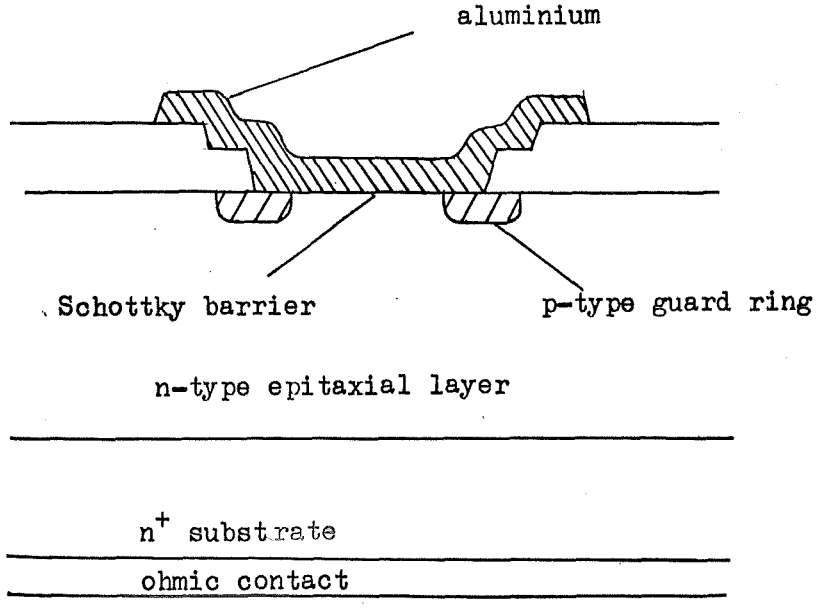
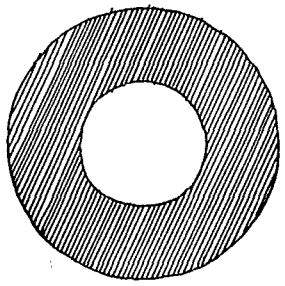
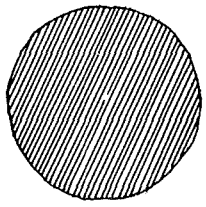


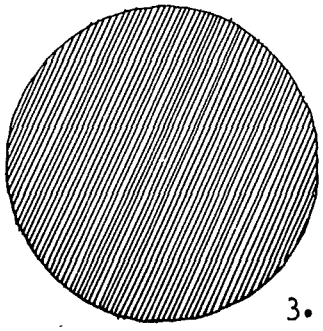
Figure 8 Guard ring structure (not to scale)



1. Oxide etching mask (Stage 3.1.3)



2. Oxide etching mask (Stage 3.1.5)



3. Metal etching mask (Stage 3.2.4)

Figure 9 Masking patterns(approximately x 200)

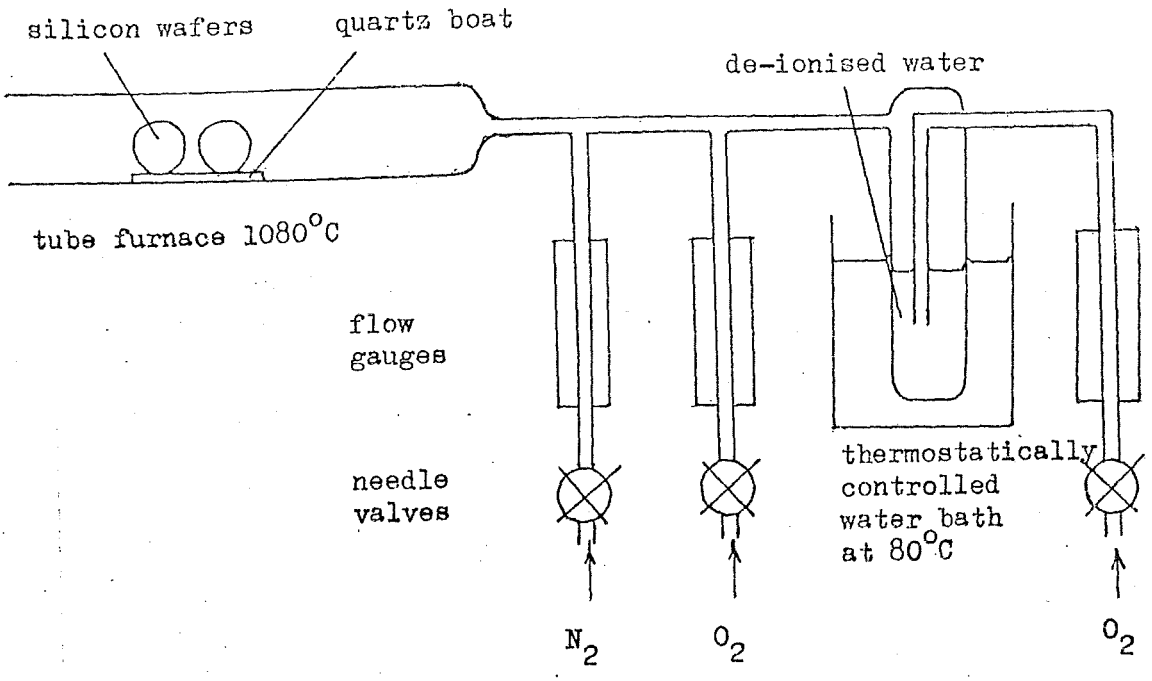


Figure 10 - Schematic of oxidation system

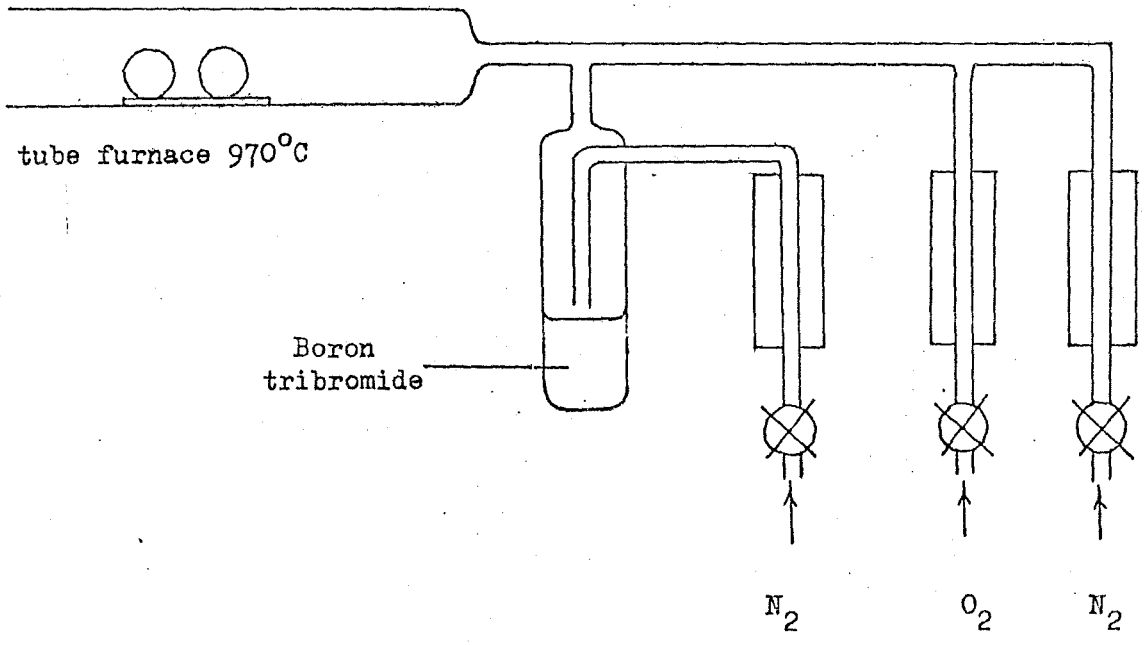


Figure 11 - Boron deposition system

dioxide to a thickness of 0.35 μm. Finally the gas flow was changed back to dry oxygen for five minutes to prepare the wafers for the photo-engraving stage, where a clean dry surface is essential for good adhesion of photo-resist[52].

3.1.3 Photo-engraving and Etching

Kodak Metal Etch Resist (KMER) was applied to the surface of the oxide covered wafers using a rotating vacuum chuck. After application of a few drops of KMER to the surface, the chuck was rapidly accelerated to 4000 r.p.m. which produced a 1 μm uniform coating. After drying the KMER layer on a hotplate at 90°C for 15 minutes, the wafer was exposed to ultra-violet light. This stage was carried out with the wafer firmly clamped to a masking pattern (Figure 9) on a Kodak high resolution glass plate using a Kullicke and Soffa model 686 mask aligner. The unexposed KMER was then washed off by applying the developing reagent and rinsing solvent from aerosol sprays. A 20 minute bake at 150°C completed the polymerisation of the exposed KMER so that it would protect the underlying oxide against the etch.

The unprotected oxide was then removed from the surface by immersing the wafer in buffered hydrofluoric acid at room temperature. This etch consisted of four parts of 40% NH_4F solution and one part of HF. After etching, the wafer was rinsed in de-ionised water and then the photoresist removed by two successive applications of stage (d) of the cleaning procedure. Stages (e) to (g) were carried out and the wafer was ready for impurity diffusion.

3.1.4 Impurity Diffusion

Figure 11 shows a schematic of the 970°C tube furnace system used to deposit the B_2O_3 glass on the surface of the wafer from which the boron would diffuse into the silicon lattice[53]. The glass was deposited all over the surface of the wafer. Where the silicon had

been exposed by the previous etching stage, the reaction

$$B_2O_3 + Si \longrightarrow SiO_2 + B$$

took place producing free boron which could diffuse into the lattice and become electrically active as a p-type impurity.

After removal of the wafers from the deposition furnace, the excess boron glass was removed from the surface by a two minute etch in 6 : 1 de-ionised water : HF.

The final stage of diffusion was a further oxidation stage to regrow oxide over the whole surface of the wafers and also, because of the high temperature involved, drive the boron impurity atoms further into the silicon lattice. This oxidation was carried out in a tube furnace at 1180°C, and after removal from this furnace, the wafers were ready for a second photoengraving stage to cut contact windows through the oxide to the silicon.

3.1.5 Second Photoengraving and Etching

The procedure used was exactly the same as that used in Section 3.1.3 except that the masking pattern appropriate for the etching of contact windows was used. After removal of the photoresist and cleaning, the wafers were then ready for transferring to the vacuum system for the evaporation of aluminium.

3.2 EVAPORATION OF METALS

Titanium was the principal metal under investigation but magnesium and aluminium Schottky barriers were also fabricated to enable a more general evaluation of the theories which were developed to explain the behaviour of the titanium diodes.

In the case of titanium and magnesium, a thin barrier film of about 0.1 μm of the metal was first evaporated with the aim of getting a film of high purity. A second evaporation of about 1 μm aluminium was made, to which aluminium wire could be bonded at

a later stage in the processing to facilitate evaluation of the devices.

The titanium was supplied in the form of 1 mm diameter wire of 99.9% purity from Koch Light. Magnesium wire of 1.5 mm diameter and 99.9% purity was supplied by B.D.H. The aluminium wire 2 mm diameter and of purity 99.998% was obtained from Johnson Matthey.

3.2.1 Evaporation Equipment

Two Edwards High Vacuum Coating Units, model 12 E 3, were used, each with a 12" diameter glass bell jar, liquid nitrogen trap, oil diffusion pump and rotary backing pump. Pressures during evaporation ranged from 10^{-6} to 10^{-5} torr.

Metal films were evaporated from tungsten filaments in a shuttered system, with substrate heating for the silicon wafers. Figure 12 shows a schematic of the jig, inside the bell jar, most of which was fabricated from stainless steel. Titanium and magnesium were evaporated in one system which had an additional heat shield round the filament to minimise heating and hence outgassing of the remainder of the bell jar system.

3.2.2 Evaporation Technique

The technique of evaporation was similar for all the metals. Prior to loading of the silicon wafers, and the metal charge, the system was pumped down and the filaments were outgassed by passing a current through them, in excess of that to be used during evaporation, for 30 seconds. Each metal charge was prepared avoiding direct handling and was ultrasonically cleaned in trichlorethylene, acetone, and de-ionised water followed by an appropriate metal etch to remove the surface layer. Silicon wafers were loaded after the preparation previously described and the vacuum system was pumped down with the minimum delay.

When the pressure reached 10^{-5} torr. the metal charge on the

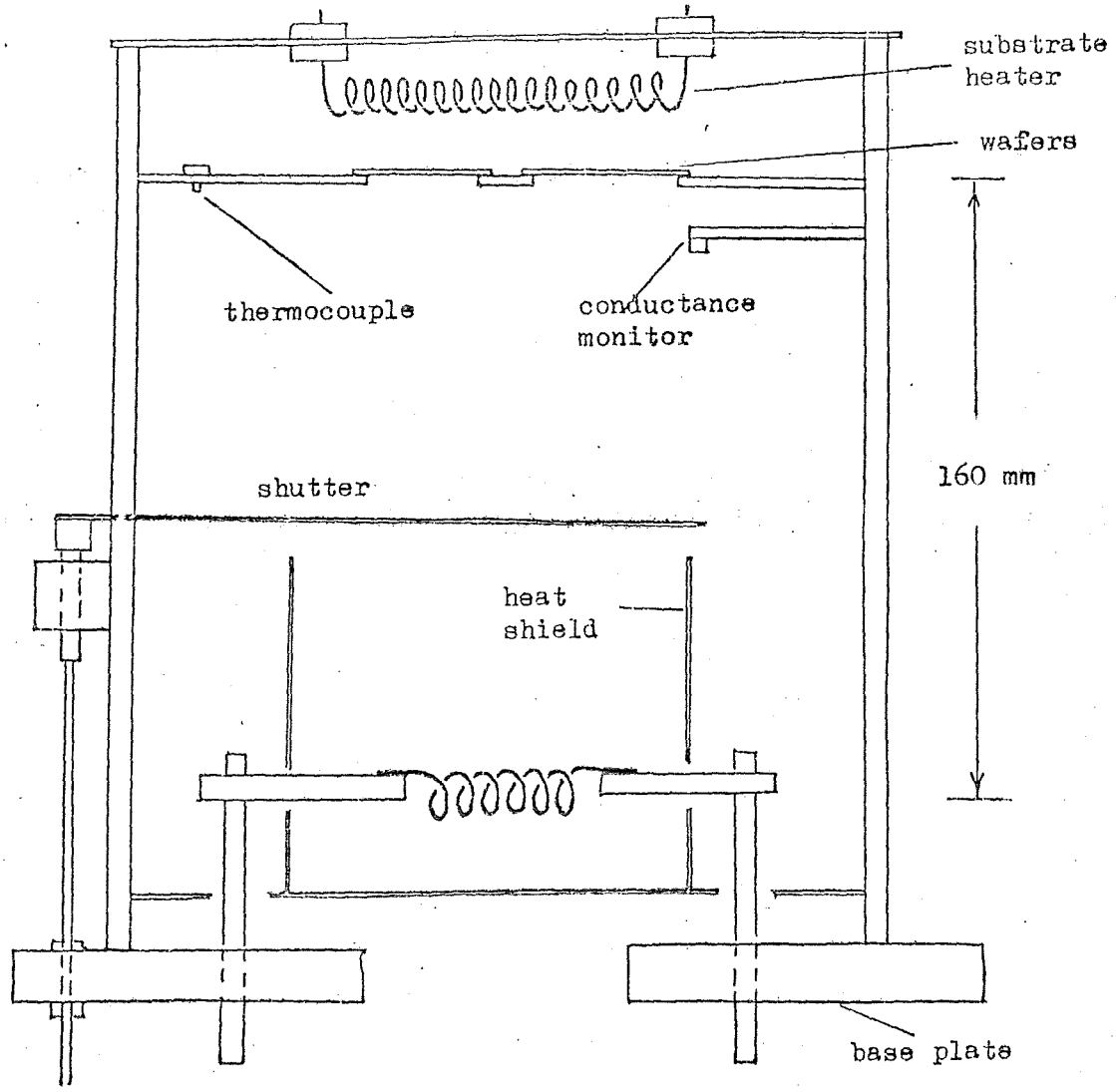


Figure 12 Schematic diagram of evaporation jig

filament was outgassed for 30 seconds at a current just below that needed to melt the charge. The rest of the vacuum system was outgassed by using the substrate heater to raise the temperature to 250°C.

The system was then allowed to cool and when the pressure stabilized below 10^{-5} torr. the metal charge was evaporated. Since freshly evaporated films of both titanium and magnesium act as excellent getters for residual gas, both these metals were evaporated slowly at first until the gettering action was detected by a fall in monitored pressure. The heating current was then raised and the shutter opened to deposit the film on the silicon wafers. However with aluminium, the filament current was raised to a high value immediately and as soon as the metal started to melt, the shutter was opened. After evaporation, the bell jar system was allowed to cool to near room temperature before the system was opened to air.

3.2.3 Film Evaluation

Film thickness, during evaporation, was monitored using an Electrotech Equipments Ltd. Film Monitor P 1001. This equipment gave a direct reading of the conductance across a glass slide positioned close to the silicon wafers inside the bell jar system. In order to convert conductance measurements into film thickness, a value of the sheet resistivity is required. The appropriate value is usually somewhat higher than the bulk resistivity because of film impurity or thin film scattering effects.[54]

After removal of the samples from the vacuum system, film thickness was measured using a multiple beam interference method.[55] This enabled the value of sheet resistivity of the deposited film to be compared with the bulk values reported in the literature. The equipment used to observe the interference pattern was a Leitz

Ortholux microscope with Multibeam Interference attachment and sodium vapour lamp. The schematic arrangement is shown in Figure 13 and the appearance of the fringe pattern in Figure 14. The thickness of the film t is given by

$$t = \frac{d}{D} \frac{\lambda}{2} \quad \text{where } \lambda = 589 \text{ nm for the sodium vapour lamp.}$$

Titanium films of between 34 nm and 136 nm were deposited with resistivity values between 69 and 79 $\mu\,\Omega$ cm. The bulk value of resistivity[56] is 43 $\mu\,\Omega$ cm but thin film values vary widely. Singh and Surplice[57] obtained films with resistivity between 100 and 170 $\mu\,\Omega$ cm for their films whereas Friebertshauser and McCamont[58] using a rapid evaporation technique obtained films with resistivity in the range 44.5 to 65.5 $\mu\,\Omega$ cm.

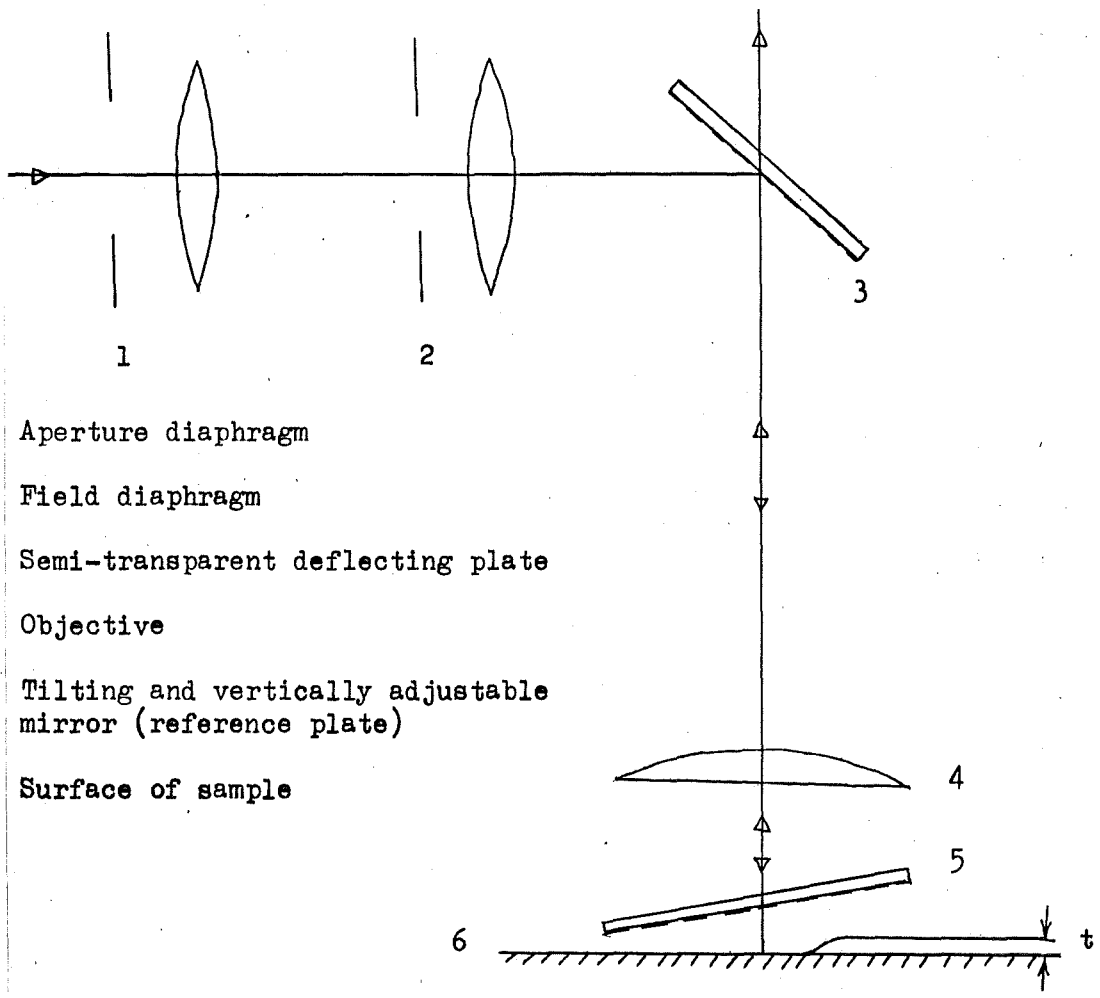
The magnesium films of between 70 nm and 200 nm thickness had resistivity values between 5.8 and 6.9 $\mu\,\Omega$ cm. These are to be compared with the bulk value of 4.4 $\mu\,\Omega$ cm[59].

The aluminium films were considerably thicker at 1.2 μm.

The substrate temperature, measured by the thermocouple shown in Figure 12, during the evaporation of aluminium onto silicon and titanium was 200°C. However during the evaporation of aluminium onto magnesium, the substrate was held at 100°C to prevent the formation of intermetallic compounds[59]. It is well known that metal films evaporated from tungsten filaments will contain traces of tungsten[54]. Examination of an evaporated film of titanium, using an electron microanalyser at the Plessey Company, Allen Clark Research Centre, failed to detect any tungsten. It was concluded that the tungsten concentration must be less than 1%, which was the sensitivity of the probe.

3.2.4 Metal Photo-engraving and Etching

The procedure used for selective etching of the metal to form circular areas of contact to the silicon was very similar to that



1. Aperture diaphragm
2. Field diaphragm
3. Semi-transparent deflecting plate
4. Objective
5. Tilting and vertically adjustable mirror (reference plate)
6. Surface of sample

Figure 13 Multibeam interference arrangement

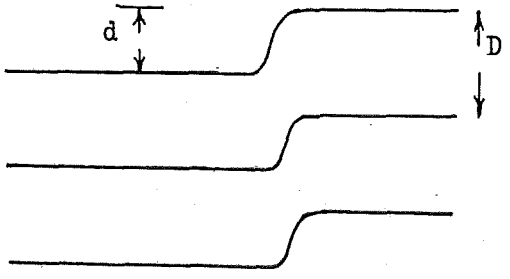


Figure 14 Appearance of fringes

described in section 3.1.3 for selective etching of silicon dioxide. Shipley AZ 1350 H photoresist was used to protect the metal during the etching stage.

For the fabrication of aluminium diodes, the following etch was used at 50°C and the etching time was about two minutes.

80 ml Phosphoric Acid

4 ml Nitric Acid

18 ml De-ionised Water

The overlay of aluminium on the titanium diodes was etched as above but once the etch had exposed the titanium it did not remove it. At this stage the wafers were rinsed in de-ionised water and transferred to the following mixture which etched away the unwanted titanium in about 30 seconds.

10 ml Hydrofluoric Acid

20 ml Hydrochloric Acid

60 ml Nitric Acid

400 ml De-ionised Water

A similar procedure was used to form the magnesium diodes with aluminium overlay. In this case the aluminium etch did remove the magnesium and so both metals could be defined in one etching stage.

In all cases, after etching the metal, the wafers were rinsed in de-ionised water and the photoresist removed with acetone.

3.3. POST WAFER PROCESSING

At this stage each silicon wafer surface was covered with a matrix array of circular metal contacts of various sizes, and to facilitate measurement and evaluation of individual diodes the following process sequence was carried out:-

3.3.1 Scribe and Break

Using a diamond tipped scribing tool, a regular array of lines, in two orthogonal directions, were cut into the surface of the silicon wafer which divided it into groups of six diodes. The silicon dust produced was blown clear, and the wafer was placed face down on a filter paper. By rolling a $\frac{3}{4}$" diameter copper pipe over the back of the wafer, the wafer was broken into 'chips', each of which had six diode contacts on the front surface. The chips were visually inspected for defects such as cracks or scratched metal and the satisfactory chips were bonded to gold plated header cans. (Figure 15)

3.3.2 Chip Bonding

The chips were attached to the metal headers by a eutectic bond between silicon and gold or using an adhesive resin. The eutectic bond required the formation of an alloy between the back face of the chip and the gold plating on the header. The header was placed in a heated jig at 400°C with a nitrogen jet blowing across the surface and the chip was placed on the header and 'scrubbed' into contact using glass rods to position the chip. When the formation of the alloy was observed, the bonded chip and header were removed to cool.

The attachment of chips by adhesive resin was used for the magnesium diodes which could not be heated above 200°C because of the possible formation of intermetallic compounds with the aluminium overlay. The method was also used for a series of titanium diodes to check if the high temperature used during eutectic bonding was altering the diode characteristics.

The epoxy adhesive used was Dupont 5504A silver epoxy which gave an electrically conductive bond. The curing cycle was 160°C for 16 hours.

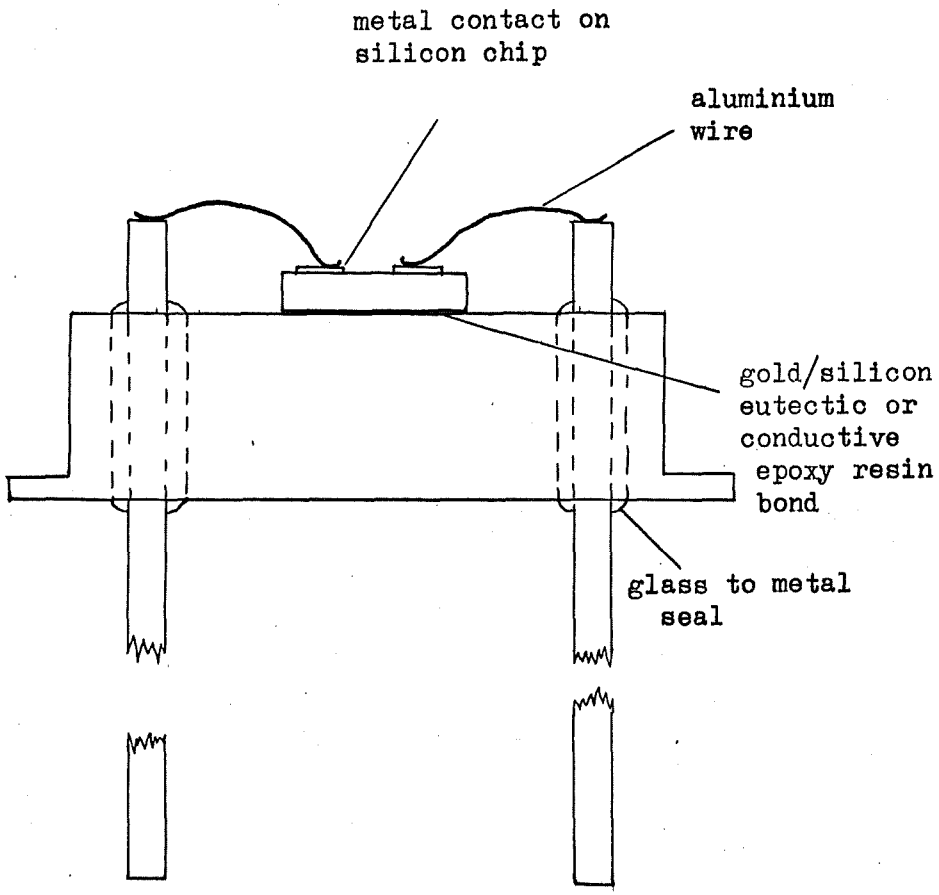


Figure 15 - Silicon chip attached to header

3.3.3 Wire Bonding

Aluminium wire of 25 μm diameter was bonded between each metal contact on the surface of the chip and the top of an adjacent post on the header. A Hugle Industries Inc. Model 1300 ultrasonic bonder was used so that the diodes were not subjected to a further heating cycle. A metal or opaque plastic cap was then fitted over the top of the header to provide mechanical protection for the diodes. The electrical characteristics of the diodes were measured by inserting the leads from the headers into the appropriate test jig.

CHAPTER 4

MEASUREMENT TECHNIQUES

This chapter describes the equipment and methods used to measure diode forward and reverse current-voltage characteristics, forward AC resistance, capacitance-voltage characteristics, activation energy plots (from current-temperature characteristics at fixed voltage), and thermal properties. The theoretical background to each method of characterising the diodes has already been given in Chapter 2. Presentation and discussion of the results is given in Chapter 5.

4.1 CURRENT-VOLTAGE MEASUREMENTS

All current-voltage measurements were made with the diode under test enclosed in a light-tight metal alloy box to avoid photoelectric generation of hole-electron pairs. At a very early stage in the measurements it was realised that the diode current was very sensitive to changes in ambient temperature. In order to minimise this effect the metal alloy box containing the diode was surrounded by a 50 mm thick layer of expanded polystyrene and the measurements were made in a thermostatically controlled room. With these precautions, a mercury in glass thermometer in contact with the alloy box indicated temperature variations of less than $\pm$ 0.1^{o}C during a series of measurements. Typical recordings of temperature fluctuations during electrical measurements are shown in Figure 16. Thus apart from any self heating effects at high current densities, the diode temperature variation would be expected to be within $\pm$ 0.1^{o}C of the mean recorded temperature for each set of measurements.

For diode currents greater than 10 μA the measuring equipment (listed in Table 1) was connected as shown in Figure 17. The expected accuracy of current and voltage measurements using this

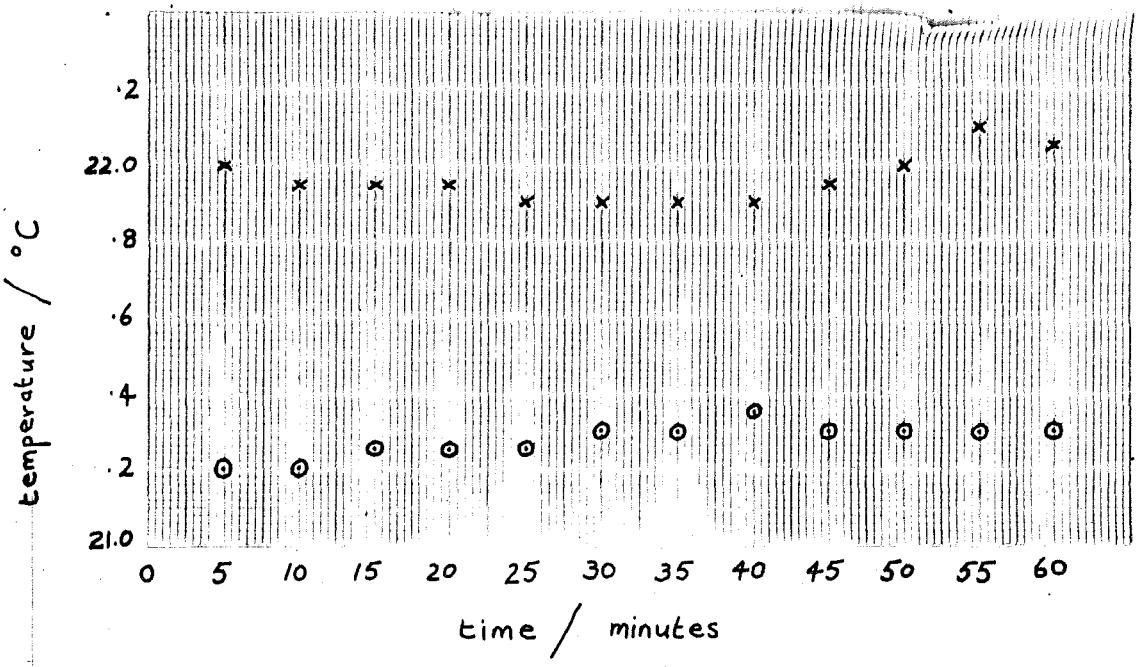


Figure 16 Typical temperature recordings during electrical measurements.

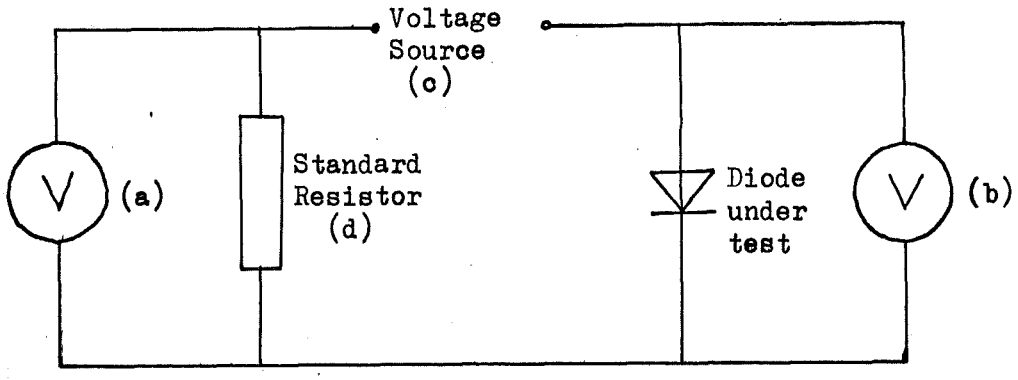


Figure 17 Schematic circuit for current-voltage measurements $> 10\mu A$.

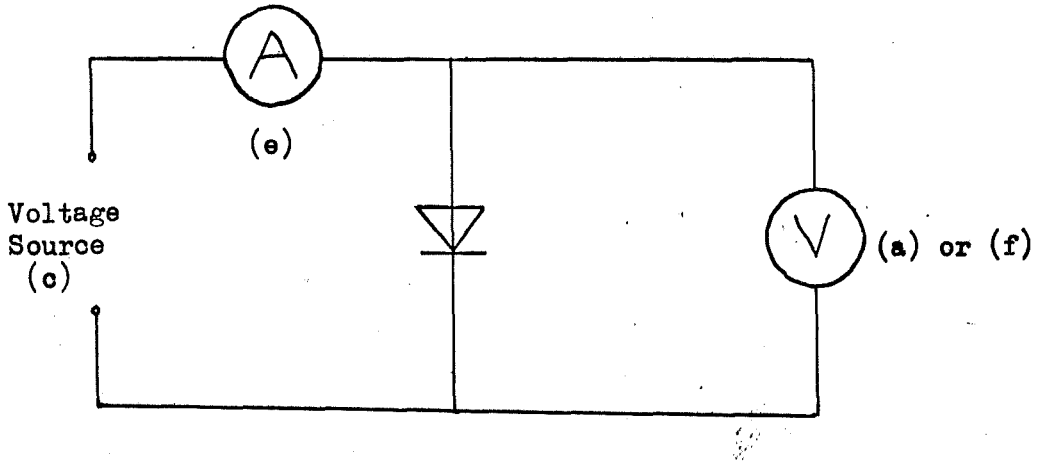


Figure 18 Schematic circuit for current-voltage measurements $< 10\mu A$.

TABLE 1

Measurement Equipment

Equipment	Type	Specified Accuracy
(a) Voltmeter	Solartron Digital Voltmeter LM 1450	± 0.05% of reading ± 0.05% of full scale
(b) Voltmeter	Solartron Digital Voltmeter LM 1420	± 0.05% of range ± 1 digit
(c) Voltage Source < 300 mV > 300 mV	Stabilised Supply Circuit (Figure 19) Solartron Transistor Power Supply Type AS 757.2	
(d) Standard Resistor	100 H. Tinsley & Co. Ltd. Type 1659	Maximum Error 0.02% at 20°C
(e) Electrometer	Keithley Type 610C	± 2% of full scale
(f) Electrometer	Vibron Type 33B2	± 1% of reading ± 0.2 mV
(g) Universal Bridge	Wayne Kerr B224	± 0.1% of reading
(h) Phase Sensitive Detector	Brookdeal FL 355 and MS 320	
(j) Oscillator	Solartron Signal Generator CO 546	
(k) Capacitance Bridge	Boonton 72A (1 MHz)	± 0.5% of full scale ± 1% of reading
(l) Capacitance Bridge	Boonton 75D (1 MHz)	±(0.25% +(10^3G + 0.5)pF) x1 range ±(0.25% +(10^3G + 0.05)pF) x0.1 range

arrangement was usually better than ± 0.1% but in all cases better than ± 0.5%. During use, the digital voltmeters were calibrated using their own internal voltage standards. After the measurements, these were then checked against a Muirhead Standard Cell type D402 which was specified as being calibrated to within ± 0.002% by the manufacturers.

For diode currents below 10 μA a different arrangement was used as shown in Figure 18. To minimise spurious leakage currents, P.T.F.E. insulation was used in the construction both of the jig to hold the diode under test and also in the stabilised voltage source. Before assembly, all insulating components were washed in non-polar solvents and handled with rubber gloves to avoid ionic contamination. Measurements made with the diode disconnected, suggested that the total leakage path had an impedance greater than $10^{10}\Omega$. For this arrangement the accuracy was limited by the Keithley Electrometer at ± 2%.

The stabilised voltage source (Figure 19) was developed from published circuits[60], to give a continously variable output between zero and 300 mV. Two low temperature coefficient zener diodes provide a reference voltage, and a feedback loop using a high gain operational amplifier ensures that the output is held at the reference voltage for a very large range of loads. Short circuit overload protection is provided by the current limiting transistor T_3. The circuit proved able to supply a voltage constant to within 1 part in 1000 over a period of several hours, much longer than that needed to complete a set of measurements.

4.2 AC RESISTANCE MEASUREMENTS

The presence of series resistance in a practical diode makes determination of the diode behaviour from current-voltage measurements more difficult especially at high currents. The measurements of diode AC resistance can then be very useful in providing additional information. The full theoretical expression for the diode AC resistance $R_{AC} = \frac{d V_m}{d I_m}$

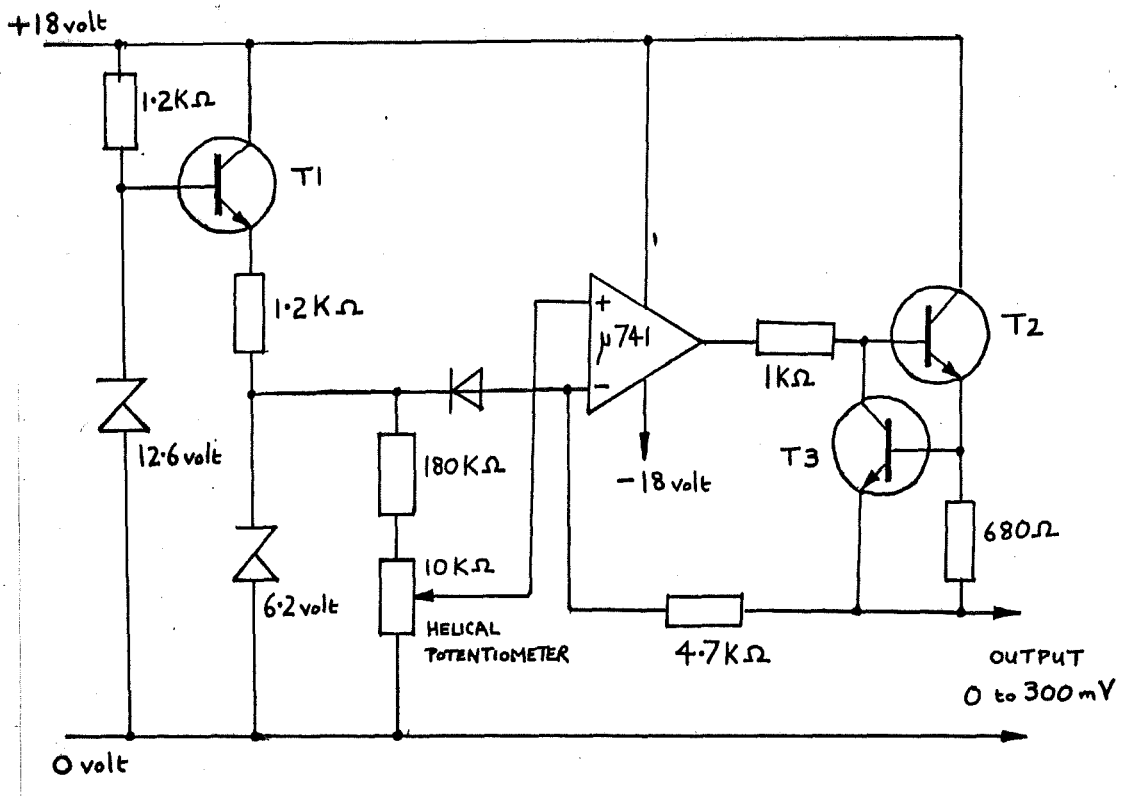


Figure 19 Circuit diagram of the stabilised voltage source.

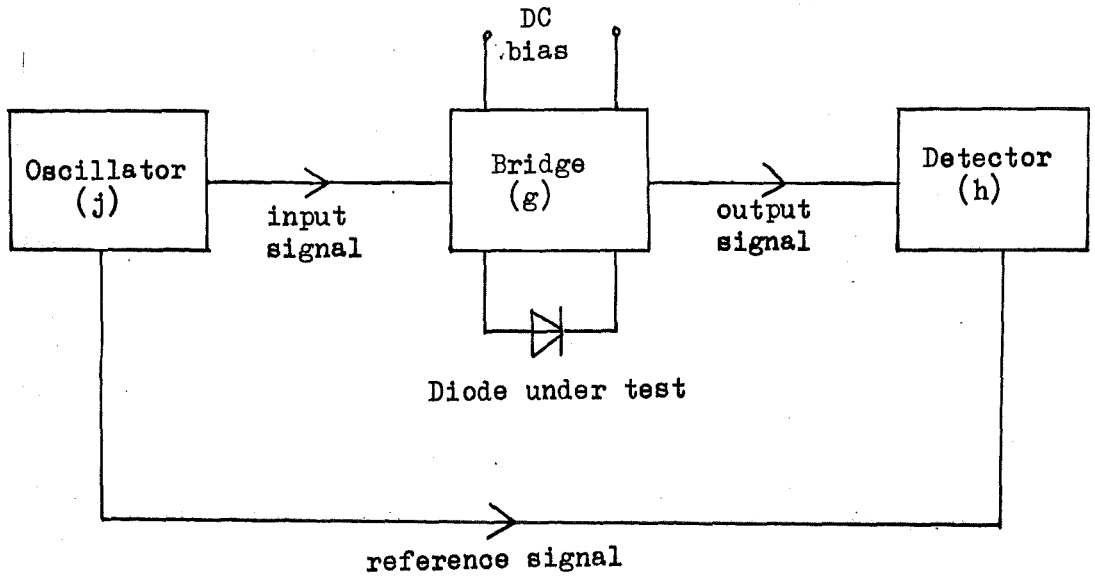


Figure 20 Measurement of diode AC resistance.

is derived in Appendix B. An approximate expression, derived from equation (7) of Chapter 2, which has often been used by other workers is

$$R_{AC} = R_{ES} + \frac{nkT}{q(I_m + I_s)} \qquad \ldots\ldots (29)$$

The measurement equipment was arranged as in Figure 20 and is illustrated in the photograph Figure 21. The universal bridge was of the transformer ratio arm type which allowed application of a steady DC bias to the diode under test while measuring its AC parameters. Figure 22 is a schematic diagram of the bridge connections but does not show details of the internal bridge circuits used to balance the output signal. Measurements of the voltage across a standard resistor in series with the DC bias supply enabled the current through the diode to be deduced.

Although the bridge did have an internal source and detector, these were not used as the internal signal amplitude was 65 mV peak to peak, and in some cases this would have been larger than the DC bias which was between 20 and 800 mV. The use of an external signal generator and phase sensitive detector gave extremely high sensitivity because of the improvement in signal to noise ratio made possible by the very narrow bandwidth of the detector compared with a conventional tuned amplifier. The polarity of the out of balance signal was indicated thus defining the sense of the adjustment neccessary to obtain balance. Another advantage was that the output voltage could be resolved into two components, one corresponding to the resistive unbalance of the bridge, the other to the reactive unbalance. Using this technique the signal size applied to the diode could be as low as 20 μV peak to peak before noise began to overload the detector. In practice a signal of 70 μV amplitude was used as the balance position

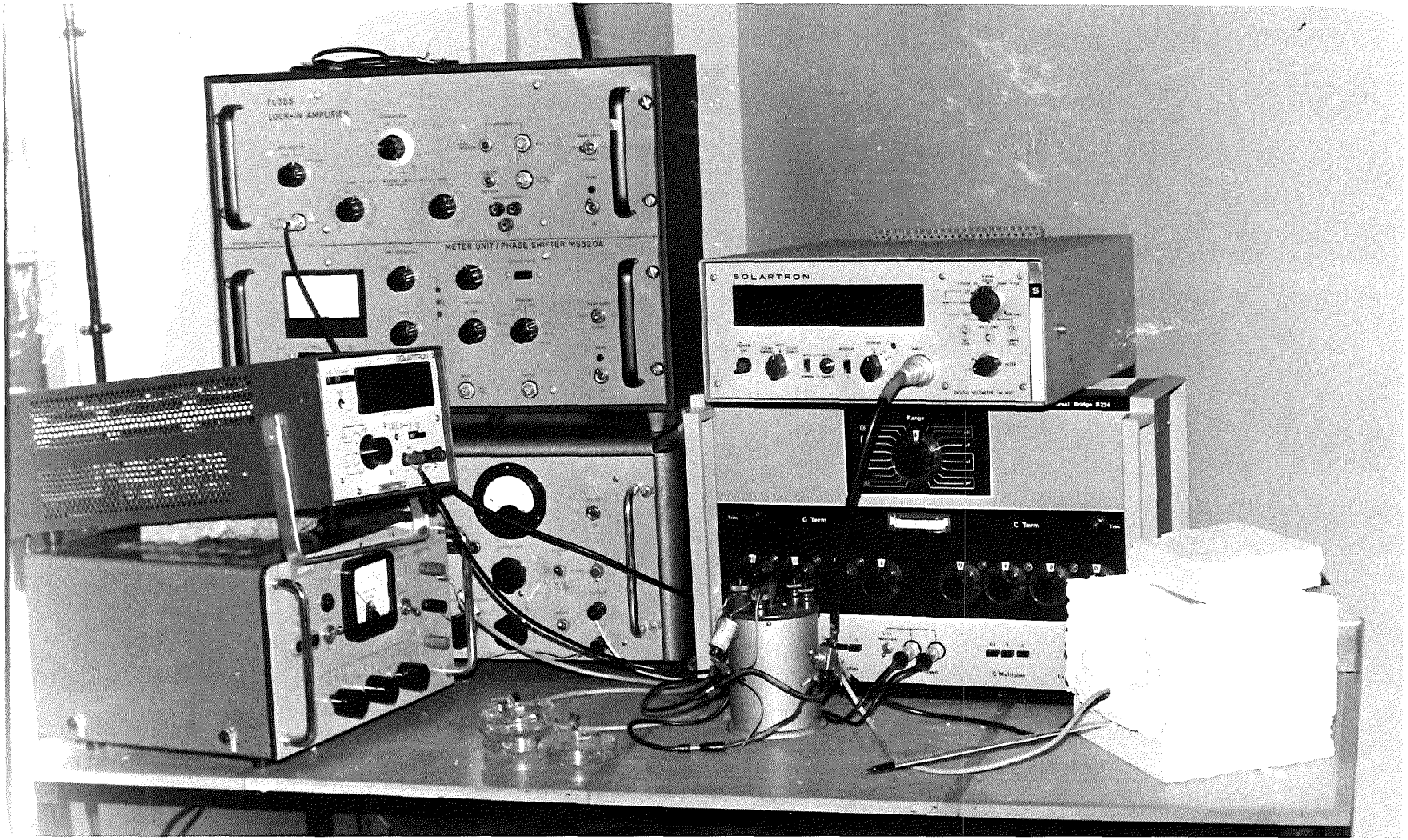


Figure 21 Photograph of Measurement Equipment.

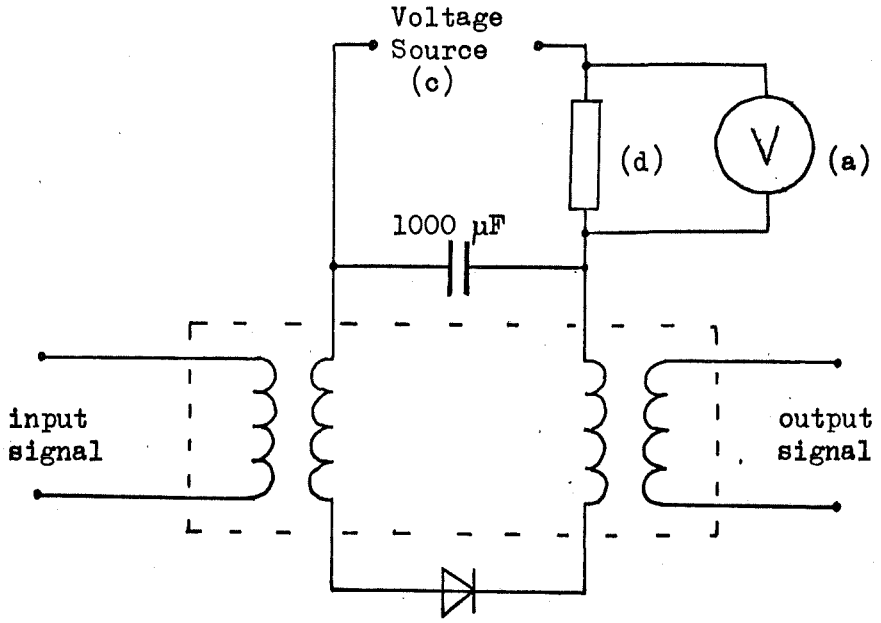


Figure 22 Diagram of connections to Bridge (g).

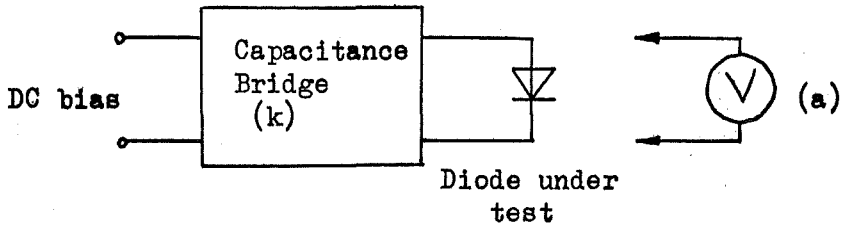


Figure 23 Diode capacitance measurements.

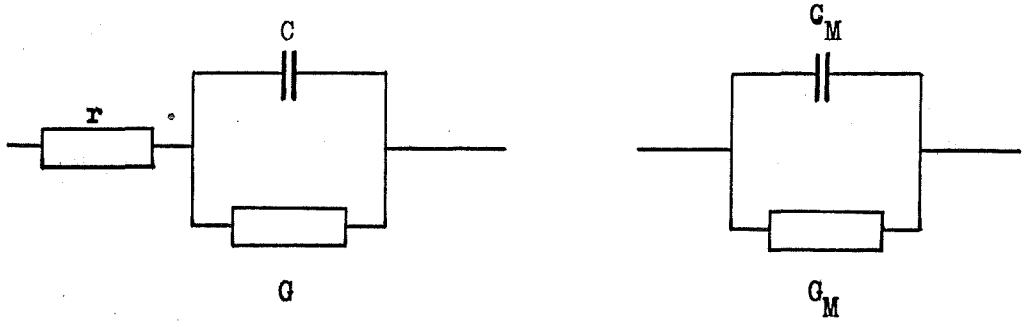


Figure 24 Diode Model (a) , and Equivalent Circuit (b) for bridge measurement of metal-semiconductor contact.

was then sensitive to changes of 1 part in 5000 in the conductance setting which enabled the full accurancy of the bridge ($\pm$ 0.1% of reading) to be realised.

Experimentally it was found that the balance position was not sensitive to variation in the signal frequency between 500 Hz and 20 kHz. However, the bridge sensitivity was greatest at 4 kHz and so this frequency was used for the measurements.

A systematic error in the bridge readings was expected due to the internal resistance of the bridge circuits and the bridge leads. Using the technique suggested in the operating instructions for the bridge, the value of this resistance was measured and found to be 0.31 Ω and 0.23 Ω for the two bridge ranges used. Thus at low bias currents through the diode where the slope resistance was of the order of 500Ω, the lead correction was insignificant, although it became increasingly important at higher bias currents.

The accuracy of the bridge was checked using 10 Ω and 100 Ω ($\pm$ 0.02%) standard resistors and after lead corrections were applied, the measured values agreed with the standard values to within the quoted accuracy of the bridge. Using the above equipment arranged as in Figure 20, it was expected that the accuracy of the current, voltage and slope conductance values would be $\pm$ 0.1% or better. However, because of the extreme sensitivity of the bridge and detector system it was noticed that changes in the ambient temperature of the order of $\pm$ 0.1^{o}C caused detectable changes in the balance position. For this reason, all the measurements were made in a thermostatically controlled room with the additional precautions listed in section 4.1. In addition to changes in ambient temperature it was also apparent that at high diode currents, self heating would occur and so measurements were made to characterise this behaviour. (See section 4.5).

4.3 CAPACITANCE-VOLTAGE MEASUREMENTS

4.3.1 Initial Measurements

The equipment used to measure the diode capacitance as a function of applied bias was connected as shown in Figure 23. The capacitance bridge was self balancing and gave a direct meter reading of the diode capacitance value. Although the bridge had the facility for applying a DC bias to the diode under test through rear terminals, it was found that the voltage appearing across the diode leads was not the same as that applied to the rear terminals. This was because of the internal resistance of the bridge biasing network and the finite current drawn by the diode in reverse bias. This difficulty was overcome by measuring the front terminal voltage directly with a digital voltmeter between readings of capacitance, for which the voltmeter leads were disconnected.

Following Goodman[46] the indicated value of capacitance was corrected for the effect of diode series resistance and reverse leakage current. The indicated value of capacitance C_M was related to the true value of capacitance C by the relation

$$C_M = \frac{C}{\left[(rG+1)^2 + \omega^2 r^2 C^2\right]} \qquad \ldots\ldots (30)$$

where r represents the semiconductor bulk resistance, and the barrier is represented by a voltage dependent capacitor C and a voltage dependent conductance G as shown in Figure 24. In the worst case, near zero bias this correction was of the order of 1%.

The capacitance bridge used a fixed 1 MHz frequency signal of amplitude 15mV. In regions where the diode capacitance was changing rapidly as a function of bias, the comparatively large signal tended to cause a significant change in capacitance. This could be as large as 4% near zero bias although the effect would become less important

as the diode was biased further into the reverse direction.

As the reverse bias across a diode was increased, its capacitance fell until eventually it reached the same order as the stray capacitance of the leads and header can enclosing the diode. Measurements of the capacitance of header cans without diodes attached, allowed correction of measured values to give the true barrier capacitance.

The quoted accuracy of the capacitance bridge was $\pm$ 1% but it can be seen from the above discussion that throughout the range of reverse bias applied to the diode, correction terms have to be applied which make it likely that the total error was larger than 1%. These doubts were reinforced by increasing discrepancies in indicated capacitance value on the different ranges of the instrument as the reverse bias across the diode was reduced towards zero.. Because of this uncertainty, a second series of measurements were made on equipment at the Plessey Company, Allen Clark Research Centre.

4.3.2 Improved Measurements

The experimental arrangement was basically the same as in Figure 23 but with the Boonton 72A bridge replaced by a Boonton 75D which had its own internal DC bias supply. The advantages of the Boonton 75D compared with the 72A were as follows: adjustable signal size and detector gain which enabled a signal of 5 mV amplitude to be used without loss of sensitivity; improved accuracy; and the facility to balance the resistive component of the diode impedance independently of the capacitive component. Even with these improvements it was not possible to make accurate measurements near zero bias because of the influence of the diode conductance G, which increased rapidly in this region and reduced the predicted accuracy of the bridge (see Table 1). In practical terms, there was a notable loss of sensitivity of the balance position when the diode conductance approached 10^{-3}S.

The detailed results of the capacitance-voltage measurements are

given in Chapter 5. The two sets of capacitance measurements agreed to within the quoted accuracy of the bridges at high reverse bias but diverged near zero bias. In general, the measurements using the 75D bridge gave more nearly linear $^1/_{C^2}$ against V plots and hence were more useful in determining the barrier parameters.

4.4 ACTIVATION ENERGY MEASUREMENTS

Measurements of diode current (at fixed voltage) as a function of temperature were made using the same instruments as shown in Figure 18 but with the diode fitted in a brass calorimeter whose temperature could be varied by immersion in various cooling mixtures. The diode temperature was monitored on a Comark Electronic thermometer Type 1602 which was connected to a Chrome-Alumel thermocouple in contact with the diode header can. The instrument calibration was checked using the fixed points of an ice/water mixture and a solid CO_2/methanol mixture.

Measurements were also made between fixed points by using a heat leak into the calorimeter to provide warming or cooling. Very close agreement between diode current values obtained on warming and cooling cycles indicated that the thermocouple probe was in good thermal contact with the diode.

In order to minimise the effect of voltage fluctuations on the current readings, the diodes were reverse biased to a voltage of 110 mV. In this region of the current voltage characteristic, the only voltage dependent term is the image force lowering of the barrier height which is a very slowly varying function of applied bias (See equation (8) Chapter 2).

As well as giving an alternative method of measuring the barrier height, these measurements verified that the temperature variation of the reverse current followed the predictions of equation (25) of Chapter 2. This enabled measurements of diode reverse current to be

used to deduce diode temperature during measurements of the thermal properties of the devices.

4.5 THERMAL MEASUREMENTS

4.5.1 Electrical Method

Each silicon chip mounted on a header can had at least six diode contacts to its top surface. Using one of these diodes at a high forward current to dissipate power, it was then possible to detect changes in the chip temperature by monitoring the reverse current at constant voltage on any other diode. In practice, two sensing diodes were used, one adjacent to the dissipating diode and one at the other edge of the chip (Figure 25) so that variations in temperature across the chip could also be measured. The electrical connections to the chip were as shown in Figure 26. The power dissipated by diode L_3 was calculated from measurements of voltage across the diode and across the 10 Ω standard resistor, and was varied between zero and 50 mW. The current through the sensing diodes S_1 and S_3 was measured at a constant reverse voltage of 300 mV and was in the range 30 to 60 μA so that the power dissipated in these diodes was negligible.

At 300 mV reverse bias, the reverse current I is not very sensitive to changes in voltage, but is very sensitive to changes in temperature. From equations (8) and (25) of Chapter 2.

$$I_R \approx A^* S T^2 \exp\left[-q/kT \left(V_B - \Delta V_B \right) \right]$$

where $$\Delta V_B = \left\{ \frac{q^3 N_D}{8\pi^2 \epsilon_{si}^3} \left(V_B - V_F - kT/q - V \right) \right\}^{1/4}$$

so that for small changes in temperature T above the ambient T_A

$$\ln \left\{ \frac{I_R(T)}{I_R(T_A)} \right\} = 2 \frac{(T - T_A)}{T_A} + \frac{q}{kT_A} \left(V_B - \Delta V_B \right) \frac{(T - T_A)}{T_A} \quad \ldots\ldots (31)$$

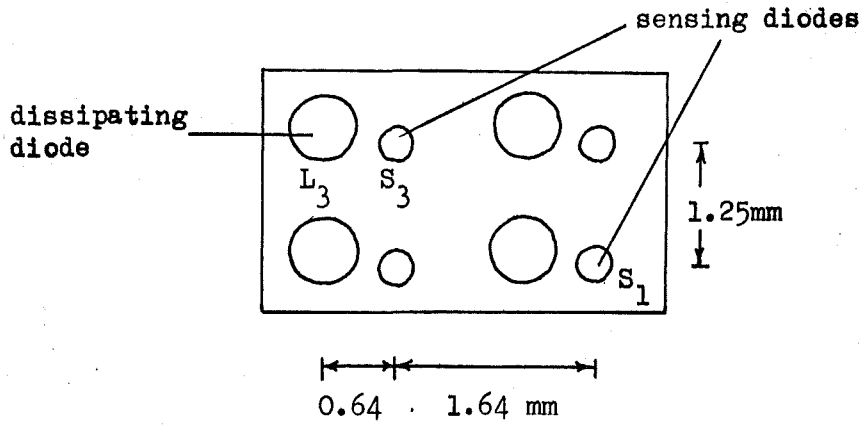


Figure 25 Position of diodes on silicon chip for thermal measurements.

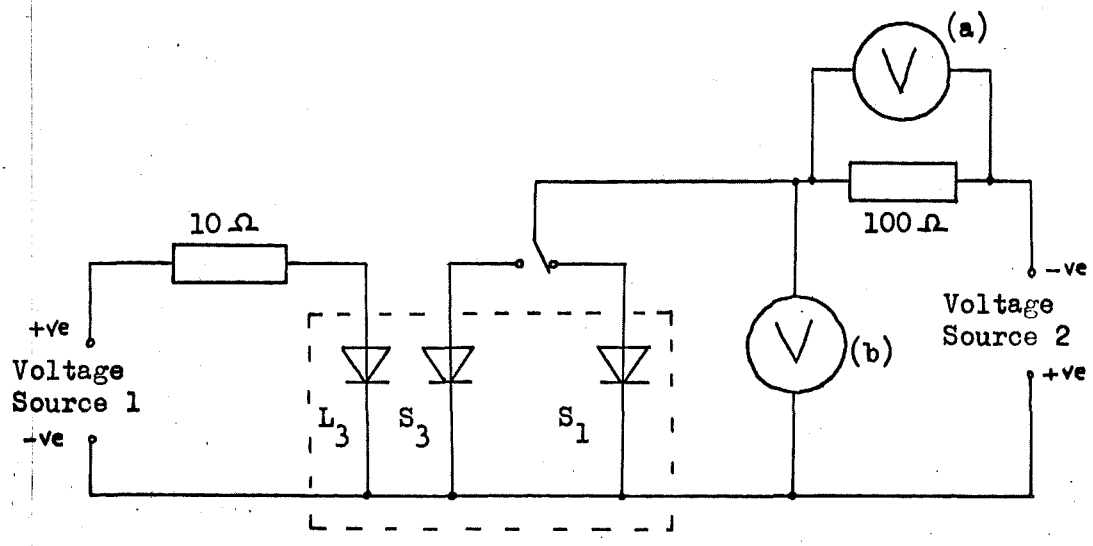


Figure 26 Electrical connections to silicon chip during thermal measurements.

Once the diode reverse current $I_R(T_A)$ has been measured at the ambient temperature T_A, the diode temperature at any later time can be deduced from $I_R(T)$.

Because the reverse current is insensitive to small changes in voltage, many potential sources of error become negligible. The voltage developed across the part of the silicon substrate common to all three diodes was measured on voltmeter (b) by disconnecting the voltage source 2. Even at the highest forward current through L_3 this voltage was only 5 mV which effectively increased the reverse bias on S_1 and S_3 to 305 mV which would have caused about 0.3% increase in I_R. This was compared with the increase of about 30% in I_R due to the temperature rise at the same current. The temperature gradient across the silicon caused a thermoelectric emf to be developed, but for the maximum measured temperature change across the silicon of 0.6°C, this voltage would have been of the order of[61] 0.5 mV which was negligible.

The main errors in the determination of temperature rise came from the errors in the measured values of reverse current ($\pm$ 0.25%), the value of $(V_B - \Delta V_B)$ ($\pm$ 2%) and the error in the measured current and voltage of the dissipating diode which gave an error in the power of $\pm$ 2% so that the resultant error in the calculated value of θ, the thermal resistance, was of the order of $\pm$ 10%.

In addition to the thermal resistance, the thermal time constant τ_{TH} of the diode and header system was determined by allowing the system to reach a steady temperature with a high power dissipation and then switching off the dissipating diode and recording the sensing current I_R as a function of time.

4.5.2 Infra-red Radiometric Method

An alternative technique used an Infra-red Radiometric microscope model RM-2A manufactured by the Barnes Engineering company, Stamford,

Connecticut, U.S.A., to measure the chip surface temperature directly. The instrument uses an Indium Antimonide detector of infra-red radiation, cooled by liquid nitrogen, to compare the radiance of the sample with the radiance from a black body at room temperature. The resolution of the instrument was $\pm \frac{1}{2}^{o}C$ at $20^{o}C$ and improved as the temperature increased. The same techniques of measuring power dissipation as described in section 4.5.1 were used. The microscope spatial resolution was better than 100 μm so that the temperature variation across the chip was detected. The use of the radiometric technique requires a knowledge of the emissivity of the sample surface relative to that of a black body (emissivity 1). This was obtained by a preliminary measurement of the radiance from a chip placed upon the calibrated hotplate provided with the instrument.

The disadvantage of the radiometric method was that the measurements could not be made under the same conditions as the current-voltage measurements when the chip was enclosed in the alloy box insulated by expanded polystyrene. Thus the results of the radiometric method could not be compared directly with the measurements described in section 4.5.1 which were made with the chip enclosed in the box and insulation.

CHAPTER 5

RESULTS

Initial measurements of titanium Schottky barrier diodes formed on n-type silicon of donor concentration $N_D = 9 \times 10^{20}$ m^{-3}, showed minor anomalies in the current-voltage characteristics[62] which could not be explained in terms of the thermionic emission theory. In order to check a possible explanation in terms of the thermionic-diffusion model, the investigation was widened to include silicon samples of donor concentration 2×10^{20} m^{-3} and 3×10^{21} m^{-3} as well as two further metals, aluminium and magnesium. In this chapter the results are presented in three sections corresponding to the three barrier metals used. The following chapter discusses the interpretation of the results in terms of the alternative theories available.

For the purpose of identification, all the diodes were referred to by an alphanumeric code (e.g. $D10AL_3$) in which the initial letter refers to the metal, D for titanium, E for aluminium and F for magnesium. The following number and letter identifies the silicon slice and chip from that slice, and the final letter and number locate the diode on the chip and indicate its diameter (L diodes are approximately 750 μm diameter and S diodes 250 μm).

5.1 TITANIUM

5.1.1 General

The most striking feature of the titanium diodes was the almost identical behaviour of diodes from a particular slice, and the very small spread between slices of the same donor concentration. Table 2 shows a typical set of voltage readings at constant current for diodes of two sizes on two chips from the same slice. Table 3 lists

TABLE 2 Measurements indicating the uniform electrical properties of diodes from a particular slice.

Chip Number	Diode Number	Voltage Readings in mV at current level indicated	
		0.1000 mA	1.000 mA
D12A	S_1	36.9	107.0
	S_2	36.7	106.4
	S_3	36.8	107.2
	S_4	36.8	107.1
D12B	S_2	37.7	108.4
	S_3	37.7	108.1
		0.1980 mA	1.980 mA
D12A	L_1	13.8	58.8
	L_2	13.4	57.7
	L_3	13.5	58.1
	L_4	13.6	58.5
D12B	L_1	14.0	58.9
	L_2	14.1	59.2
	L_3	14.0	59.0

TABLE 3 Titanium n-type silicon barrier heights from current-voltage measurements.

Diode	Barrier Height V_B volts	N_D m^{-3}
$D3AS_1$	0.500 ± .005	9×10^{20}
$D4CS_3$	0.500 ± .005	"
$D6AS_1$	0.510 ± .005	"
$D7AS_2$	0.495 ± .005	"
$D8AL_4$	0.495 ± .005	"
$D12BL_2$	0.490 ± .005	"
Mean	0.500 range ± .010	"
$D11AS_3$	0.485 ± .005	3×10^{21}
$D10AS_2$	0.500 ± .005	2×10^{20}

TABLE 4 Comparison of titanium n-type silicon barrier heights from activation energy plots and current-voltage measurements.

Diode Number	Barrier Height volts	
	$E_A/_q + \Delta V_B$	V_B (I - V)
$D1AS_1$	0.55 ± .01	0.545 ± .005
$D2AS_1$	0.56 ± .01	0.555 ± .005
$D4AS_1$	0.51 ± .01	0.500 ± .005
$D4CS_3$	0.51 ± .01	0.500 ± .005

the calculated barrier heights for diodes from eight slices.

5.1.2 Barrier Height

(a) Current-Voltage Characteristics

The current-voltage characteristics in most cases, could be interpreted in terms of equation (7) if the effect of series resistance was included. Figure 27 shows the measured current voltage characteristic for $D11BS_3$ which had only a limited linear region between 75 and 100 mV before the voltage drop across the series resistance became significant. However, if the measured values of voltage Vm were corrected for the small voltage drop across the series resistance to give V and then $\frac{I_m}{1 - \exp(-qV/kT)}$ was plotted against V, a linear plot was obtained, with slope corresponding to an 'n value' of $1.03 \pm .01$. This procedure was equivalent to representing the current-voltage characteristics by equation (16a)

$$I = I_s \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right]$$

The intercept of this plot with the current axis, I_s (V = 0) could then be used to calculate the barrier height using equation (25)

$$I_s = A^* S T^2 \exp\left[-q/kT\left(V_B - \Delta V_B\right)\right]$$

where the value of A* was taken[40] as 110 amp cm^{-2} $^oK^{-2}$.
The barrier height value was relatively insensitive to the small changes in A* caused by electron tunnelling, scattering, and diffusion effects which are discussed in Appendix A. The dominant barrier lowering mechanism was found to be image force lowering (Section 5.1.6) and so the barrier height values in Table 3 have been corrected by the calculated value of ΔV_B at zero bias.

The mean value of barrier height of 0.50 volts agreed very closely with previously published results of Cowley[30] (0.50 volt), Saltich[31]

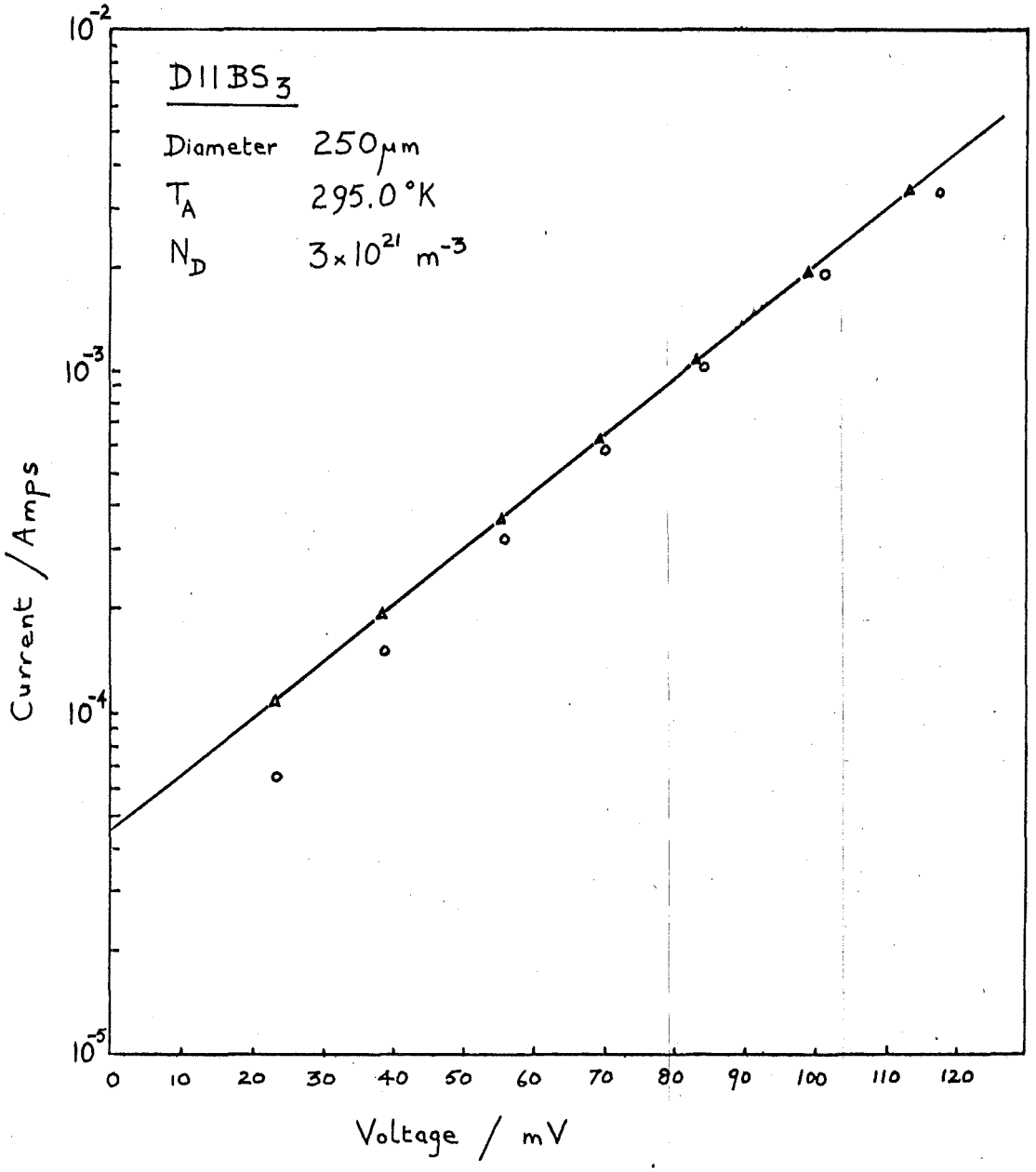


Figure 27 Current-voltage characteristics of a titanium n-type silicon diode plotted as :-

(a) ∘ I_m against V_m .

(b) Δ $\dfrac{I_m}{1 - \exp(-qV/kT)}$ against V, where $V = V_m - I_m R_{ES}$.

(0.48 volt), and Saltich and Terry[32] (0.51 volt).

(b) Activation Energy Measurement

This technique was only used on a small number of diodes because of the long time period needed to complete a cooling and heating cycle. The experimental plots of $\ln \frac{I}{T^2}$ against $\frac{1}{T}$ were linear between room temperature and $-50^{o}C$, but below that the current was greater than that expected from the thermionic emission theroy, presumably due to edge leakage or tunnelling effects. By inspection of equation (25) it can be seen that E_A, the activation energy obtained from the slope of the plot should be equal to $q\ (V_B - \Delta V_B)$ if thermionic emission was the dominant current transport mechanism. Table 4 shows the barrier height values obtained from the activation energy plots where ΔV_B was taken as the image force lowering at the reverse bias of 110 mV used. Also shown are the corresponding values from current-voltage measurements. The good agreement between the barrier heights obtained from the two measurement methods confirms that thermionic emission was the dominant current contribution at room temperature. Diodes $D1AS_1$ and $D2AS_1$ were fabricated at a very early stage using an unshuttered titanium evaporation and the barrier heights were significantly higher than all the later results using the shuttered evaporation technique described in Chapter 3.

(c) Capacitance-Voltage Characteristics

According to equation (26) the plot of $1/C^2$ against V should be linear with slope $\frac{2}{q\ N_D\ \epsilon_{si}\ S^2}$ and intercept $V_D = V_B - V_F - kT/q$. Although most of the experimental plots were linear, several were not, even using the improved measuring technique described in section 4.3.2. Cowley[30] also obtained non-linear plots which he attributed to the presence of an interfacial layer, even though he obtained linear plots with other metal contacts using the same silicon surface preparation. His explanation seems unlikely, especially as Card and Rhoderick[35]

obtained linear plots with surface oxide layers present of thickness between 0.8 and 2.6 nm. A much simpler explanation is that the lack of balance sensitivity when measuring capacitance near zero bias, led to increasing errors in the capacitance values. As discussed in section 4.3.2, this lack of sensitivity was due to the high parallel conductance of the diodes resulting from their low barrier height. This explanation is consistent with Cowley's observation of linear plots for other metals, all of which had higher barriers than titanium. An additional factor contributing to non-linearity would be any non-uniformity in the impurity concentration through the epitaxial layer. Figure 28 shows some typical plots of $1/C^2$ against bias. Table 5 lists the barrier heights deduced from the intercepts. From the slope of the plot the value of N_D was deduced and then V_F was calculated using the expression[40]

$$V_F = \frac{kT}{q} \ln \frac{N_C}{N_D} \qquad \ldots\ldots (32)$$

The barrier heights from capacitance voltage measurements showed a greater spread in values than those from the current-voltage measurements but were generally higher. Differences between the barrier heights, measured by the two techniques, of the order of 10 mV have been recorded by several previous workers[31, 63, 67, 68] and represent the change in effective barrier height from zero electric field (C - V method) to zero applied bias (I - V method) when the internal electric field is not zero.

5.1.3 Impurity Concentration N_D

Apart from D10 and D11, all the silicon slices used in the investigation were supplied with a nominal doping 6.5 to 9 x 10^{20} m^{-3}. D10 and D11 were supplied to nominal doping concentrations of 3 x 10^{20} m^{-3} and 3 x 10^{21} m^{-3} respectively. Table 6 lists the

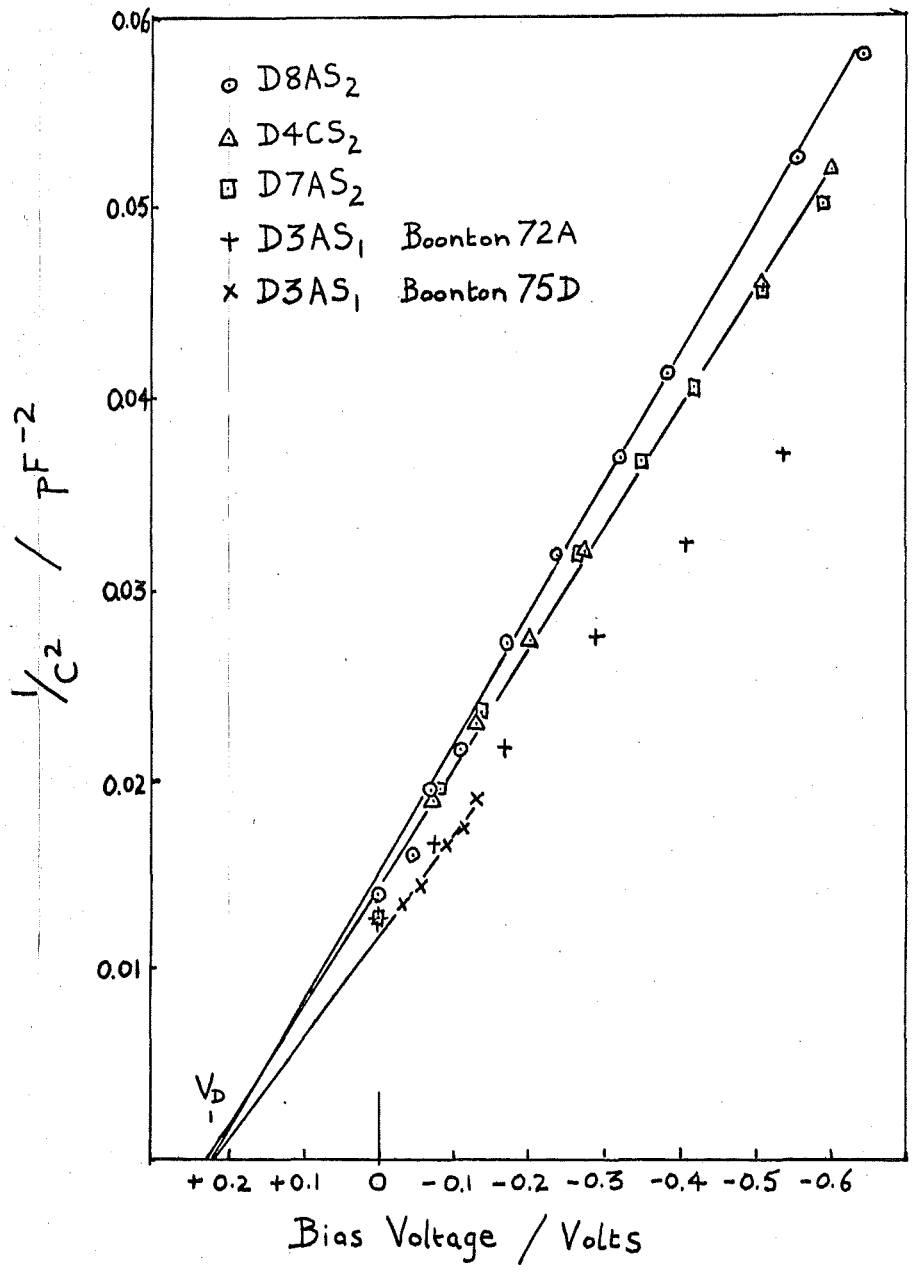


Figure 28 Capacitance-voltage characteristics of titanium n-type silicon diodes plotted as $^1/_C2$ against V. ($N_D \approx 9 \times 10^{20} m^{-3}$)

TABLE 5 Titanium n-type silicon barrier heights from Capacitance-voltage measurements.

Diode	Intercept V_D	$V_B = V_D + V_F + {}^{kT}/_{q}$ volts
$D3AS_1$	0.23 ± .01	0.52 ± .01
$D3BS_1$	0.23 ± .01	0.52 ± .01
$D4AS_1$	0.25 ± .02	0.54 ± .02
$D4CS_2$	0.23 ± .02	0.52 ± .02
$D4CS_3$	0.25 ± .02	0.54 ± .02
$D6AS_1$	0.24 ± .02	0.53 ± .02
$D7AS_2$	0.24 ± .02	0.53 ± .02
$D8AS_2$	0.23 ± 0.1	0.52 ± .01
$D8AL_4$	0.22 ± .02	0.51 ± .02
$D11AL_2$	0.23 ± .01	0.52 ± .01
$D12AL_1$	0.26 ± .02	0.55 ± .02

Mean 0.53

experimentally determined impurity concentrations from capacitance-voltage measurements, which correlate very well with the manufacturer's nominal values. It was not possible to make four point probe resistivity measurements because the surface n-type epitaxial layers were deposited on heavily doped n^+ substrates. Table 6 also lists the estimates of impurity concentration deduced from measurements of diode series resistance described in the following section.

5.1.4 Additional Barrier Model Parameters

(a) Series Resistance R_{ES}

In many cases the variation of the diode AC Resistance as a function of current followed the approximate relationship (equation (29))

$$R_{AC} = R_{ES} + \frac{n\,kT}{q\,(I_M + I_S)}$$

The value of the series resistance R_{ES} was then obtained from the intercept of the plot of R_{AC} as a function of $(I_M + I_S)^{-1}$. In the cases where diffusion or other effects caused a non-linearity in the plot, it was still possible to obtain a rough estimate of R_{ES}. As discussed in Appendix B $R_{ES} = R_S + R_L$ where R_S is the resistance of the quasi-neutral epitaxial region, and R_L is the resistance of the substrate, back contact and leads. R_L is assumed to be independent of the area of the front contact S, whereas $R_S(0) = \rho\,(x_{EPI} - \lambda(0))/S$. Hence the values of R_S and R_L were deduced from the values of R_{ES} for the large and small diameter diodes on each chip. Table 6 includes the values of impurity concentration obtained from the resistivity ρ using published curves[40].

(b) Epitaxial Layer Thickness x_{EPI}

Figure 29 shows the experimental capacitance-voltage characteristics plotted as $1/C^2$ against V for diodes from slice D11. The abrupt change

TABLE 6 Diode parameters : impurity concentration and epitaxial layer thickness.

Diode Number	Impurity Concentration N_D m^{-3}			Nominal Epitaxial Layer thickness μm
	Nominal	C - V plot	R_{ES} Value	
$D1AS_1$	7×10^{20}	5.7×10^{20}	-	15 ± 1
$D2AS_1$	"	6.1×10^{20}	-	"
$D3AS_1$	6.5 to 9×10^{20}	9.2×10^{20}	-	"
$D4AS_1$	"	7.0×10^{20}	-	"
$D4CS_2$	"	6.6×10^{20}	-	"
$D4CS_3$	"	6.9×10^{20}	-	"
$D6AS_1$	"	8.0×10^{20}	-	"
$D7AS_2$	"	7.2×10^{20}	-	"
$D8AS_2$	"	8.2×10^{20}	-	"
$D8AL_4$	"	7.5×10^{20}	-	"
$D10AL_3$	2 to 3×10^{20}	$\sim 2 \times 10^{20}$	$\sim 2 \times 10^{20}$	1.5
$D11AL_2$	2 to 3×10^{21}	3.3×10^{21}	2×10^{21}	"
$D11BL_4$	"	3.0×10^{21}	2×10^{21}	"
$D12AL_1$	6.5 to 9×10^{20}	9.1×10^{20}	9×10^{20}	15 ± 1
$F19AL_1$	8×10^{20}	7.7×10^{20}	9×10^{20}	"
$F19AL_3$	"	8.4×10^{20}	-	"

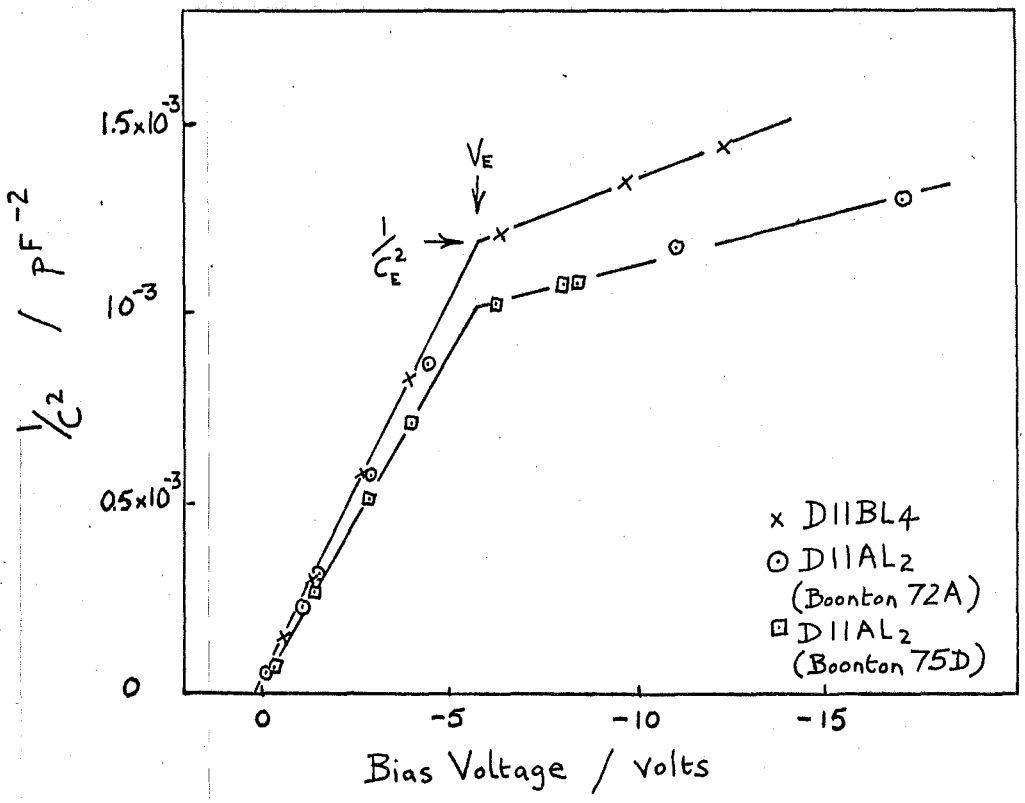


Figure 29 Capacitance-voltage characteristics of Ti / n-Si diodes showing abrupt change in donor concentration when the epitaxial region becomes fully depleted. $N_D = 3 \times 10^{21} m^{-3}$ for epitaxial layer.

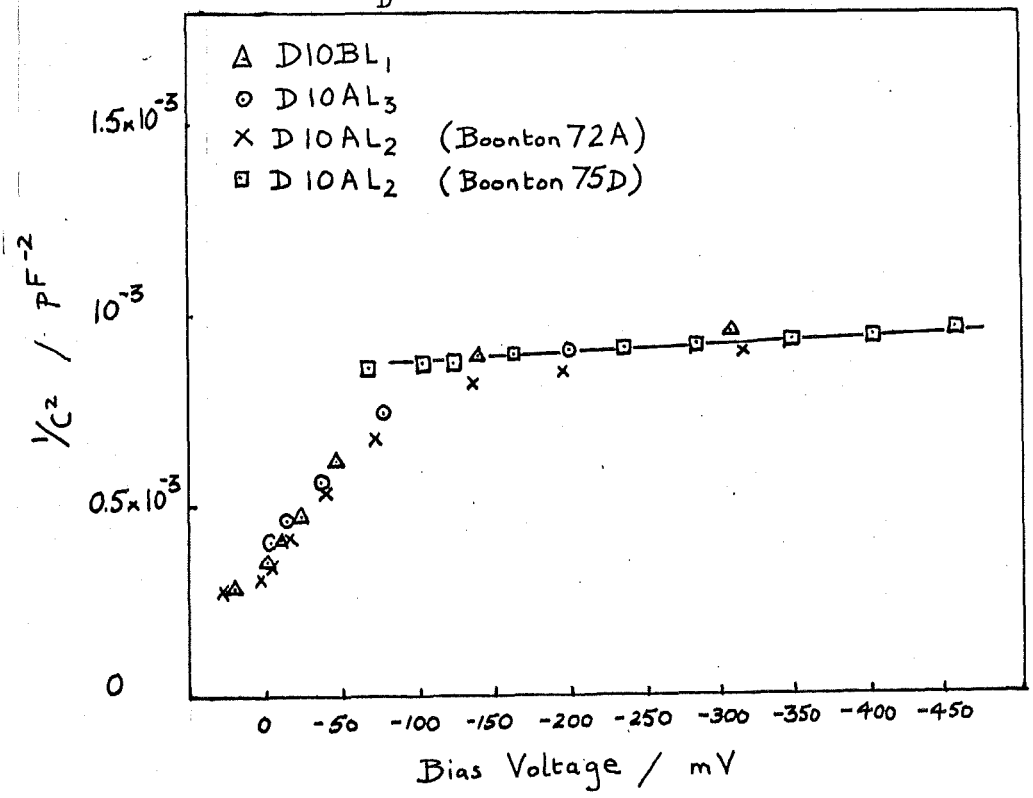


Figure 30 Capacitance-voltage characteristics of Ti / n-Si diodes. The lightly doped epitaxial layer becomes fully depleted for very small reverse bias voltages of the order of 100 mV.

in slope resulted from the change in impurity concentration when the depletion region reached the substrate. Using the value of reverse voltage, V_E, at which the change in slope occured, and the epitaxial region donor concentration, N_D, the epitaxial layer width x_{EPI} was calculated using the relation ship

$$x_{EPI} = \lambda(V_E) = \left[\frac{2\epsilon_{Si}(V_D - V_E)}{q N_D} \right]^{1/2}$$

The calculated value of x_{EPI} was 1.5 ± 0.1 µm which agreed well with the nominal value quoted by the supplier. The value of x_{EPI} was also calculated from the capacitance C_E at which the epitaxial region was fully depleted. $C_E = \frac{S\,\epsilon_{si}}{x_{EPI}} = 30 \pm 1$ pF so that $x_{EPI} = 1.5 \pm .05$ µm.

This technique could not be used for the nominally 15 µm thick epitaxial layers on other slices, as the voltage required to fully deplete the epitaxial region would have been about 130 volts, in excess of the breakdown voltage of the diodes. However the excellent agreement between the doping concentration calculated from the series resistance R_{ES}, using the nominal value of x_{EPI}, and other methods showed that a value of 15 µm for x_{EPI} was consistent with the other measurements. (See Table 6).

For the diodes formed on slice D10, the lightly doped epitaxial layer was almost fully depleted at zero bias, so that it was difficult to get a precise value for V_E. (Figure 30). However, the value of 33 ± 1 pF for C_E gave a value of $1.4 \pm .05$ µm for x_{EPI} which was close to the nominal value of 1.5 µm.

(c) Thermal Parameters

Figures 31 (a) and 31 (b) show the measured diode temperature rise as a function of dissipated power for steady state conditions using the two techniques described in Section 4.5. For steady state conditions, the thermal resistance θ_{DC} had a value $215 \pm 15^{\circ}C$ watt^{-1} for chip D12A and $230 \pm 20^{\circ}C$ watt^{-1} for chip D7A using the electrical

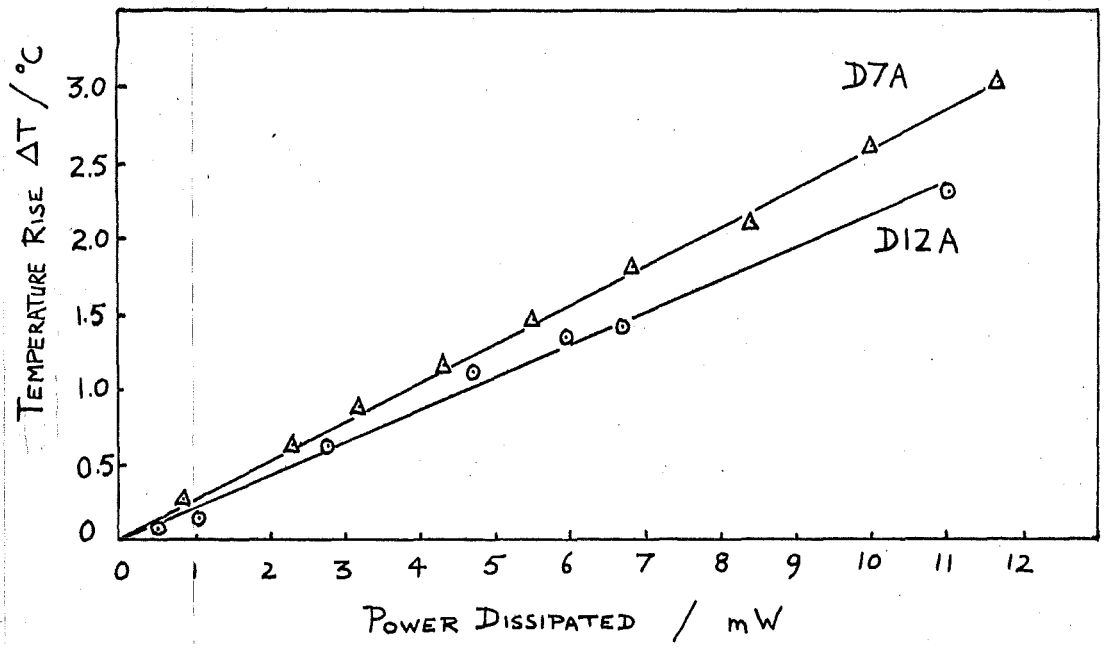


Figure 31(a) Diode temperature rise as a function of power dissipation, measured by the electrical method.

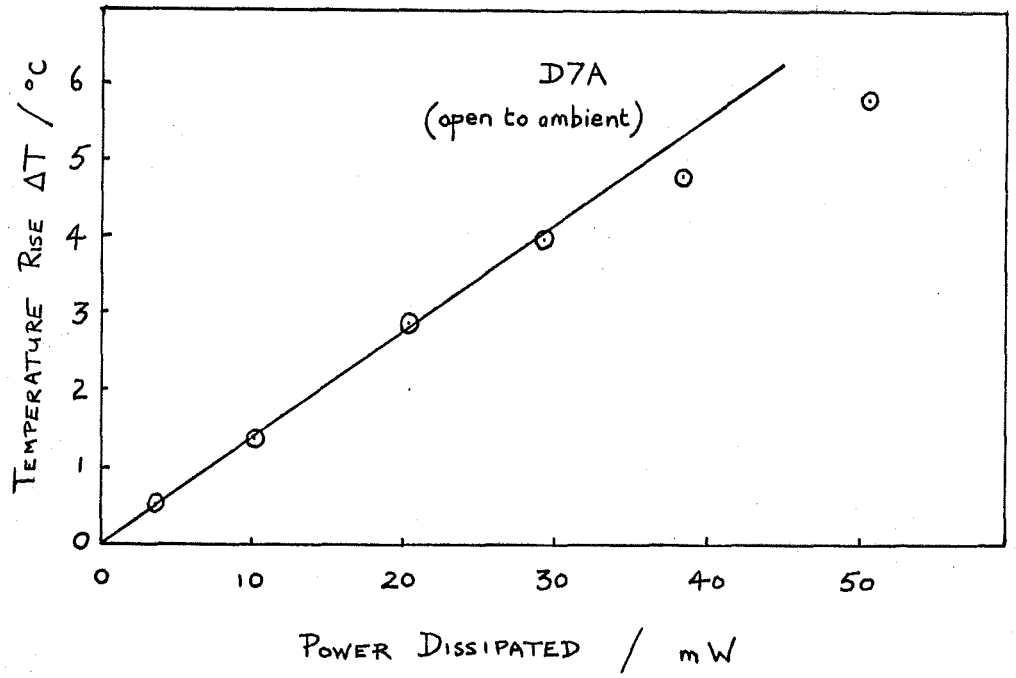


Figure 31(b) Diode temperature rise as a function of power dissipation, measured by radiometric microscope.

method. The radiometric microscope method gave a value of $150 \pm 30^{\circ}C$ $watt^{-1}$ for chip D7A but, as discussed in Section 4.5, this value cannot be compared directly with the electrical measurement, because the diode was uncovered for the microscope measurement. The microscope was just able to resolve a temperature variation across the chip at the highest power dissipation used, which was of the order of $10^{\circ}C$ $watt^{-1}$ across 1.4 mm. The electrical method detected a temperature difference between the two measurement diodes 2.1 mm apart, equivalent to $12 \pm 4^{\circ}C$ $watt^{-1}$. The distance between the power dissipating diode and the nearest sensing diode was only 0.6 mm so that the temperature between them caused only a small error in the determination of Θ_{DC}.

Figure 32 shows the thermal behaviour of the sensing diode after an instantaneous reduction of the power dissipation from 17 mW to 15 μW (the power dissipated by the sensing diode). $\ln\left\{\frac{I_R(T)}{I_R(T_A)}\right\}$, which is proportional to ΔT, is plotted on a logarithmic scale against time. The linear relationship found between 30 and 180 secs. corresponded to an exponential decay of temperature with a time constant $\tau_{TH} = 75 \pm 5$ secs. The fall in temperature during the first few seconds was much more rapid and corresponded to the shorter thermal time constants of the chip/header system (see Appendix D). The expected thermal time constant for the header can/ambient system was of the order of 40 secs.

5.1.5 Forward Current-Voltage Characteristics

As discussed in Section 5.1.2, the major features of the current-voltage characteristics for most diodes, could be represented by equation (16a) if the effect of series resistance was taken into account. However, there were deviations which were greatest for the diodes on the silicon of lowest impurity concentration. Figure 33 shows the experimental values of $\ln\left[\frac{I_m}{1-\exp(-qV/kT)}\right]$ plotted against diode voltage V, for large diodes from slices D10, D11 and D12. These

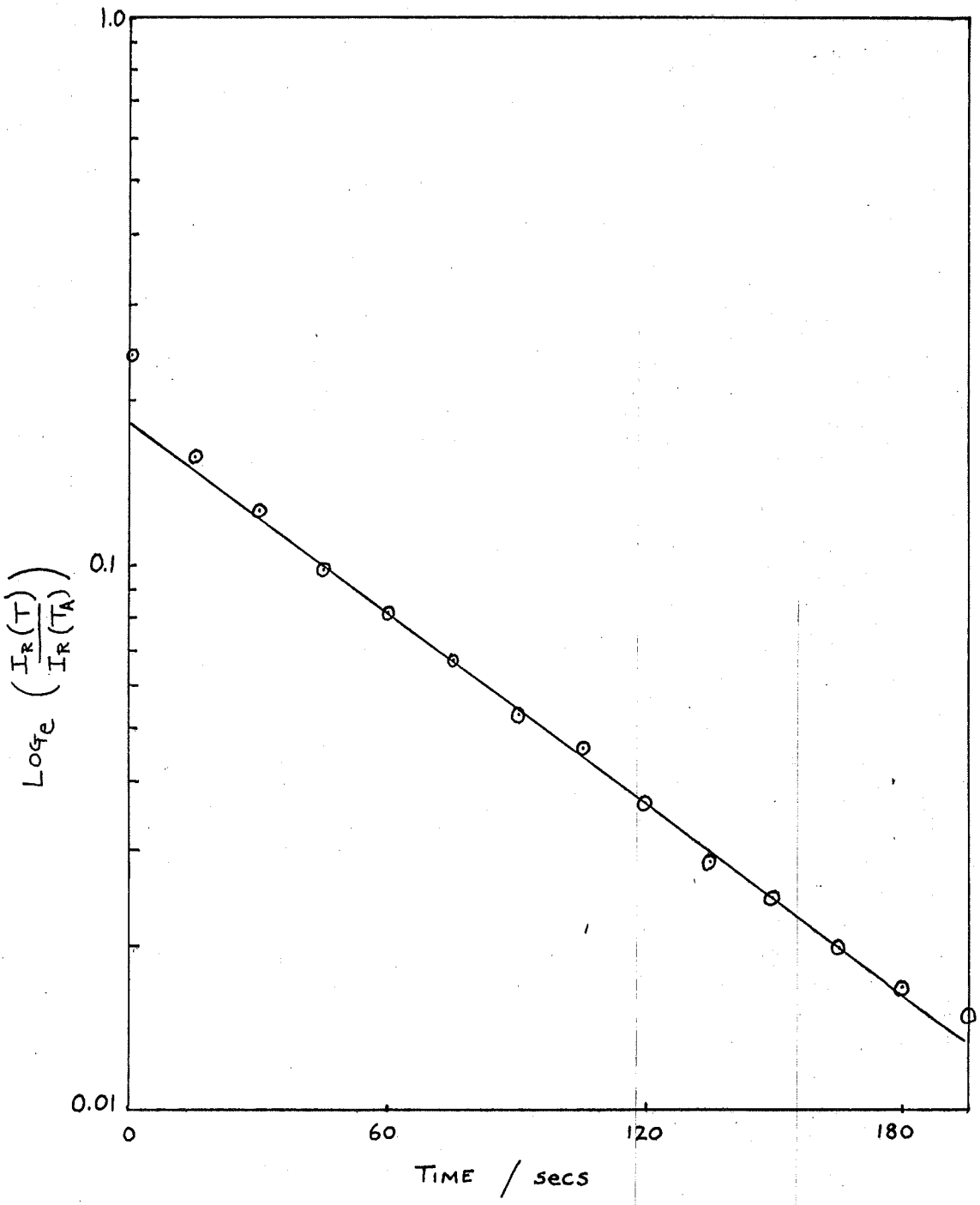


Figure 32 Cooling characteristic of diode after an instantaneous drop in dissipated power. $\ln\left\{\frac{I_R(T)}{I_R(T_A)}\right\}$ is proportional to $\Delta T = T - T_A$ for small temperature changes.

slices were cleaned together as a group and then had the metal layers deposited in the same evaporation. Thus if there was an interfacial layer present, it would be identical for all three slices. Although the plots were linear, the saturation current density at any particular voltage was significantly lower for the diodes on the slices of lower doping, and was coupled with a higher n value (smaller slope). Similar, but more pronounced effects were observed on small diodes from the same slices, D10, D11 and D12, as shown in Figure 34. Due to the size difference, the current density at any given current was about ten times larger for these diodes compared with those shown in Figure 33. The plots for small diodes from slice D10 became non-linear at high current densities. In terms of equation (16a)

$$I = I_s \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right]$$

the non-linearity is equivalent to a decreasing value of I_S or an increasing value of n. It is shown in Appendix A that this equation is not valid when either of these parameters is changing rapidly as a function of voltage.

However, in the case where the plots were almost linear, then the n values were determined from the slope, and the experimental results are presented in Table 7. The spread of n values for diodes fabricated on a particular slice was of the order of $\pm$ 1% for the two more heavily doped slices D11 and D12. For the lightly doped slice D10 the high n values and large spread were indicative of major deviations from the simple thermionic emission theory. In Chapter 6 it is shown that these deviations can be explained, for the most part, in terms of the thermionic diffusion theory.

5.1.6 Reverse Current-Voltage Characteristics

The activation energy plots, discussed in Section 5.1.2 (b), have already suggested that thermionic emission was the dominant reverse

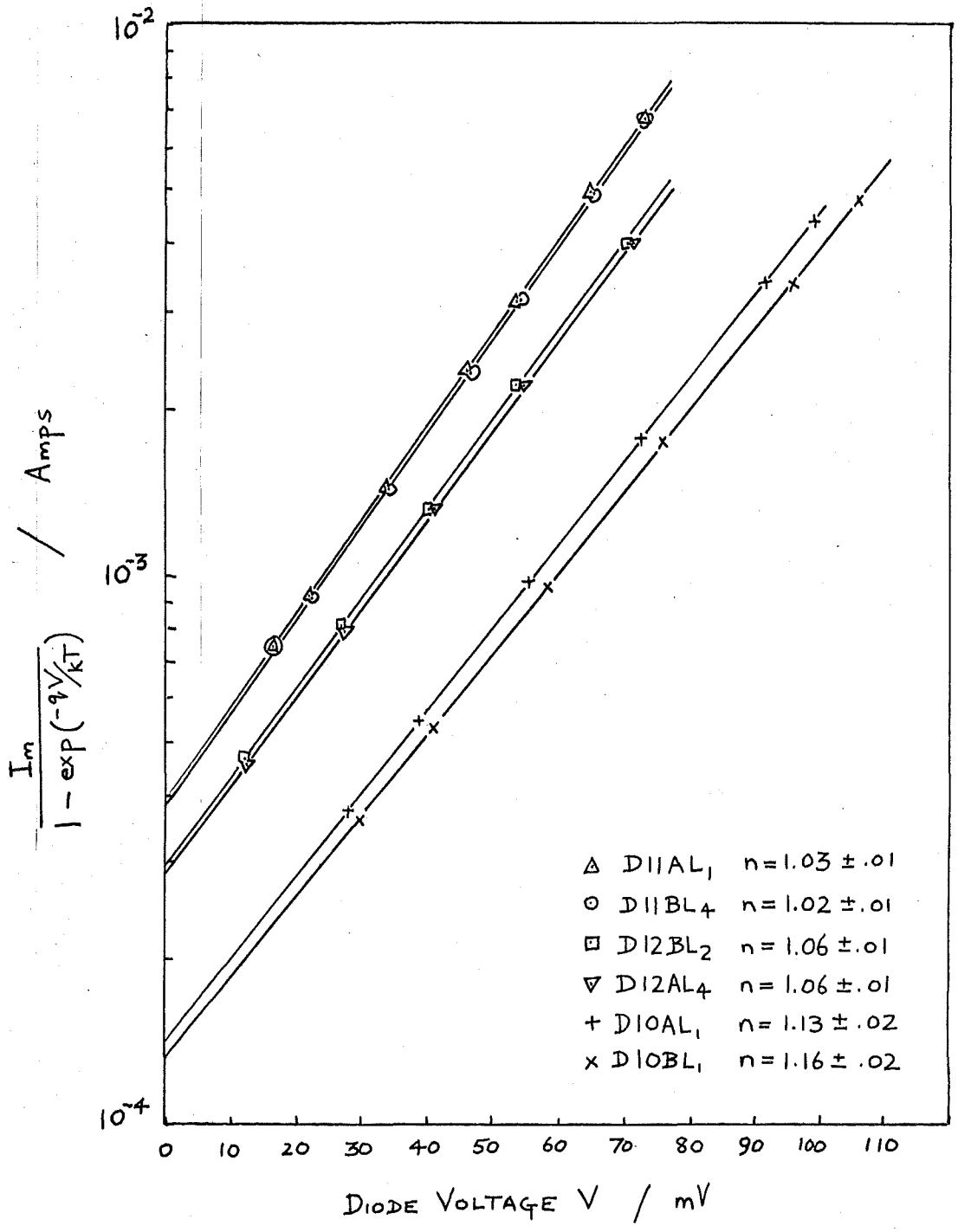


Figure 33 Current-voltage characteristics of 750 μm diameter titanium n-type silicon diodes. Silicon impurity concentrations were $3 \times 10^{21} m^{-3}$ (D11), $9 \times 10^{20} m^{-3}$ (D12), and $2 \times 10^{20} m^{-3}$ (D10).

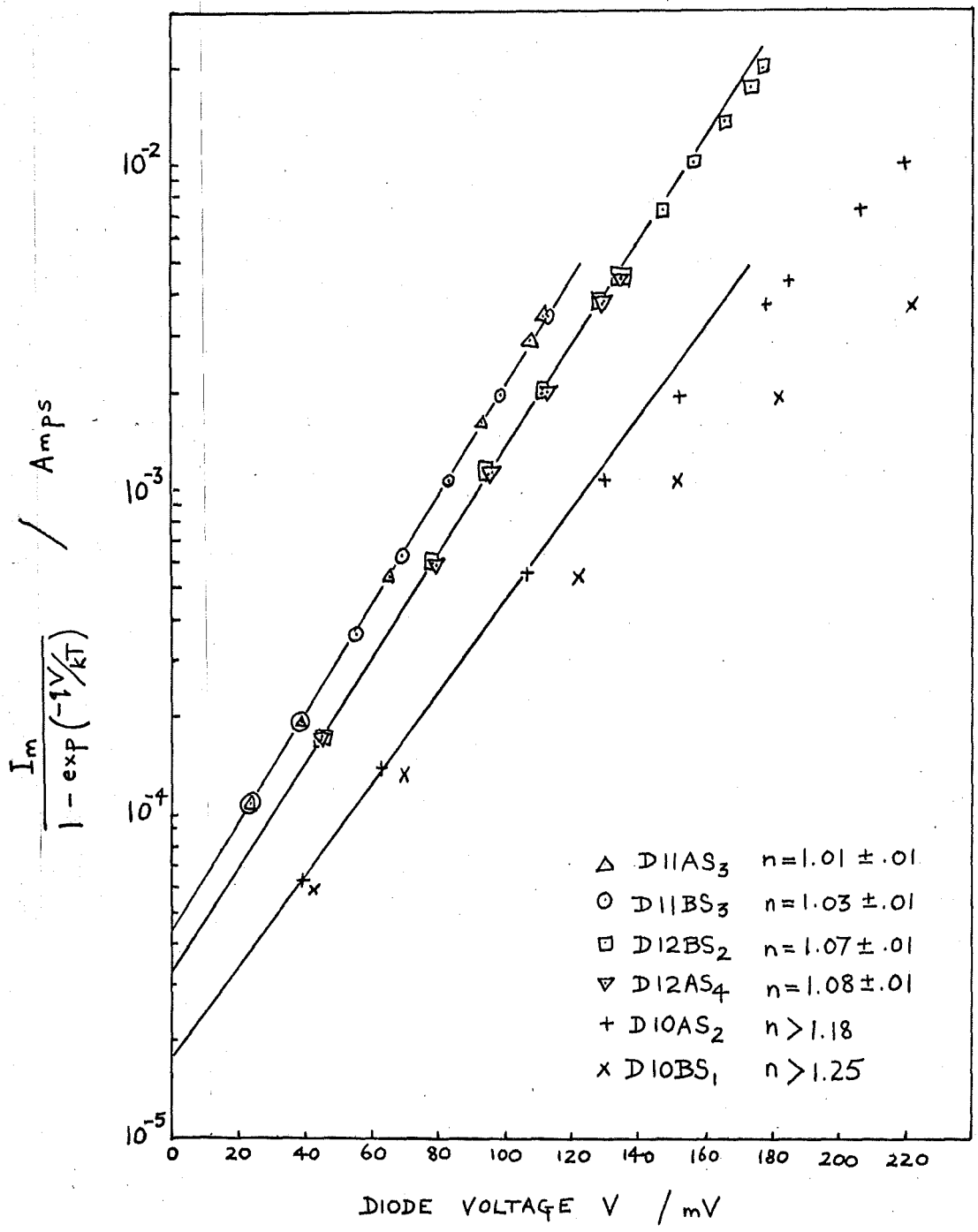


Figure 34 Current-voltage characteristics of 250 μm diameter titanium n-type silicon diodes.

TABLE 7 Experimental n values from current-voltage (I - V) measurements and from AC Resistance (R_{AC}) measurements.

Diode Number	n Value		Impurity Concentration m^{-3}
	I - V	R_{AC}	
$D11AL_1$	1.03	1.01	3×10^{21}
$D11BL_4$	1.02	1.01	"
$D11AS_3$	1.01	1.03	"
$D11BS_3$	1.03	1.02	"
$D12AL_4$	1.06	1.02	9×10^{20}
$D12BL_2$	1.06	1.02	"
$D12AS_4$	1.08	1.06	"
$D12BS_2$	1.07	1.06	"
$D10AL_1$	1.13	1.06	2×10^{20}
$D10BL_1$	1.16	1.07	"
$D10AS_2$	>1.18	>1.17	"
$D10BS_1$	>1.25	>1.11	"

current mechanism at room temperature. Further evidence supporting this hypothesis came from the reverse current-voltage characteristics. Figure 35 shows the experimental results plotted as $\ln\left[\frac{I_m}{\exp(qV/kT)-1}\right]$ against $(V_B - V_F - kT/q - V)^{1/4}$ for several diodes. The linear relationship evident between reverse voltages of 200 mV and 20V was consistent with image force lowering of the barrier height being the dominant reverse current mechanism in this range. Table 8 lists the experimental slopes for comparison with the theoretical values for two impurity concentrations and two temperatures. Although the experimental values were close to the theoretical values, they were all slightly higher. A possible explanation of the discrepancy is given in a previously published paper by the author[62], included in Appendix E. Also discussed in that paper is the anomalous curvature of the plots for reverse voltages below 200 mV which is equivalent to a decreasing value of $I_S = \frac{I_m}{\exp(qV/kT) - 1}$. This corresponds to the theoretically predicted decrease in $A^{**} = \frac{A^* f_p f_n}{1 + v_s/v_d}$ at low internal electric fields, and is evidence for the validity of the thermionic-diffusion theory rather than the thermionic-emission theory. The reverse current-voltage characteristics of the diodes formed on the thin epitaxial layers (D10, D11) were not as close to the theoretical predictions as the characteristics of the diodes discussed above. Figure 36 shows a comparison of three typical diodes from slices D10, D11, and D12. D10AS$_1$ had a lower reverse current near zero bias corresponding to the lower saturation current in the forward direction (see Figure 34). The saturation current rapidly increased with reverse bias, which would be expected if the diffusion limitation on current flow were being eased. Eventually for reverse biases greater than about 200 mV the epitaxial region would be completely depleted (see Section 5.1.4 (b)). As soon as the depletion region reached the substrate, an increase in the generation

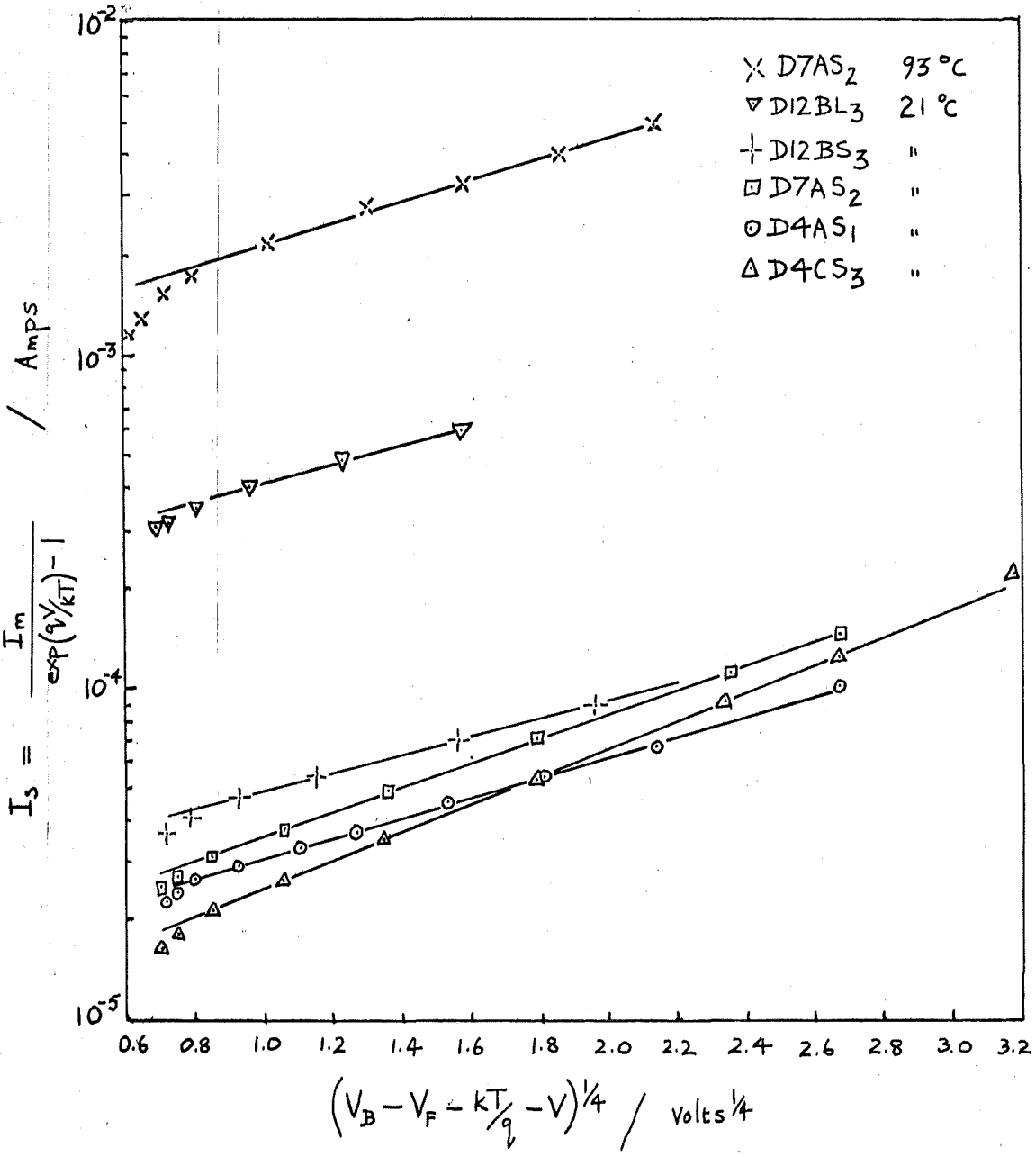


Figure 35 Reverse current-voltage characteristics, showing the linear relationship between I_S and $(V_B - V_F - {}^{kT}/_{q} - V)^{\frac{1}{4}}$. The voltage axis corresponds to reverse bias from zero to 100 volts.

TABLE 8 Comparison of experimental slopes of reverse current-voltage characteristics plotted as ln I_R against $(V_B - V_F - V - {}^{kT}/_{q})^{\frac{1}{4}}$ with the theoretical value ${}^{q}/_{kT}\left[\frac{q^3 N_D}{8\pi^2 \epsilon_{si}{}^3}\right]^{\frac{1}{4}}$ assuming image force lowering is the dominant mechanism.

Diode Number	Experimental Slope volts$^{-\frac{1}{4}}$	Theoretical volts$^{-\frac{1}{4}}$
21°C		
$D4AS_1$	0.70 ± .02	0.56
$D4CS_3$	0.97 ± .02	"
$D7AS_2$	0.84 ± .02	"
$D8AL_4$	0.63 ± .04	"
$D8AS_2$	0.67 ± .03	"
$D12BL_3$	0.75 ± .03	"
$D12BS_3$	0.64 ± .04	"
$D11AL_3$	0.91 ± .05	0.76
$D11AS_4$	1.02 ± .04	"
93°C		
$D4AS_1$	0.70 ± .03	0.45
$D7AS_2$	0.72 ± .03	"

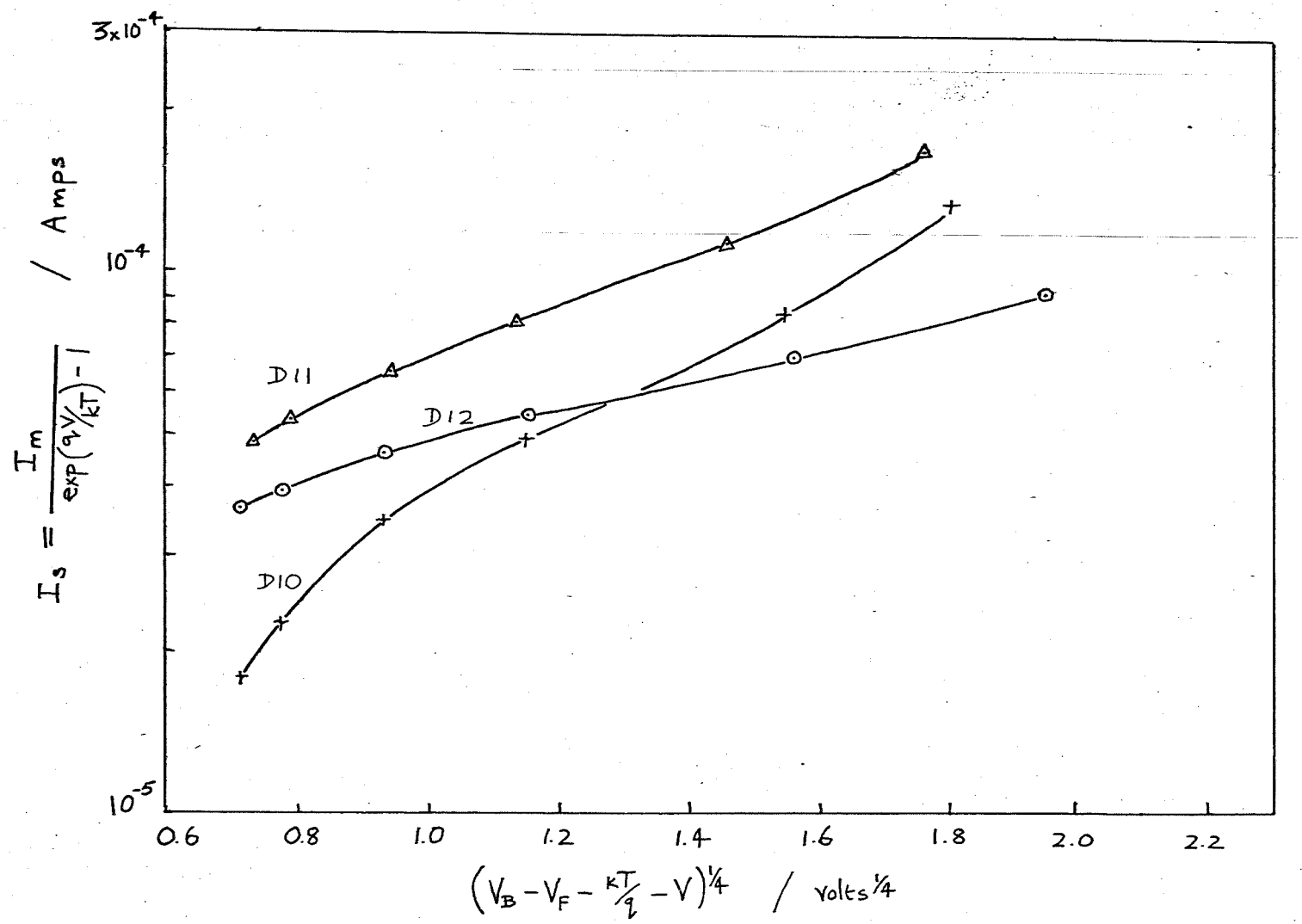


Figure 36 Comparison of reverse current-voltage characteristics for typical diodes from slices D11, D12, and D10, with impurity concentrations 3 x $10^{21}m^{-3}$, 9 x $10^{20}m^{-3}$, and 2 x $10^{20}m^{-3}$ respectively.

current would be expected[22] as the carrier lifetime in the heavily doped substrate would be very short in comparison with the lightly doped epitaxial region. The same comments apply to diodes on slice D11 which had a higher impurity concentration in the epitaxial layer so that it would be fully depleted at about 6 V reverse bias.

5.1.7 Diode AC Resistance

The diode AC resistance was measured for currents between 50 μA and 20 mA. As discussed in Section 4.2, the diode AC Resistance should follow the relationship

$$R_{AC} = R_{ES} + \frac{nkT}{q\,(I_m + I_S)}$$

as long as n is close to unity. If n and the saturation current I_S can be treated as constants, then the experimental plot of R_{AC} against $(I_m + I_S)^{-1}$ should be a straight line of slope $\frac{nkT}{q}$ and intercept R_{ES} on the y axis. Typical experimental plots for large diodes from slices D10, D11 and D12 are shown in Figure 37.

The results for the diodes on slice D11 ($N_D = 3 \times 10^{21}\ m^{-3}$) followed the relationship given above with a constant n value of 1.01 as the plot was linear over the whole range of measured current. The n values agreed well with those calculated from current-voltage measurements (see Table 7). The n values for diodes from slice D12 ($N_D = 9 \times 10^{20}\ m^{-3}$) were slightly higher but the plots were still linear. However, the diodes formed on the silicon of impurity concentration $N_D = 2 \times 10^{20}\ m^{-3}$ (slice D10) gave slightly non linear plots which suggested that the n value was changing as a function of current. For much of the lower range of current the experimental points could be fitted to a line with slope corresponding to $n = 1.06 \pm .01$.

Figure 38 shows the experimental values of R_{AC} for the smaller

diodes, which, for a given value of $(I_m + I_S)^{-1}$ had a current density of approximately ten times that of the larger diodes. As before, the diodes from the slice D11 gave linear plots with low n values which agreed with the values from current-voltage measurements. The results for diodes from slice D12 corresponded to a much higher n value of 1.06 but the plots were still linear except for slight deviations at the highest currents. These deviations were discussed in the second published paper by the author[69], included in Appendix E. The treatment given there, analysed the results in terms of a varying n value, and also the measurements were extended to much higher current densities than those shown in Figure 38. The experimental plot of R_{AC} against $(I_m + I_S)^{-1}$ for the small diodes from slice D10 was so markedly non linear, that it was only possible to assign a lower limit to the n value. This was also the case for the n value from the current-voltage characteristics (Figure 34) but even so the agreement between the two methods of estimating n was quite good. When the n value is changing rapidly, its estimated value using the different techniques will vary (see Section 6.4.1 (a)) so that the n value formulation becomes inconvenient. It is then somewhat simpler to analyse the results in terms of a varying saturation current I_s (V). In the discussion of results in Chapter 6, both approaches will be used.

The series resistance for diodes with linear plots was found by straightforward extrapolation of the plot to intercept the y axis where $R_{AC} = R_{ES}$. For non linear plots the series resistance could not be accurately determined unless the reason for the non linearity was known. Diode self heating would cause a linear plot at low currents to turn upwards at high current if the temperature rise causing an increase in R_{ES} was dominant, and the best estimate of R_{ES} at the ambient temperature would be given by an extrapolation of the linear

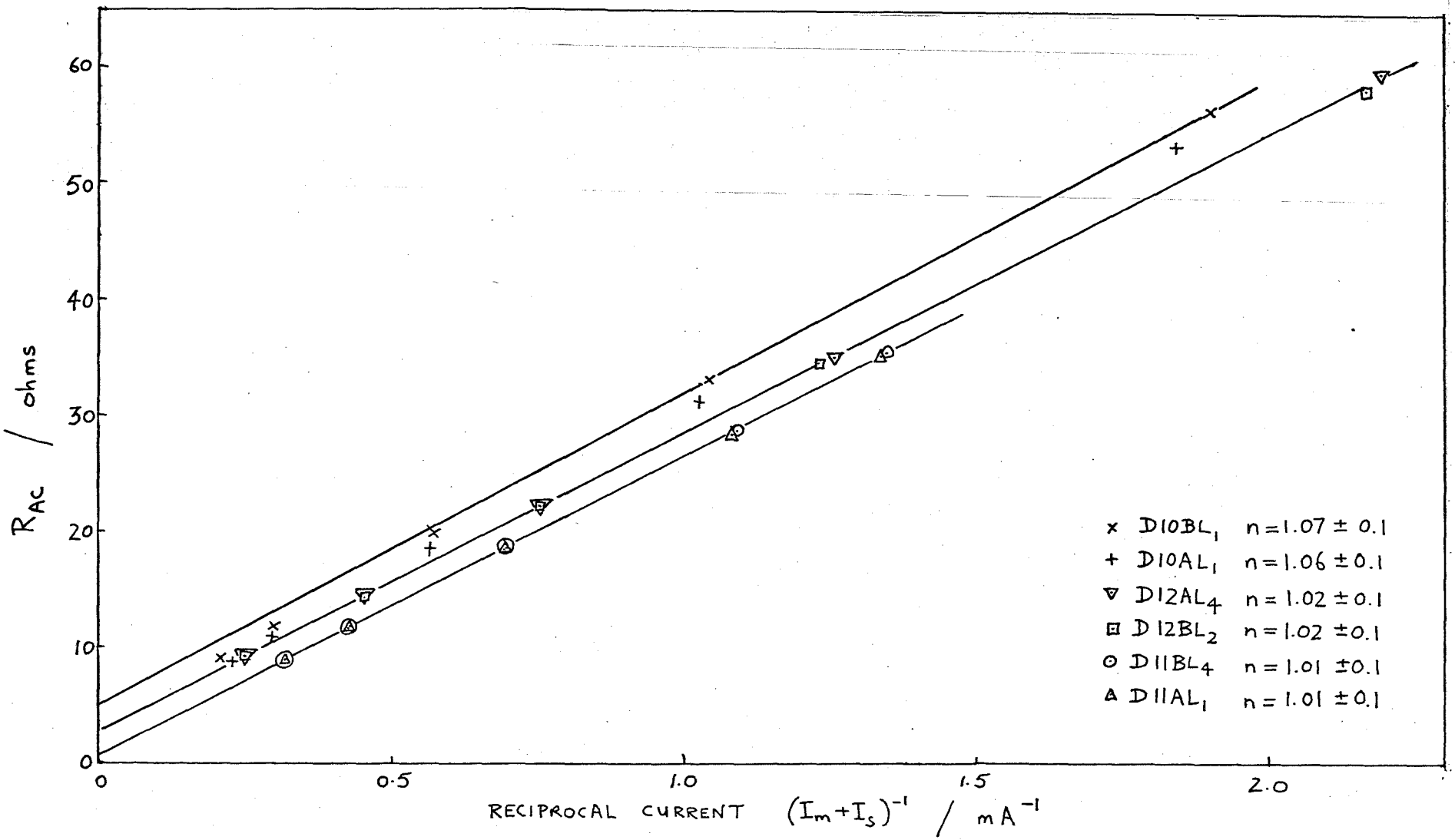


Figure 37 AC Resistance characteristics of 750 μm diameter titanium n-type silicon diodes.

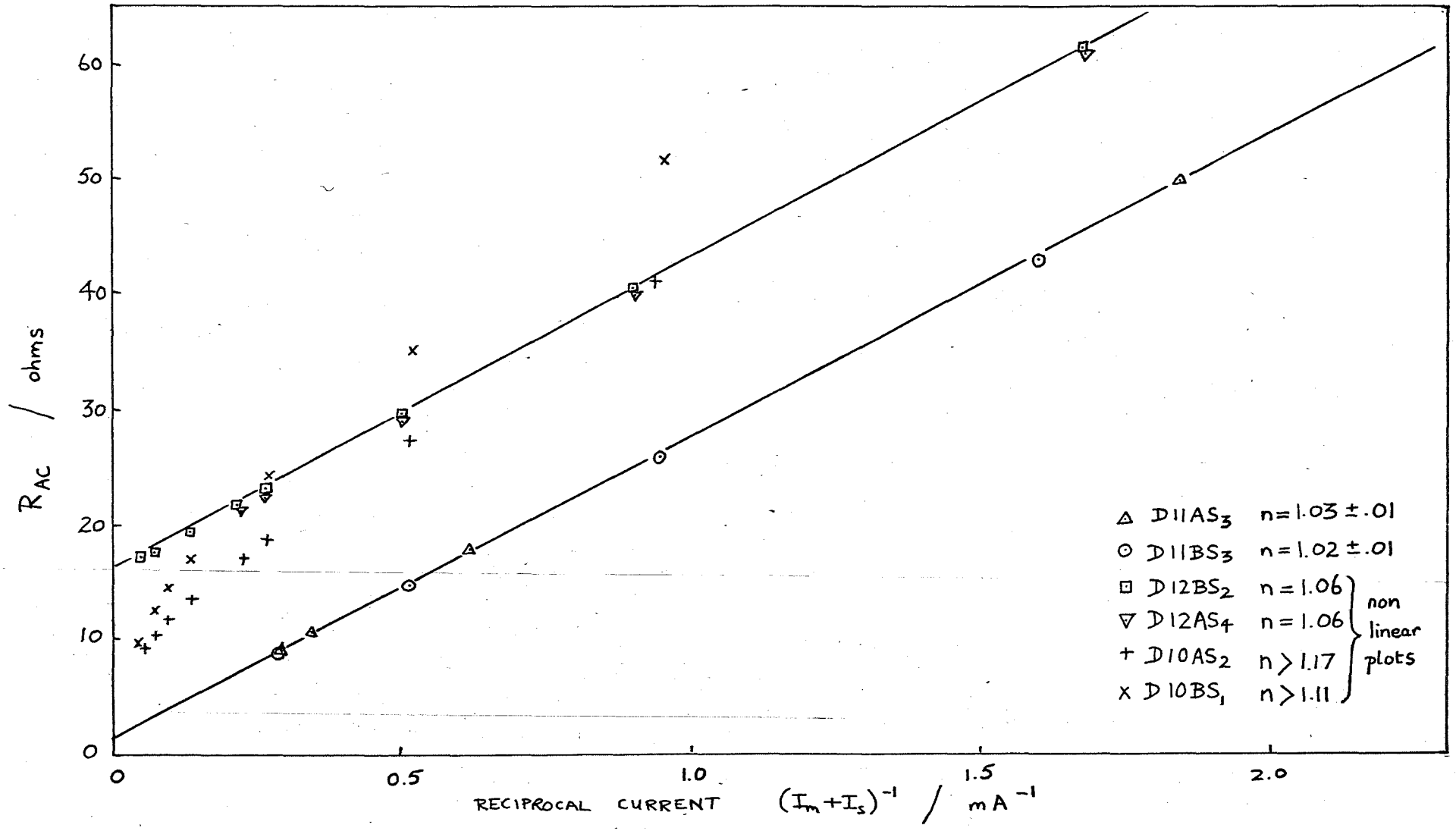


Figure 38 AC Resistance characteristics of 250 μm diameter titanium n-type silicon diodes.

portion of the plot. For plots which were linear at low current and then turned sharply downwards at high current, minority carrier injection would be a possible explanation, and again in that case extrapolation of the linear portion of the plot would give the unmodulated resistance of the epitaxial layer. With diffusion effects, the curvature would be caused by a changing value of n and the true value of R_{ES} would be given by the extrapolation of the curved plot to the y axis. The experimental values of R_{ES} used to calculate the impurity concentrations shown in Table 6 (see Section 5.1.4 (b)) were obtained using this latter technique, as other evidence had suggested that thermionic diffusion effects were dominant in the diodes with non linear plots. In addition to the effects already mentioned, variation of the width of the undepleted epitaxial layer would be significant on lightly doped silicon and would cause variation of the R_{ES} value. Thus it was only for truly linear plots that an unambiguous determination of R_{ES} could be made.

5.2 ALUMINIUM

5.2.1 General

The aluminium n-type silicon Schottky barrier diodes were fabricated with a p-type guard ring diffused into the n-type silicon to a depth of 2 ± 0.5 µm (measured by a conventional lapping and junction staining method[53]). The saturation current of the guard ring diode was of the order of 10^{-16} amps (measured on a similar device without the Schottky contact) so that the current contribution of the guard ring could be neglected in comparison with the aluminium Schottky contact which had a saturation current of the order of 3×10^{-9} amps.

5.2.2 Current-Voltage Characteristics

Figure 39 shows typical current-voltage characteristics of the

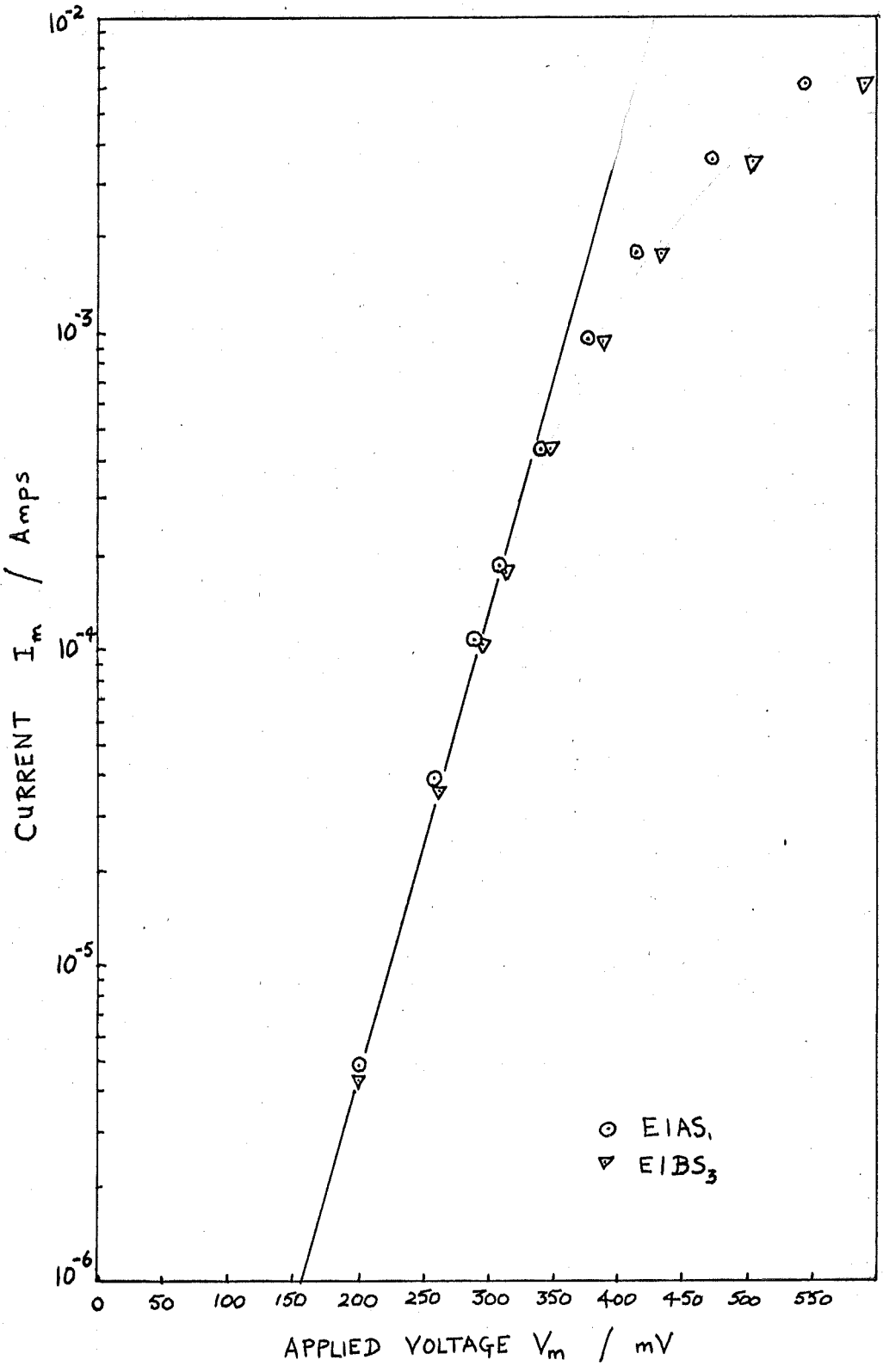


Figure 39 Current-voltage characteristics of 230 μm diameter aluminium n-type silicon diodes.

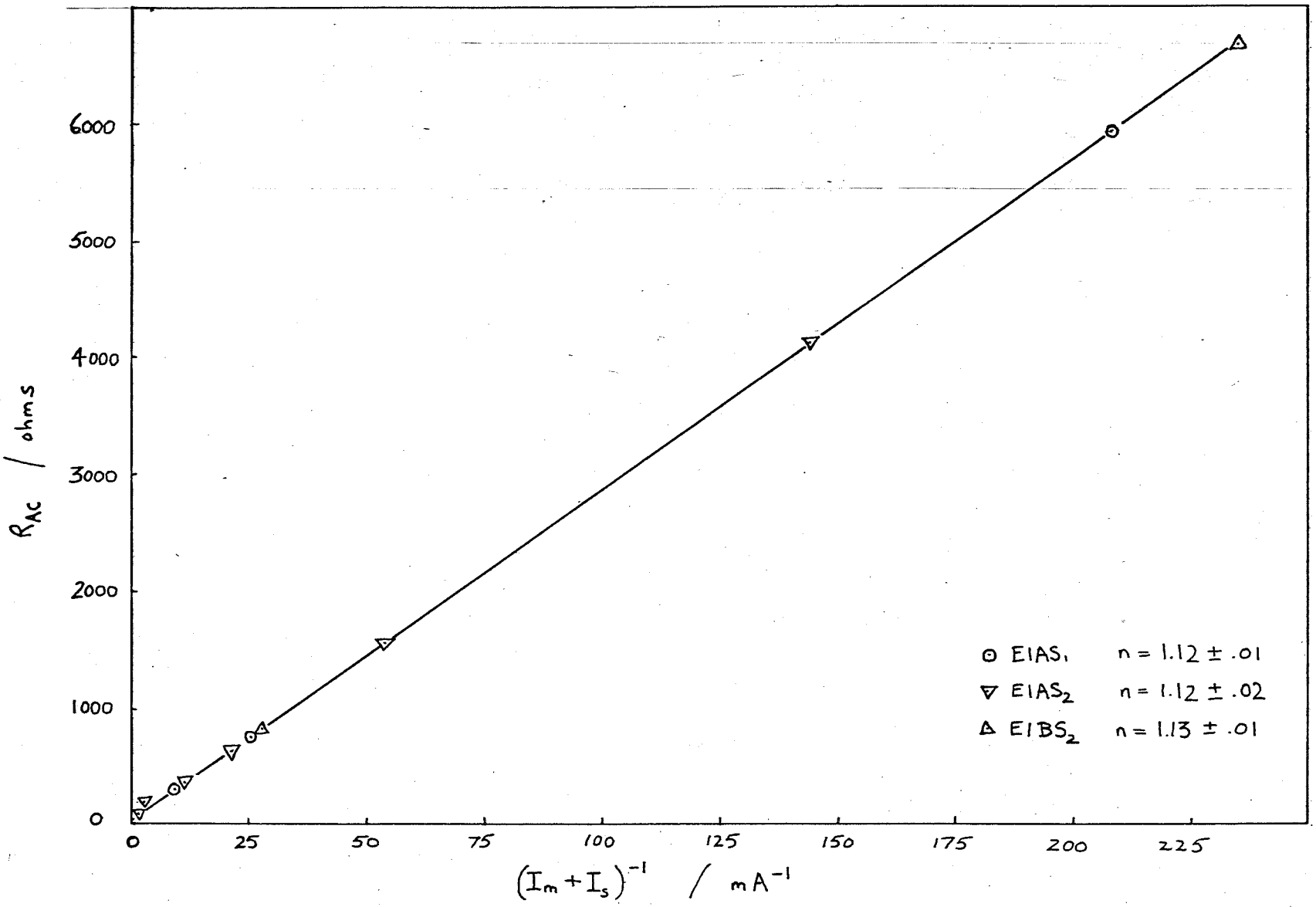


Figure 40 AC Resistance characteristics of 230 μm diameter aluminium n-type silicon diodes.

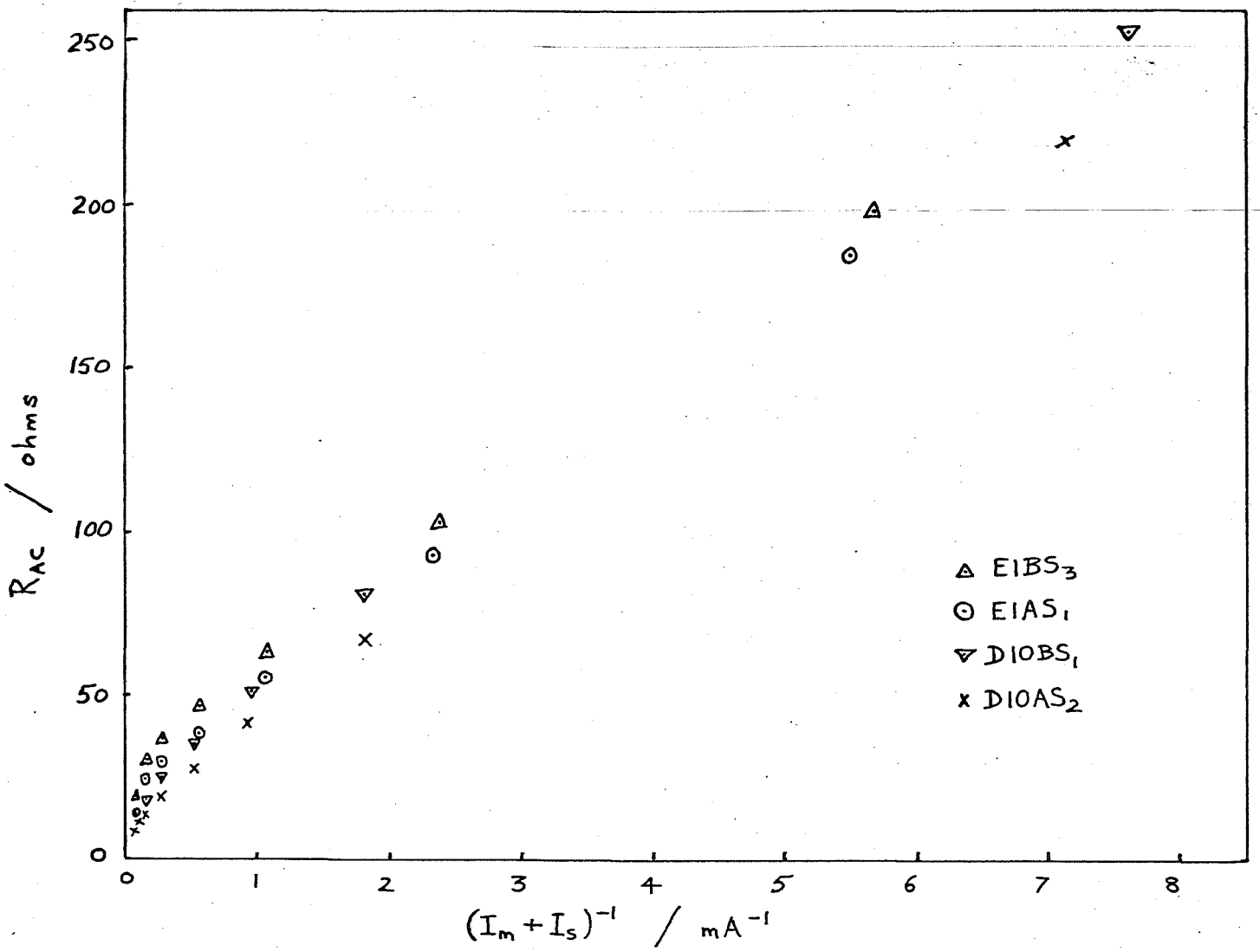


Figure 41 Comparison of AC Resistance characteristics of Ti and Al barriers of similar area at high currents.

aluminium diodes, which can be interpreted in terms of equation (16a) with an n value of 1.15 ± .02. The barrier height V_B calculated from the saturation current I_S using equation (25) was 0.72 ± .02 volt, which agreed closely with the values of 0.71 volt and 0.73 volt obtained by Chino[62] and Yu and Snow[14], on chemically prepared surfaces and was between the values of 0.76 volt on cleaved surfaces and 0.50 volt on chemically cleaned surfaces obtained by Turner and Rhoderick[11].

5.2.3 Diode AC Resistance

The diode AC Resistance was measured for diode currents between 5 μA and 10 mA. The values of R_{AC} were then plotted against $(I_m + I_S)^{-1}$ and as shown in Figure 40, between 5 μA and 0.5 mA, the values followed the linear relationship expected from equation (29) with a constant n value of 1.12 ± .02 which agreed closely with the n value from the current-voltage characteristics. Above 0.5 mA the plots became non linear and Figure 41 shows the experimental results for aluminium diodes at high currents, and for comparison, the results for titanium diodes of similar area from slice D10.

5.3 MAGNESIUM

5.3.1 General

Magnesium n-type silicon Schottky barrier diodes have been reported with barrier heights as low as 0.35 volt[64], and it was hoped that many of the anomalous effects observed on titanium n-type silicon barriers would be even more evident on magnesium barriers because of the lower barrier height. The magnesium barriers fabricated in this investigation, using the procedure described in Chapter 3, had uniform and reproducible characteristics, but the barrier height was much higher than expected.

5.3.2 Current-Voltage Characteristics

Figure 42 shows the experimental characteristics for several diodes, where $\frac{I_m}{1 - e^{-qV/kT}}$ has been plotted on a logarithmic scale against diode Voltage V. The diode voltage was obtained from the measured voltage Vm by correcting for the voltage drop across the series resistance R_{ES} (whose value was obtained from the AC resistance measurements). The linear plots showed that the characteristics could be fitted well by an expression of the form of equation (16a). Table 9 shows the n values and barrier heights V_B deduced from the slope and intercepts of the experimental plots. The spread in barrier height values between 0.53 and 0.57 volt was greater than for the other metals but compared well with previously published results. Crowell, Shore and LaBate[64] obtained values between 0.52 and 0.32 volt for diodes on freshly cleaved surfaces and on surfaces with deliberately grown interfacial layers, which had large but unspecified n values. An early result by Archer and Atalla[65] has been quoted as 0.37 volt (Cowley and Sze[37]), 0.4 volt (Atalla[29]), and 0.35 volt (Ma, Yang and Chang[66]). The uncertainty presumably arose because the original result was given in terms of the apparent barrier height from the semiconductor side ($= V_B - \Delta V_B - V_F$). Ma, Yang and Chang[66] have reported a barrier height of 0.35 volt on n-type silicon, but did not present any current voltage characteristics, and their fabrication procedure included an anneal between 550°C and 640°C which may have caused interdiffusion of the silicon and magnesium as the eutectic temperature[59] is 645°C.

The special precautions taken during fabrication to guard against the formation of intermetallic compounds, and the near ideality of some of the magnesium diodes fabricated in this study (n as low as 1.03) suggests that the higher values of the barrier height reported here, are more reliable than many of the previous results. Further evidence is that a value of 0.55 volt for V_B fits the plot of barrier height

TABLE 9 Experimental parameters for Magnesium n-type silicon Schottky barriers.

Diode	V_B (I - V)	n (I - V)	n (R_{AC})
$F12AS_1$	0.570 ± .005	1.06	1.06
$F18AS_1$	0.550 ± .005	1.10	1.13
$F18AL_1$	0.555 ± .005	1.10	1.10
$F19AS_4$	0.530 ± .005	1.15	1.11
$F19AL_3$	0.545 ± .005	1.03	1.04

Mean 0.556

against work function given in Cowley and Sze's paper[37] much better than the lower values, and Saltich and Terry[32] quote a barrier height of 0.55 volt for magnesium on n-type silicon but do not give a direct reference to the source of their data.

5.3.3 Diode AC Resistance

The experimental values of R_{AC} are shown in Figure 43 plotted against $(I_m + I_S)^{-1}$ for diodes of two sizes. R_{AC} was measured for currents between 20 μA and 5 mA. The n values deduced from the slopes of the plots, all of which were linear, are shown in Table 9. Comparison with the values obtained from the current-voltage measurements showed that although the agreement between the two methods of measurement was good, there was a large variation between diodes which did not appear to be linked to diode size. Edge effects were more likely to be significant for the magnesium diodes, which had a higher barrier than titanium and hence a lower thermionic emission saturation current. If these edge or surface effects were due to a generation/recombination mechanism then the n value contribution would be expected to decrease at higher forward bias[22]. Figure 45 shows that this was the case for the magnesium diodes with high n values, but further discussion will be left until the next chapter.

5.3.4 Capacitance-Voltage Characteristics

The experimental values of $1/C^2$ plotted as a function of diode reverse bias are shown in Figure 44. The plots were linear down to a bias of 30 mV where the parallel conductance of the diode became significant and caused a loss in sensitivity of the balance position. As can be seen from Table 6, the impurity concentration deduced from the slope of the plot, agreed well with the nominal value, and the calculated from the series resistance. The intercept of the plot on the voltage axis gave a value of the built in voltage

$V_D = V_B - V_F - {}^{kT}/_{q}$ from which the barrier height was calculated to be 0.55 ± 0.01 volt.

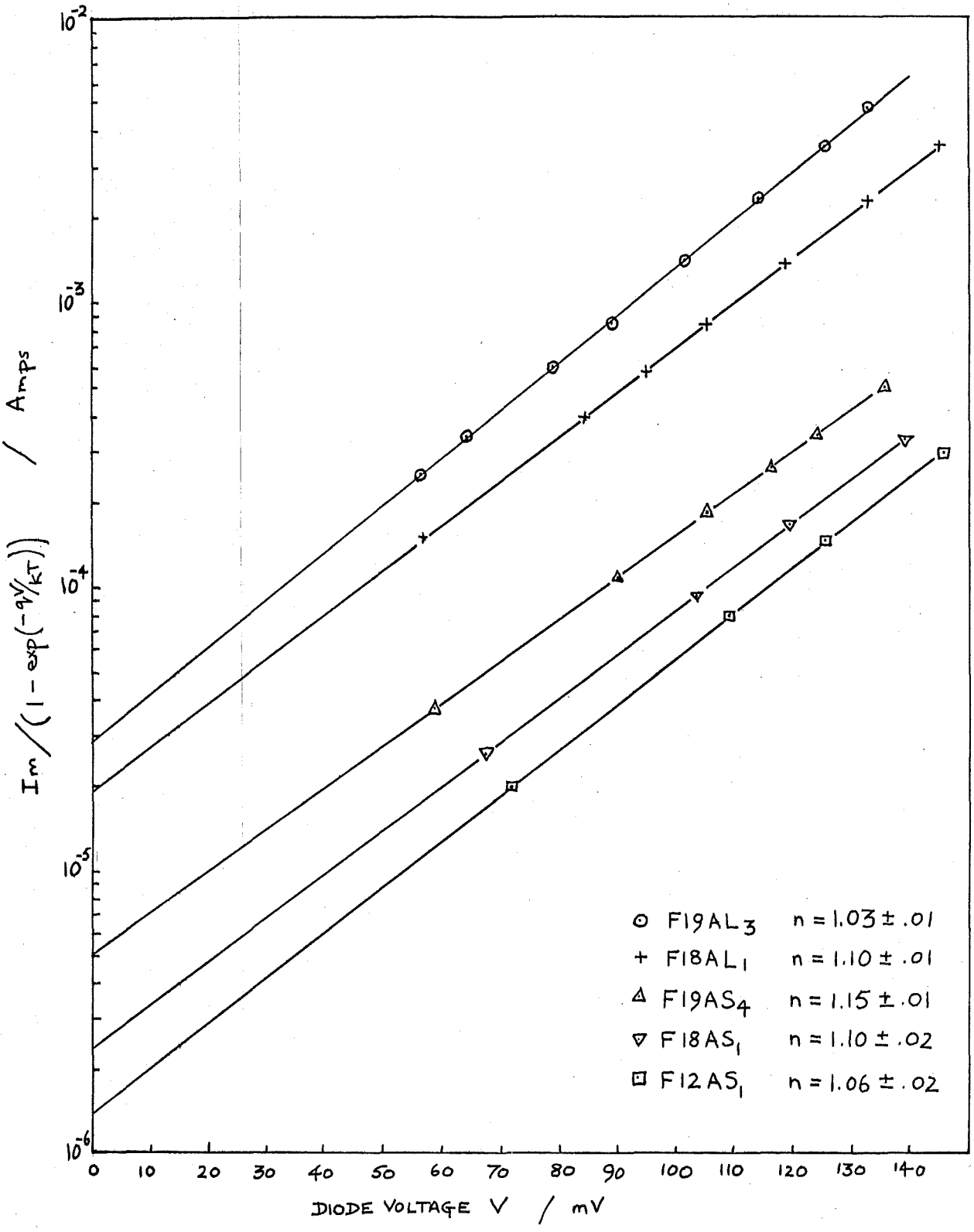


Figure 42 Current-voltage characteristics of 230 μm and 730 μm diameter magnesium n-type silicon diodes.

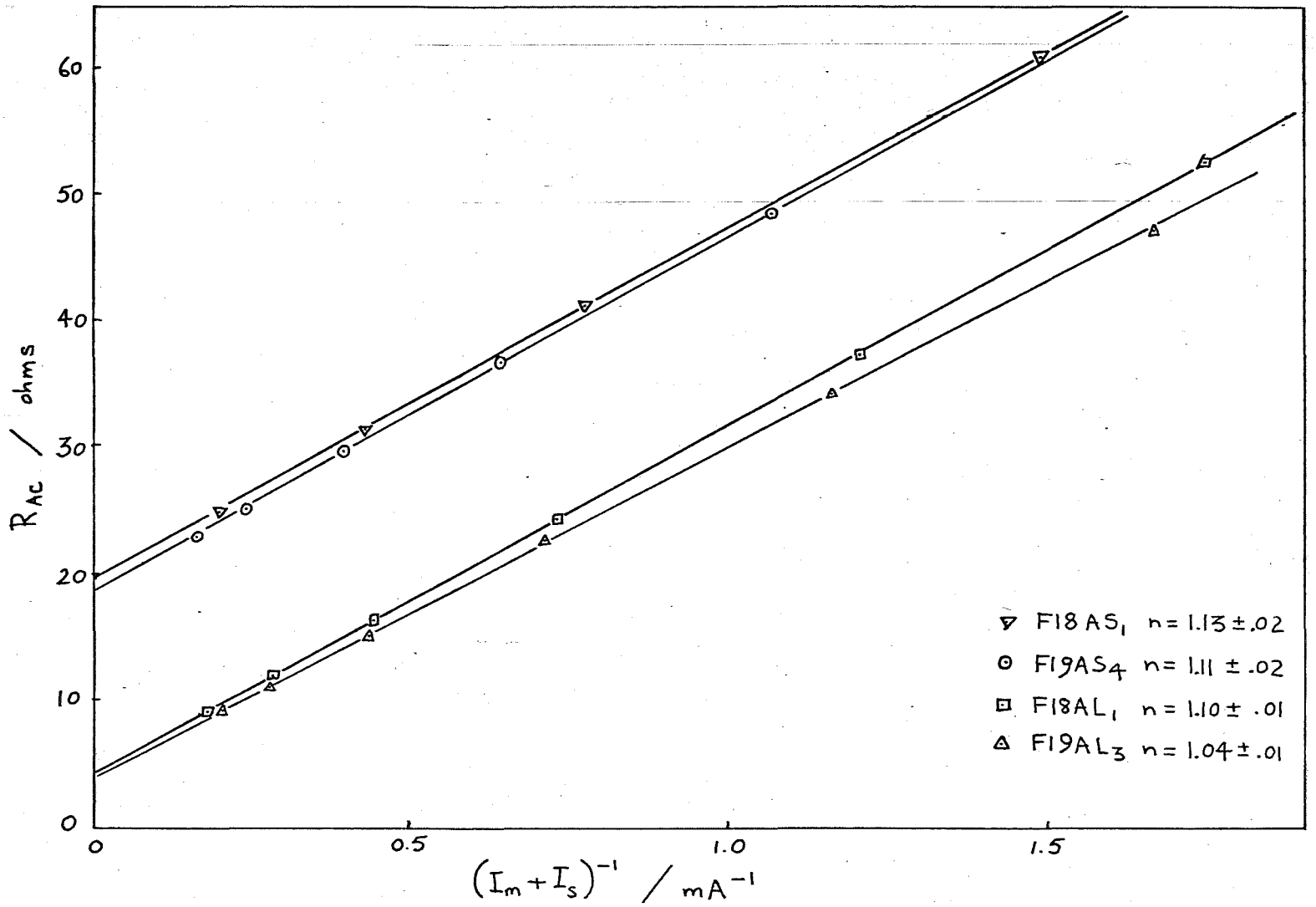


Figure 43 AC Resistance characteristics of 230 μm and 730 μm diameter magnesium n-type silicon diodes.

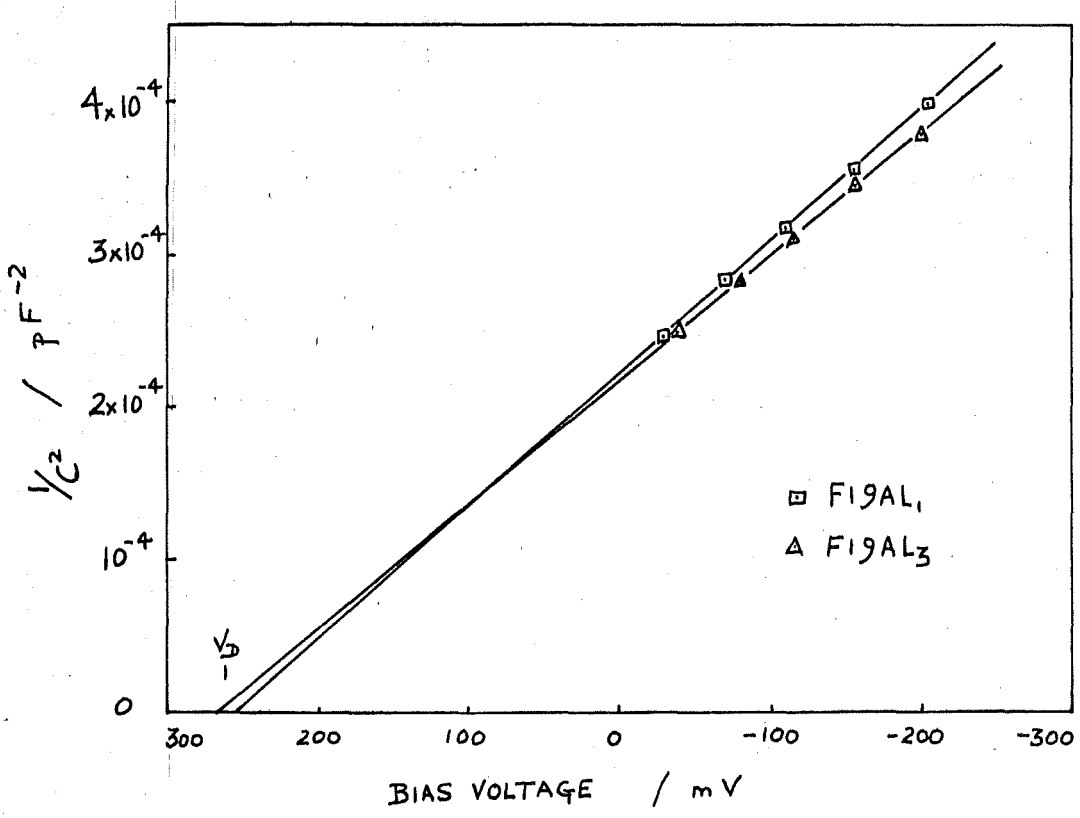


Figure 44 Capacitance-voltage characteristics of 730 μm diameter magnesium n-type silicon diodes.

CHAPTER 6

DISCUSSION OF RESULTS

6.1 GENERAL

Many of the main features of the behaviour of the Schottky barriers investigated in this work have already been explained in terms of the existing theories outlined in Chapter 2. In particular the current-voltage characteristics have been shown to correspond closely to a relationship of the form of equation (16a)

$$I = I_S \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right]$$

with n values in the range 1.01 to 2. However, these n values are equivalent to deviations in the diode voltage of between 1 and 100% from that predicted by the thermionic-emission model, and in this chapter a closer match between experiment and theory will be attempted.

6.2 INITIAL DISCUSSION OF RESULTS FOR TITANIUM BARRIERS

6.2.1 Comparison of Experimental and Theoretical n values

Table 10 shows the theoretical contributions to non-ideality from image force lowering, thermionic-diffusion, tunnelling and interface effects, expressed in terms of n - 1. These have been calculated using the relationships given below, at two values of band bending and three values of impurity concentration.

For image force lowering[30]

$$n = \left(1 + \frac{d\,V_B}{d\,V}\right)^{-1} \quad \text{where} \quad \frac{d\,V_B}{d\,V} = -\frac{\Delta V_B}{4\,(V_B - V_F - kT/q - V)}$$

For the thermionic-diffusion theory[24], equation (A16) from Appendix A gives

$$n = \frac{\delta_V + D(\beta^{1/2})}{\delta_V + 0.5\beta^{-1/2}}$$

The contributions to n - 1 from tunnelling effects have been taken from the graphical presentation of results given by Chang and Sze[18].

The contribution to n - 1 from interface effects depends not only on the material and thickness of the interfacial layer, but also on D_S the density of surface states[35]. Assuming $D_S = 0$ and an oxide thickness $\delta = 1.5$nm, which was a possible upper limit[44], for the surface preparation given in Chapter 3,

$n = 1 + \frac{\delta \epsilon_{si}}{\lambda \epsilon_{ox}}$ which varies as a function of voltage and impurity concentration because of the presence of the factor λ, the depletion region width. If D_S is not zero then an additional contribution to n would be expected, which would be similar for slices with identical surface preparation.

When there is more than one contribution to the non-ideality, it will be assumed that the composite value of n - 1 is just the arithmetic sum of all the individual contributions, as long as these are small.

It should be noted that all the mechanisms, except thermionic-diffusion, predict n values which increase with increasing impurity concentration which is contrary to the experimental results shown in Table 7. All the contributions to the n values are voltage dependent and, except for surface effects discussed below, tend to increase as the band bending β decreases.

The experimental value of n = 1.02 $\pm$ .01 for diodes on slice D11 was lower than the sum of all the possible contributions given in Table 10, so that it was unlikely that there was a significant contribution from interface effects. The sum of the image force lowering (IFL) and thermionic-diffusion (TD) contributions appropriate to these diodes was n = 1.03.

Diodes on slice D12 had n values in the range 1.05 $\pm$ .03 which was slightly higher than the value of n = 1.04 given by the sum of IFL

TABLE 10 Theoretical contributions to non-ideality expressed as n - 1

Slice No.	D10		D12		D11	
Impurity Concentration	2×10^{20} m^{-3}		9×10^{20} m^{-3}		3×10^{21} m^{-3}	
Band Bending in kT/q units	6.8 (V=0)	2.0	8.3 (V=0)	2.0	9.6 (V=0)	2.0
n - 1 Image Force Lowering	.010	.024	.011	.035	.014	.048
n - 1 Thermionic-Diffusion	.057	.209	.026	.152	.013	.109
n - 1 Interfacial Oxide Layer δ=15 Å, D_S=0	.004	.008	.008	.016	.014	.029
Tunnelling n - 1	< 0.01		< 0.01		≈ 0.01	

and TD contributions.

The n values for the diodes on slice D10 were more widely spread but for the larger diodes n = 1.11 ± .05 which was greater than the value of n = 1.07 given by the sum of the IFL and TD contributions. However, the most important feature of both the experimental and theoretical results for this material was that the n value was increasing rapidly as a function of voltage applied to the diode.

One contribution to non-ideality which has been neglected so far, is that from surface effects[22]. Although generation and recombination currents can result in n values as high as two, their contribution decreases as the diode is biased further into the forward direction and the thermionic-emission currents dominate. The experimental results discussed in Sections 6.5 and 6.6 show that for the titanium silicon diodes the n values increased as the diodes were further forward biased, so that it was unlikely that surface effects were making a significant contribution to the non-ideality. This was confirmed by the reverse current-voltage characteristics (Section 5.1.6) which were dominated by thermionic-emission effects. However, later measurements on aluminium and magnesium barriers (see Section 6.3.2) showed that in some cases surface effects could be important.

6.2.2 Comparison of Saturation Currents

Figures 33 and 34 show that for the diodes from the slices of different impurity concentration, there was a corresponding change in the saturation current values I_S (V = 0) given by the intercepts on the current axis.

From equation (A12) of Appendix A

$$J_s = \frac{f_p f_q \, q \, N_c \, v_{co}}{1 + D/\delta_v} \exp\left[-\frac{q}{kT}\left(V_B - \Delta V_B\right)\right]$$

$$= \frac{\exp\left(\frac{q\Delta V_B}{kT}\right)}{1 + D/\delta_v} \left[f_p f_q q N_c v_{co} \exp\left(\frac{-q V_B}{kT}\right) \right]$$

so if variations in f_p f_q can be neglected, the expression in the square brackets can be taken as equal for all three impurity concentrations. In this case the saturation currents should be in the same ratio as $\frac{\exp\left(\frac{q\Delta V_B}{kT}\right)}{1 + \frac{D}{\delta_v}}$ Table 11 shows the theoretical values of this expression together with the experimental results for large and small diodes on each of the three silicon slices of different impurity concentration. The agreement was good and suggested that the model used to derive equation (A12), which included image force effects and thermionic-diffusion, adequately described the experimental behaviour. The effect of variations in f_p f_q would be to reduce the saturation current at low internal electric fields (low β) and would be most significant for the diodes on silicon of lowest impurity concentration.

Table 12 lists the experimentally measured and theoretically calculated values of the same parameters at a forward bias of 120 mV, and again the agreement was good although the experimental value for the lightly doped silicon was low. This may have been due to the reduction in f_p f_q at low internal electric field discussed above.

6.2.3 Preliminary Conclusions

The main features of the non-ideality of the titanium n-type silicon diodes have been explained in terms of a model where thermionic diffusion and image force lowering effects are dominant. Alternative models have been rejected either because they predict behaviour which had the wrong dependence on impurity concentration (tunnelling or interfacial layer effects) or because they predict behaviour which had the wrong dependence on bias voltage (surface effects).

In order to check these conclusions, the analysis of the results is

TABLE 11 Diode model parameters, and a comparison of experimental saturation currents with the theoretical model predictions at zero bias, for three impurity concentrations.

Parameter \ Slice	D10	D12	D11
δ_v	0.16	0.35	0.63
V_F volts	0.301	0.269	0.232
β	6.8	8.1	9.6
$1 + D/\delta_v$	2.33	1.53	1.27
ΔV_B mV	6.4	9.9	14.0
Normalised Ratio $\dfrac{\exp\left(\frac{q\Delta V_B}{kT}\right)}{1 + D/\delta_v}$	0.41	0.70	1
Experimental Ratio of I_S Values — small diodes	0.36	0.75	1
Experimental Ratio of I_S Values — large diodes	0.34	0.73	1

TABLE 12 As Table 11, but at a forward bias of 120 mV .

Parameter \ Slice	D10	D12	D11
β	2.1	3.4	4.8
$1 + D/\delta_v$	3.76	1.95	1.42
ΔV_B mV	4.8	7.9	11.7
Normalised Ratio $\dfrac{\exp\left(\frac{q\Delta V_B}{kT}\right)}{1 + D/\delta_v}$	0.29	0.63	1
Experimental Ratio of I_S Values — small diodes	0.20	0.61	1
Experimental Ratio of I_S Values — large diodes	0.21	0.62	1

extended below to include the wider variation of parameters which was carried out in the experimental programme. Thus far, only the theoretical predictions for variation of impurity concentration N_D have been compared with experiment. In the next section the effect of changes in barrier height V_B is checked by analysing the results for aluminium and magnesium barriers, and then the analysis is extended to higher current densities. This enables the experimental dependence of the n value and the saturation current I_S on band bending β to be compared with the theoretical predictions.

6.3 VARIATION OF BARRIER METAL

6.3.1 Theoretical Predictions

In the thermionic-diffusion theory, the only parameter which is dependent upon changes in the barrier height is the band bending $\beta = \frac{q}{kT} (V_B - V_F - {}^{kT}/_{q} - V)$. Using the experimentally determined V_B values for titanium, magnesium and aluminium of 0.50, 0.55 and 0.72 volts respectively, the corresponding values of β at zero applied bias are 8.3, 10.2, and 16.9.

For a given value of band bending, the thermionic-diffusion theory predicts identical behaviour for all three metal silicon barriers, (all other parameters such as N_D being equal) although the applied voltage needed to obtain a given band bending will vary widely. For example a band bending of 5 (kT/q units) results from applied diode voltages of 83 mV, 133 mV and 303 mV on titanium, magnesium and aluminium respectively.

6.3.2 Comparison with Experiment

Figure 45 shows the experimental n values for the different metal barriers plotted as function of band bending. The n values were obtained from the AC resistance measurements. The incremental slope

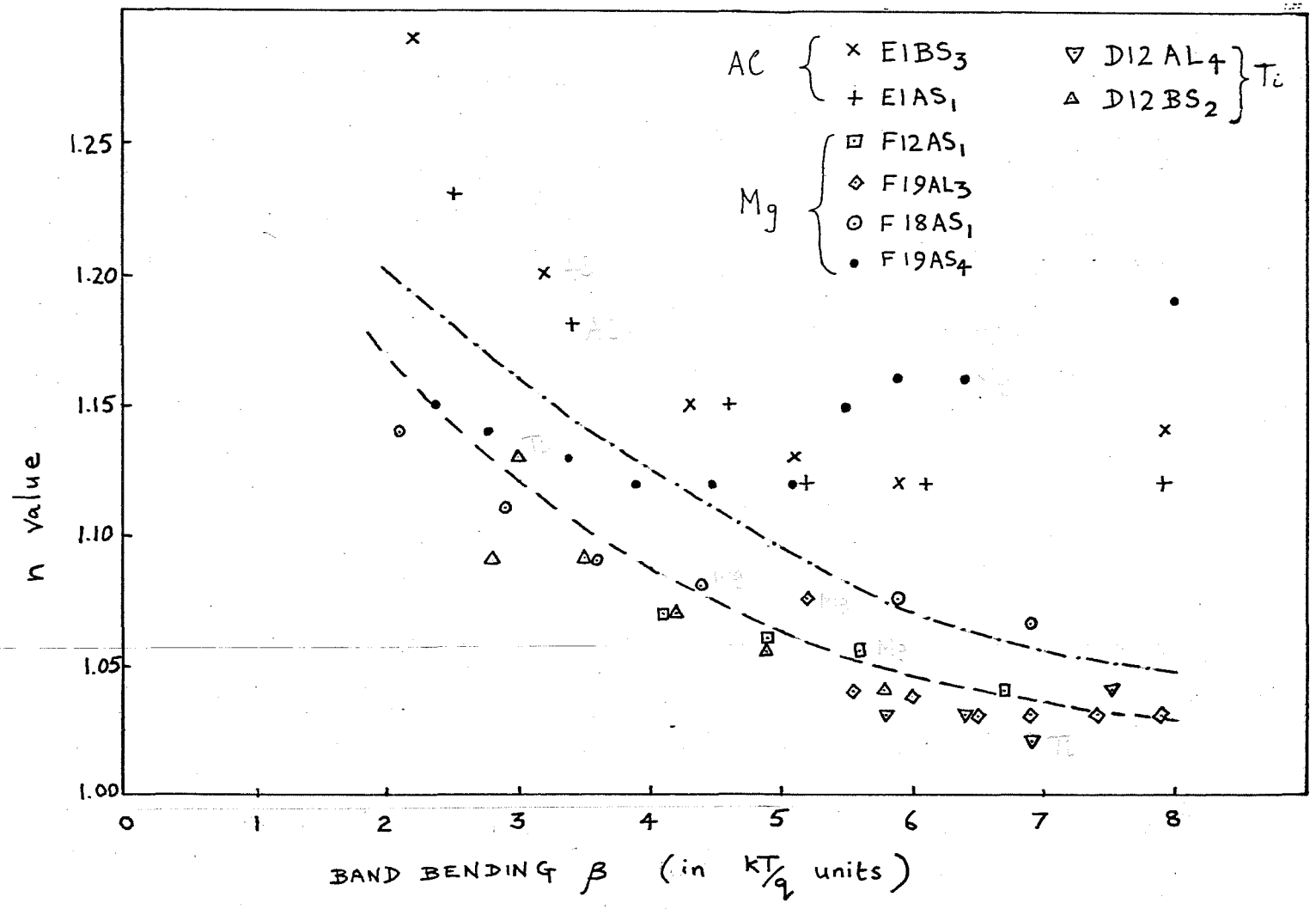


Figure 45 Comparison of n values for aluminium, magnesium, and titanium barriers on n-type silicon with the predictions of thermionic-diffusion theory – – – – , and thermionic-diffusion theory + image force effects —·—·—·— .

of the plot of R_{AC} against $(I_E + I_S)^{-1}$ will be approximately $\frac{nkT}{q}$ as long as the n value is constant or only slowly varying (see Section 5.1.7 and equation (29)).

Figure 45 shows that apart from F19AS4, the results were similar over the whole range of band bending for the titanium and magnesium diodes which were fabricated using similar techniques. However, the aluminium diodes, fabricated using the guard ring technique had n values which were higher by about 0.10 but which did show an almost identical upward trend at low values of β .

Although the general upward trend in n value was in agreement with the theoretical values from thermionic-diffusion theory, the detailed agreement was not very good, especially at low β where the n values were changing rapidly. A possible explanation of this discrepancy is given in the following section. The theoretical results in Figure 45 were taken from Figure 54 of Appendix A.

The results for diodes $E1BS_3$ and $F19AS_4$ show that where a high n value was obtained at low forward bias (high β) this tended to decrease slightly before following the general upward trend at low β . This was consistent with a large contribution to the n value from surface effects as discussed in Section 6.2.1.

6.4 FURTHER RESULTS ON TITANIUM BARRIERS AT HIGHER CURRENT DENSITIES

6.4.1 Variation of n value as a Function of Band Bending

(a) Methods of Calculating n value

In the analysis of data presented in Section 6.3.2 the n values were calculated from the incremental slope of the diode AC resistance characteristic which was taken as equal to $\frac{nkT}{q}$ if the n value was constant or only changed slowly as a function of diode current. However, the preliminary results shown in Figure 45 suggest that the n value may be varying rapidly at high currents (low β). In this

case the incremental slope of the AC resistance characteristic $\frac{n'kT}{q}$ will not be equal to $\frac{nkT}{q}$ but will involve terms in derivatives of n. It can easily be shown that $n \doteq n' - (I_M + I_S)^{-1} \frac{d\,n}{d(I_m+I_s)^{-1}}$ and since n is tending to increase as $(I_M + I_S)^{-1}$ decreases n will be greater than n'.

Under the conditions described above, an alternative method of calculating the n value is to use the absolute value of R_{AC} at a given current and substitute into equation (B14) derived in Appendix B.

$$R_{AC} = R_S(V,T) + R_L + \frac{nkT}{q(I_m+nI_S)}\left\{1 + \frac{I_m 0.5 R_S(0,T)}{(x_{EP_1} - \lambda(0))}\left[\frac{2\epsilon_{si}}{qN_D(V_B - V_F - \frac{kT}{q} - V)}\right]^{\frac{1}{2}}\right\}$$

Although this expression is expected to be valid for diode currents up to 10 mA, the value of series resistance $R_{ES} = R_S + R_L$ and its voltage dependence must be known or assumed before the expression can be used to calculate n.

The original definition of n (Equation (A13)) was in terms of the slope of the plot of $\ln \left\{\frac{J}{1 - \exp(-qV/kT)}\right\}$ against V, but this does not provide an accurate method of estimating n for the following reasons. Firstly, the measured voltage V_m must be corrected for the effect of series resistance which is difficult at high currents when R_{ES} is a function of voltage and temperature. Secondly, when diode self heating becomes significant, it is clear that the experimental results cannot be compared directly with the predictions of an isothermal theoretical model. This comment also applies to the previous methods of calculating n.

(b) Comparison of Experimental and Theoretical Results

Figure 46 shows a comparison of the n values determined from the experimental data using the three techniques described above, for two values of the parameter R_{ES} for diode $D12BS_2$. Also shown is the apparent value n' from the incremental slope of the AC resistance

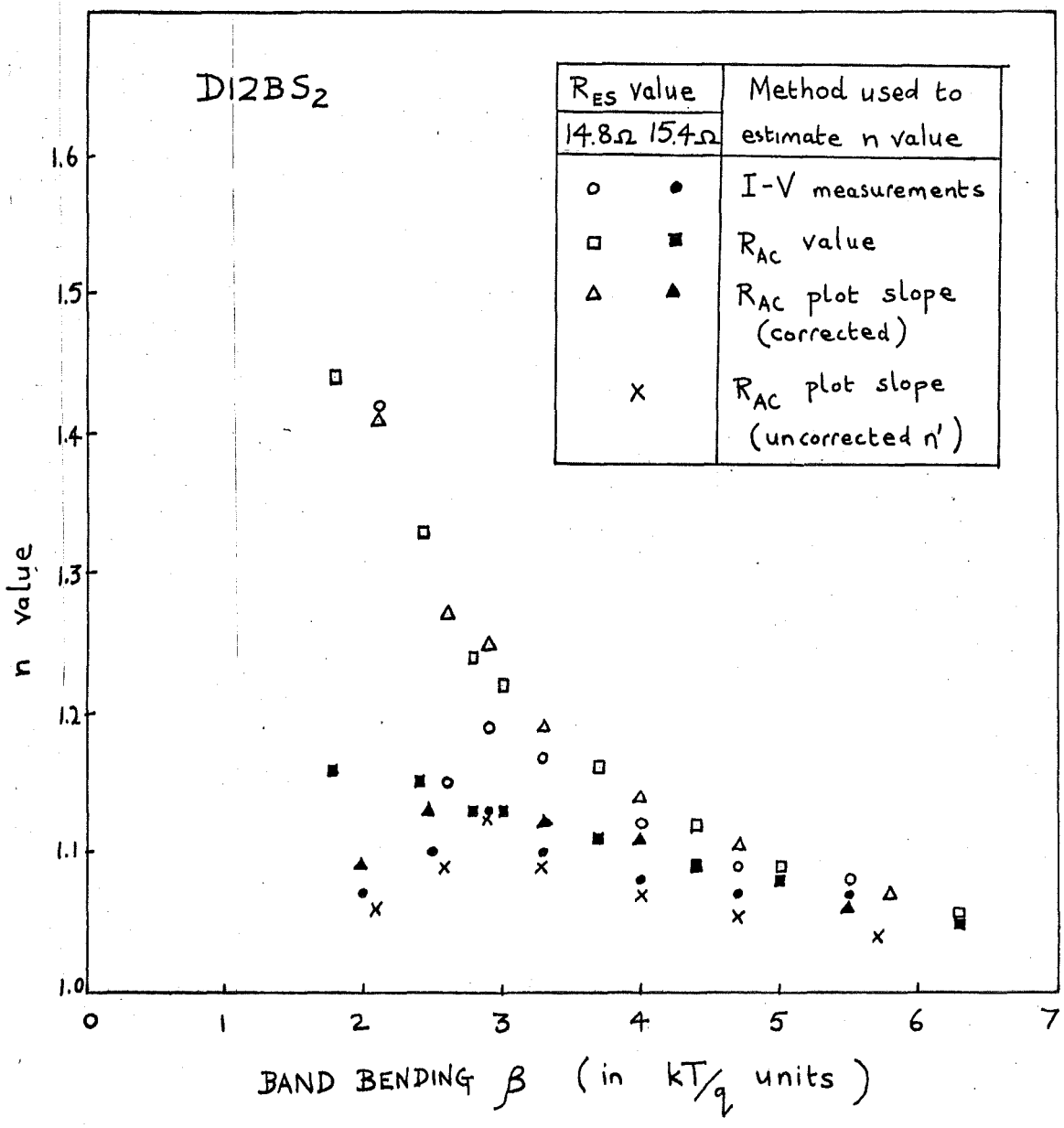


Figure 46 Comparison of n values for diode D12BS$_2$ calculated by three methods, showing the effect of taking different values for R_{ES}.

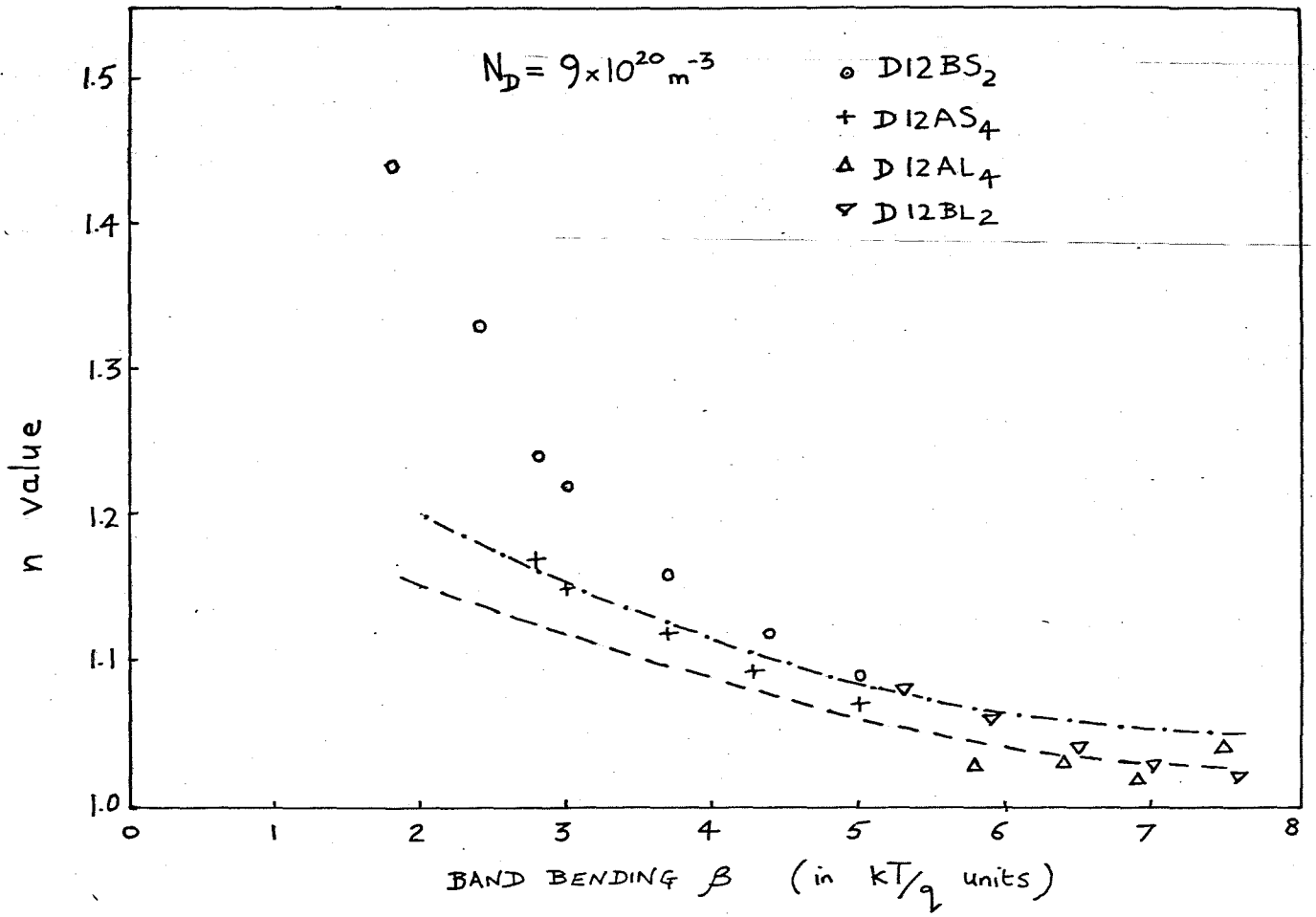


Figure 47 Experimental and theoretical results for n value variation as a function of band bending, for diodes on silicon of impurity concentration $N_D = 9 \times 10^{20} m^{-3}$; ———— thermionic-diffusion theory,

—.—.—. thermionic-diffusion + image force effects.

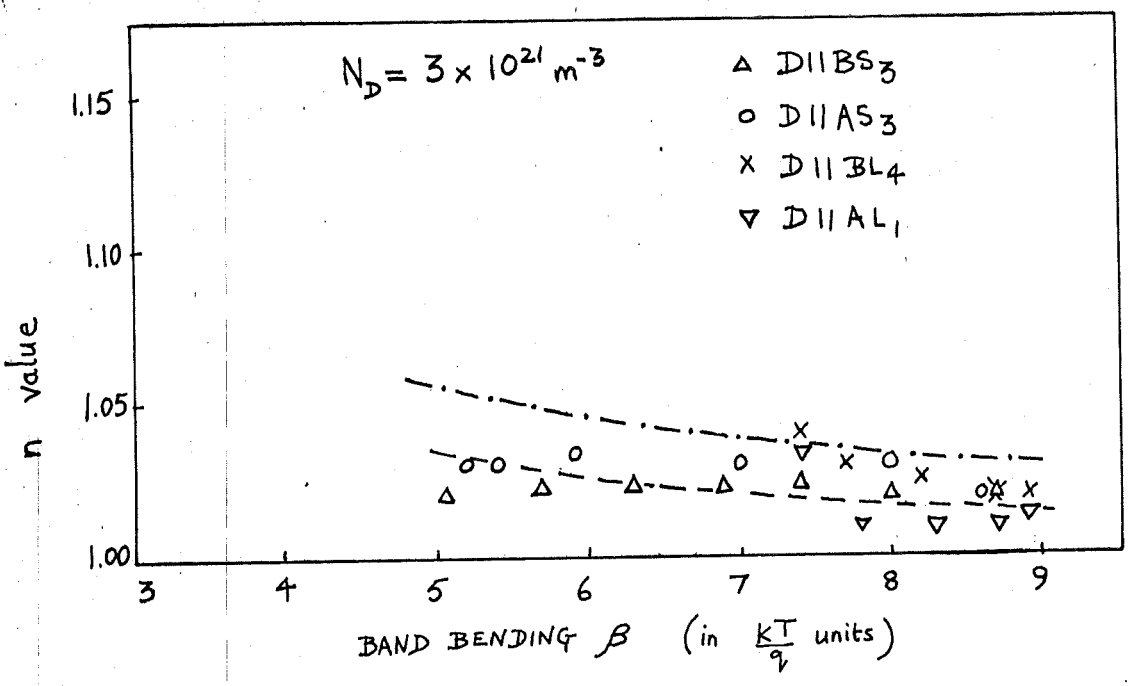


Figure 48 Theoretical and experimental results for n value variation as a function of band bending, for diodes on silicon of impurity concentration $N_D = 3 \times 10^{21} m^{-3}$: ---- thermionic-diffusion theory, -.-.-.- thermionic-diffusion + image force effects.

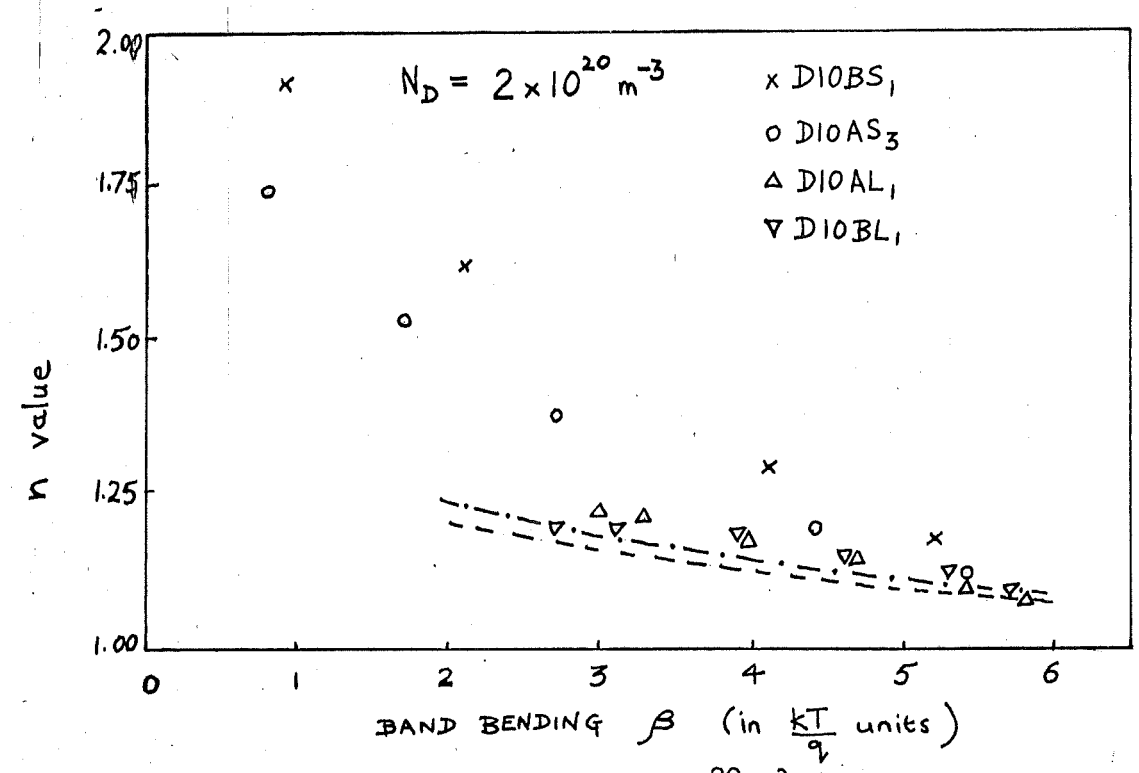


Figure 49 As above figure, with $N_D = 2 \times 10^{20} m^{-3}$.

characteristic. The agreement between the n values determined by the different techniques was better for $R_{ES} = 14.8\,\Omega$ than for $R_{ES} = 15.4\,\Omega$ but the main feature was the critical dependence of n on the value of R_{ES} at low values of β although the n value was almost independent of R_{ES} at higher β.

The conclusion that n' was in general less than n would be consistent with the results presented in Table 7 and Figure 45. In Table 7 the n' values from diode AC resistance characteristics were lower than those n values from current-voltage characteristics, and in Figure 45 some of the n' values were lower than the theoretical predictions.

Figures 47, 48 and 49 show the variation of n value plotted as a function of β for diodes fabricated on n-type silicon of the three impurity concentrations used in the experimental study.

For comparison, the theoretical values from the thermionic-diffusion model, with and without the addition of image force effects, are also shown in these figures. The agreement with the experimental results was good for $\beta > 5$, but below this value the n values were generally much higher than those predicted by the theory, and as discussed previously, the n values were increasingly dependent upon the value of the parameter R_{ES}.

6.4.2 Variation of Saturation Current as a Function of Band Bending

(a) Calculation of Saturation Current

Using the estimate of R_{ES} from the diode AC resistance characteristic (or alternatively the value of R_{ES} which gave a good fit to the experimental data using the computer diode simulation model discussed in Section 6.4.3) the measured voltage V_m was corrected to give the voltage across the barrier V. The saturation current was then calculated as $I_S = \dfrac{I_m}{\exp\left(\frac{qV}{kT}\right) - 1}$. Although the value of I_S was dependent upon

the value of R_{ES} it was found that this dependence was not as critical as that of the n value.

The theoretical saturation current values given in Figure 50 represent $\frac{J_S}{J_{TH}(V = 0)}$, where J_{TH} (V = 0) is the saturation current density from thermionic-emission theory including image force lowering ΔV_B at V = 0

$$J_{TH} = \frac{I_{TH}}{S} = A^* T^2 \exp\left[-\frac{q}{kT}\left(V_B - \Delta V_B\right)\right]$$

In order to compare the experimental saturation current (I_S) values with the theoretical predictions, the values of I_S must be normalised by dividing by the value of I_{TH} (V = 0) appropriate to the impurity concentration of the diode. This involves taking a value for V_B, the barrier height, and then calculating ΔV_B in each case. Since the diodes formed on slice D11 had the most nearly ideal characteristics, the saturation current for these diodes was used to calculate I_{TH}.

$$I_{TH}(V=0)\Big|_{D11} = I_S(V=0)\Big|_{D11}\left(1 + D/\delta_V\right) = 0.0566 \text{ mA}$$

and hence

$$I_{TH}(V=0)\Big|_{D10} = I_{TH}(V=0)\Big|_{D11} \exp\left[-\frac{q}{kT}\left(\Delta V_B(V=0)\Big|_{D11} - \Delta V_B(V=0)\Big|_{D10}\right)\right]$$

$$I_{TH}(V=0)\Big|_{D12} = I_{TH}(V=0)\Big|_{D11} \exp\left[-\frac{q}{kT}\left(\Delta V_B(V=0)\Big|_{D11} - \Delta V_B(V=0)\Big|_{D12}\right)\right]$$

This procedure is equivalent to empirically fitting the experimental and theoretical values at V = 0 ($\beta = 9.1$) for diodes from slice D11.

(b) Comparison of Experimental and Theoretical Results

Figure 50 shows the experimental and theoretical values of normalised saturation current plotted as functions of band bending β. The ratio of saturation currents for the diodes on the three silicon slices was in good agreement with the theoretical prediction over most of the range of measurements. For each impurity concentration, the variation of saturation current as a function of β was in general

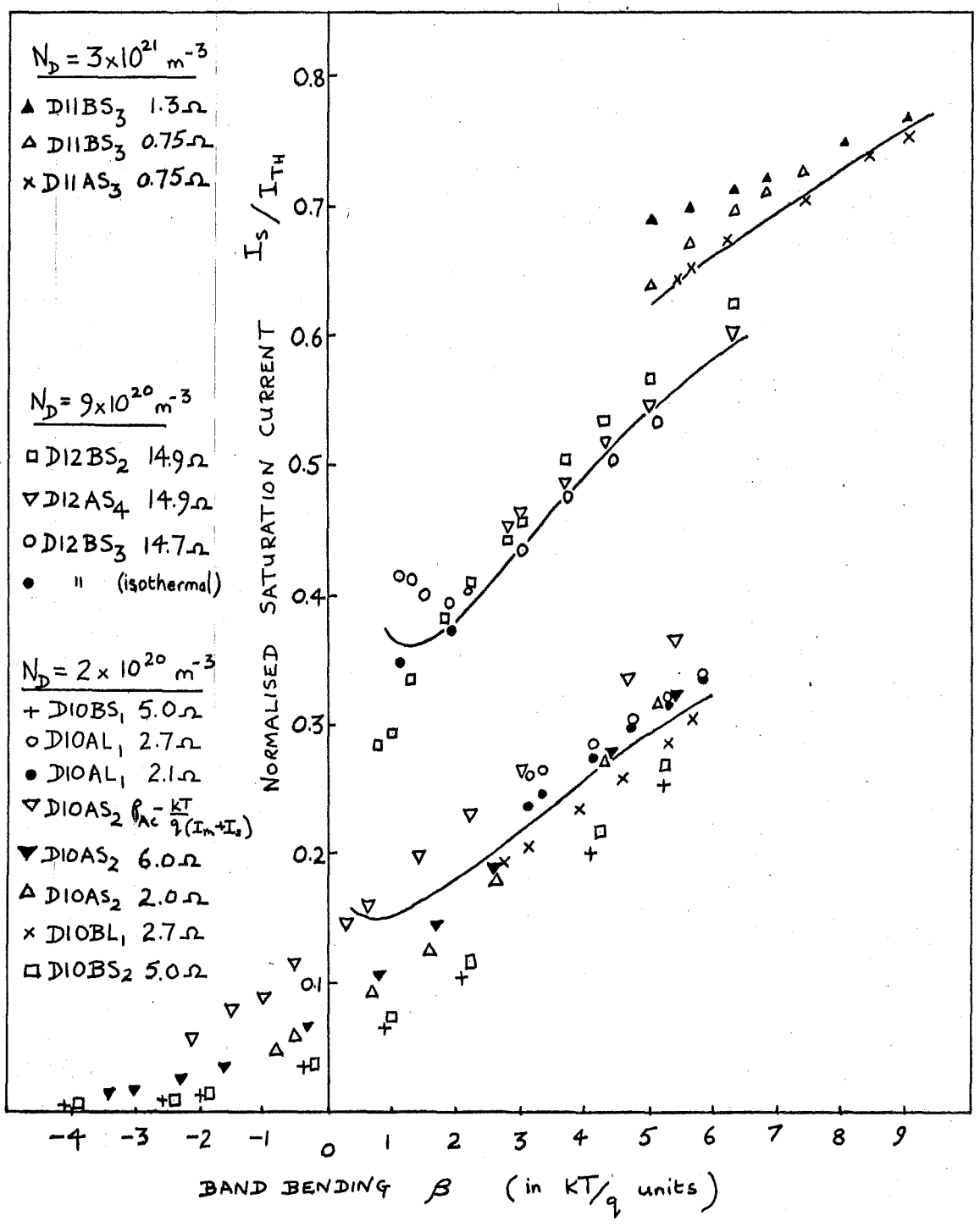


Figure 50 Comparison of experimental results and theoretical predictions for variation of saturation current with band bending. The solid lines represent the predictions of the theoretical model, which includes thermionic-diffusion and image force effects, for each of the three impurity concentrations used (see Fig. 53 Appendix A).

agreement with the predictions of the model based on thermionic-diffusion and image force effects. Although the saturation current values were dependent upon the value of R_{ES} for each diode, the general form of the variation was fairly insensitive to changes in R_{ES}. This is illustrated in Figure 50 by results for some diodes plotted for various values of R_{ES}, all of which showed a similar decrease in saturation current at low β .

The experimental values for diodes formed on the silicon of lowest impurity concentration (D10) extended through the flat band condition ($\beta = 0$) into the region where the theoretical models were no longer valid. The main feature of the experimental results in this region was the continuing decrease in saturation current. The experimental values of saturation current for band bending below $\beta = 2$ could not be compared directly with the predictions of any isothermal theory because the effects of diode self heating were becoming significant. This is illustrated in Figure 50 where the results for diode $D12BS_3$ have been included with and without correction for the effect of diode self heating

6.4.3 Computer Diode Simulation Model

It was found that the comparison of experimental and theoretical results discussed in Section 6.4.1 and 6.4.2 involved a lot of numerical calculations which could easily be processed by a computer. An additional reason for using a computer diode simulation model is given in the following discussion.

As the current density across the barrier increased, the diode behaviour was expected to become more complex because of the possible influence of diode self heating, minority carrier injection, variation of the width of the undepleted epitaxial layer in addition to further restrictions on the current flow caused by diffusion effects. In any given diode, one of these mechanisms may have been dominant at high current, but it was difficult, a priori, to decide which mechanisms to

neglect. The advantage of a computer model was that it could be based on simple theory and then the additional mechanisms could be introduced until there were enough free parameters available that the diode behaviour could be matched by the model over the whole range of experimental measurements. The problems of using such a model have been discussed in detail by Tantraporn[48]. In particular, a close fit between the model and experimental results only shows the theoretical basis is adequate, if the value of the free parameters which give the best fit are physically meaningful.

Table 13 shows the relative effect of some of the high current mechanisms calculated by the computer model given in Appendix C. Also shown are the values of γ, the minority carrier injection ratio calculated using equation (18) of Chapter 2, which are seen to be negligible up to currents of 10 mA. It was suggested in Section 5.1.7 that minority carrier injection could have modulated the resistivity of the epitaxial layer and caused the observed rapid decrease in R_{AC} at high currents. There are two reasons why this explanation was unlikely. Firstly, the theoretical prediction of γ was too low by a factor of between 10^3 and 10^5 to make the level of injection significant at 10 mA. Secondly, as shown in Figure 41, the variation in R_{AC} at high currents was very similar for aluminium and titanium diodes and occurred at almost identical values of β. The theoretical values of γ for these two diodes differed by a factor of 3×10^2 as a result of the difference in barrier heights.

A typical output from the computer diode simulation model is given in Appendix C. For diodes on the silicon of impurity concentration 9×10^{20} m^{-3} and 3×10^{21} m^{-3} the model could match the experimentally measured values of voltage, current and AC Resistance to better than 1% over the whole range of measurement. The model was not able to match the experimental results for currents greater than about 1 mA for the

TABLE 13 Relative effect at three current levels of diode self-heating, minority carrier injection, series resistance modulation, and reduction of saturation current by diffusion effects, for small diodes.

Slice Number	Current mA	ΔT °C	γ	$\frac{R_{ES}}{R_{ES}\ (V=0)}$	$\frac{I_S}{I_S\ (V=0)}$	β
D11	0.1	0.0	1.6×10^{-11}	1.01	0.95	8.8
	1.0	0.0	1.6×10^{-10}	1.04	0.85	6.7
	10	0.3	1.6×10^{-9}	1.07	0.81	4.6
D12	0.1	0.0	2.4×10^{-10}	1.00	0.92	6.9
	1.0	0.1	2.4×10^{-9}	1.01	0.80	4.5
	10	0.8	2.4×10^{-8}	1.03	0.62	1.4
D10	0.1	0.0	10^{-8}	1.56	0.80	4.6
	1.0	0.0	10^{-7}	2.32	0.53	2.1
	10	0.7	10^{-6}	-	-	-ve
E1	0.1	-	3×10^{-6}	-	-	5.6
	1.0	-	3×10^{-5}	-	-	2.9
	10	-	3×10^{-4}	-	-	1.2

diodes on silicon of impurity concentration 2×10^{20} m^{-3} which suggested that the thermionic-diffusion theory was not adequate to describe the behaviour of these diodes below $\beta = 2$.

6.4.4 Limitations of the Theoretical Model

In the discussions of Sections 6.4.2 and 6.4.3 , it was evident that the theoretical model was unable to match the experimental behaviour for band bending $\beta<2$. This section outlines some of the limitations of the theoretical model which explain why this disagreement occurs.

The derivation of thermionic-diffusion theory given in Appendix A, assumed that the shape of the potential barrier was parabolic, a result which followed from the assumption of an abrupt edge to the depletion region and a uniform space charge density. Goodman[46] has shown that the effect of the reserve layer is to reduce the effective band bending by one unit of kT/q . Thus for band bending of the order of two units of kT/q , the effect of the reserve layer is significant and the assumption of parabolic band bending is no longer valid.

The effect of tunnelling and phonon scattering of electrons in the barrier region was included in the terms f_q and f_p used in the model. For internal electric fields $> 10^5$ volt m^{-1}, the variation in $f_p f_q$ is small[40] and the product can be treated as a constant. However, this value of electric field corresponds to β of the order of 0.1 for $N_D = 9 \times 10^{20}$ m^{-3} and 0.5 for $N_D = 2 \times 10^{20}$ m^{-3}, and so the effects of changes in $f_p f_q$ are expected to be increasingly important at lower values of β.

CHAPTER 7

SUMMARY AND CONCLUSIONS

7.1 SUMMARY OF RESULTS

Measurements have been made on titanium, magnesium and aluminium Schottky barrier diodes on n-type silicon, over a wide range of current density such that, in some cases, the diodes were close to the flat band condition $\beta = 0$ (where band bending $\beta = q/kT\ (V_B - V_F - \frac{kT}{q} - V)$)

Most of the diodes showed nearly ideal behaviour at low applied voltages and the current-voltage characteristics could be represented by the relationship

$$I = I_S \exp\left(\frac{qV}{nkT}\right)\left\{1 - \exp\left(\frac{-qV}{kT}\right)\right\}$$

with n values as low as 1.01 . It was concluded that tunnelling, interfacial layer and surface effects were insignificant for such diodes. However, at higher current densities, many of the same diodes exhibited deviations from ideal behaviour, which were equivalent to n values as high as 1.25 , or which could be interpreted in terms of a rapidly decreasing saturation current I_S .

7.2 CONCLUSIONS

The main features of this behaviour can be explained in terms of a thermionic-diffusion model of current transport through the barrier region, which includes the effects of image force lowering of the barrier. The behaviour predicted by this model deviates increasingly from that predicted by the thermionic-emission model as the band bending β and the impurity concentration N_D decrease. The observed characteristics agree with the predictions of the thermionic-diffusion model for band bending in the range $9 > \beta > 2$, but do not

agree for values of β less than 2 .

Previous calculations by Rhoderick[79] show that measurements made on gold n-type silicon barriers ($N_D = 5 \times 10^{21}$ m^{-3}) are in agreement with the thermionic-diffusion theory at $\beta \approx 10$. Cowley[30] and Saltich[31] both obtained n values of 1.03 for titanium n-type silicon diodes of impurity concentrations 5×10^{21} m^{-3} and 5×10^{22} m^{-3} respectively. Cowley's conclusion, that for his diodes an n value of 1.03 could be explained solely in terms of image force lowering effects, is consistent with the results obtained in this study which suggest that the effects of thermionic-diffusion are very small for $N_D > 3 \times 10^{21}$ m^{-3}.

The results obtained in this work suggest that for diodes formed on silicon of impurity concentration between 2×10^{20} m^{-3} and 3×10^{21} m^{-3} , the thermionic-diffusion model is valid between $\beta = 9$ (where its predictions are very close to those of the thermionic-emission model) and $\beta = 2$. This lower limit appears to correspond to the limit discussed by Crowell and Sze[15] , when phonon scattering of electrons between the barrier maximum and the metal becomes dominant. It is suggested that in order to develop a theory valid for β less than 2 , the diffusion analysis will have to be extended beyond the potential energy maximum, instead of using an effective thermionic-emission velocity boundary condition. The analysis will also have to consider the effect of the reserve layer on the shape of the potential variation near the barrier.

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APPENDIX A

THERMIONIC-DIFFUSION THEORY

Derivation of Current-Voltage Relationship

The electron current density through the barrier region is due to a combination of drift and diffusion,

$$J_n = q\left[n(x)\mu_n \mathcal{E} + D_n \frac{\partial n}{\partial x} \right]$$

which can be expressed as

$$J_n = q\, n(x)\mu_n \left(\frac{1}{q} \frac{\partial \phi_n}{\partial x} \right) \qquad \ldots\ldots(A1)$$

where q is the magnitude of the electronic charge, n(x) is the density of conduction electrons at x, μ_n is the electron mobility, $\mathcal{E}$ is the electric field in the depletion region, D_n is the electron diffusion constant, T is the electron temperature which is assumed constant through the barrier and equal to the lattice temperature, $\phi_n(x)$ the electron quasi-Fermi energy or imref and $\psi(x)$ the energy of the semiconductor conduction band are both positive when measured relative to the metal Fermi energy.

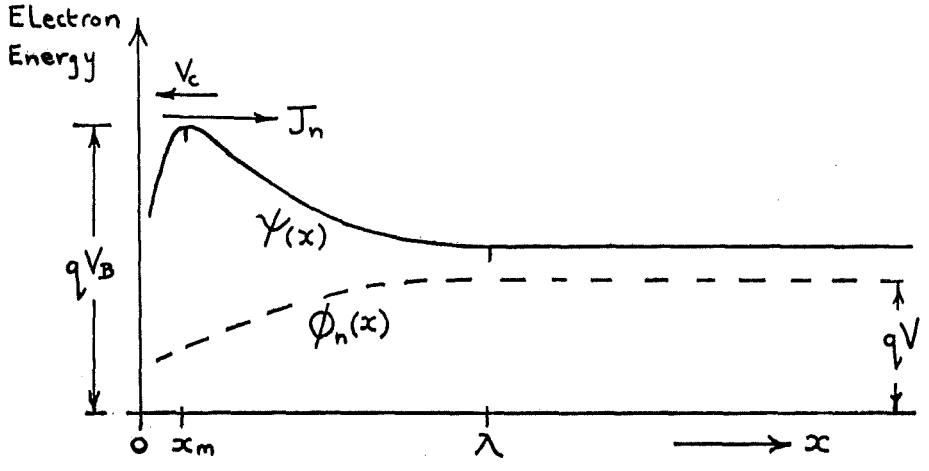


Figure 51 Electron energy levels through the barrier.

$$n(x) = N_c \exp\left[-\left(\frac{\psi(x) - \phi_n(x)}{kT}\right)\right] \qquad \ldots\ldots(A2)$$

Under steady state conditions with no recombination J_n is constant through the barrier, independent of x. The Figure shows the energy levels through the barrier including image force lowering which moves the peak of the barrier from x = 0 to x = x_m. Initially the approximation that the barrier height V_B is independent of the bias voltage V will be made, because the image force lowering effect is small.

In the region between x_m and the metal surface, because the potential energy changes rapidly over a distance comparable with the electron mean free path, equations (A1) and (A2) will not be valid and hence the distribution of carriers cannot be described in terms of an imref or an effective density of states. If this portion of the barrier acts like a sink for electrons, then the current flow can be described in terms of an effective electron collection velocity v_c at the potential energy maximum, and is in fact an alternative to applying a boundary condition to the imref at the metal surface. The electron current can be expressed as

$$J_n = q(n_m - n_o)\, v_c \qquad \ldots\ldots(A3)$$

where $n_o = n(x_m)$ at zero bias V = 0, $n_m = n(x_m)$ when a bias voltage V is applied (V positive for forward bias).

Under zero bias $\phi_n(x_m) = 0$ $\psi(x_m) = qV_B$ so $n_o = N_C \exp\left[-qV_B/kT\right]$

For a forward bias V $\phi_n(x_m) = qV$ $\psi(x_m) = qV_B$ and

$$n_m = N_c \exp\left[-(qV_B - \phi_n(x_m))/kT\right] \qquad \ldots\ldots(A4)$$

Eliminating n(x) between equations (A1) and (A2)

$$J_n = q\mu_n\left(\frac{1}{q}\frac{\partial \phi_n}{\partial x}\right) N_c \exp\left[-\left(\psi(x) - \phi_n(x)\right)/kT\right]$$

and integrating between x_m and λ

$$\frac{J_n}{\mu_n N_c kT}\int_{x_m}^{\lambda}\exp\left(\frac{\psi(x)}{kT}\right)dx = \int_{x=x_m}^{x=\lambda}\frac{1}{kT}\exp\left(\frac{\phi_n(x)}{kT}\right)d\phi$$

$$= \left[\exp\left(\frac{\phi_n(x)}{kT}\right)\right]_{x=x_m}^{x=\lambda}$$

$$= \exp\left(\frac{qV}{kT}\right) - \exp\left(\frac{\phi_n(x_m)}{kT}\right) \quad \ldots(A5)$$

From (A3) and (A4)

$$\frac{n_m}{N_c} = \frac{n_o}{N_c} + \frac{J_n}{qv_cN_c}$$

$$\exp\left[-\left(\frac{qV_B - \phi_n(x_m)}{kT}\right)\right] = \exp\left(-\frac{qV_B}{kT}\right) + \frac{J_n}{qv_cN_c}$$

$$\exp\left(\frac{\phi_n(x_m)}{kT}\right) = 1 + \frac{J_n}{qv_cN_c}\exp\left(\frac{qV_B}{kT}\right) \quad \ldots..(A6)$$

Eliminating $\phi_n(x_m)$ between (A5) and (A6)

$$\frac{J_n}{\mu_n N_c kT}\int_{x_m}^{\lambda}\exp\left(\frac{\psi(x)}{kT}\right)dx - \exp\left(\frac{qV}{kT}\right)$$

$$= -1 - \frac{J_n}{qv_cN_c}\exp\left(\frac{qV_B}{kT}\right)$$

Putting $$\frac{1}{V_d} = \int_{x_m}^{\lambda}\frac{q}{\mu_n kT}\exp\left[\frac{(\psi(x) - qV_B)}{kT}\right]dx \quad \ldots..(A7)$$

$$\frac{J_n}{qN_cv_d}\exp\left(\frac{qV_B}{kT}\right) + \frac{J_n}{qN_cv_c}\exp\left(\frac{qV_B}{kT}\right) = \exp\left(\frac{qV}{kT}\right) - 1$$

Hence $$J_n = \frac{qN_cv_c}{1 + v_c/v_d}\exp\left(\frac{-qV_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad \ldots\ldots(A8)$$

The expression for v_d given in equation (A7) can be evaluated if some form for the potential variation through the barrier is assumed, such as that given in equation (3) of Chapter 2,

$$V(x) = \frac{qN_D}{\epsilon_{si}}\left(\lambda x - x^2/2\right) - V_B \qquad 0 \leq x \leq \lambda$$

This potential distribution results from the assumption of a uniform space charge density qN_D between $x = 0$ and $x = \lambda$. Image force lowering of the barrier is neglected in this expression, but its effect will be small between $x = x_m$ and $x = \lambda$. The potential energy $\psi(x)$ is given by

$$\psi(x) = -qV(x) = qV_B - \frac{q^2N_D}{\epsilon_{si}}\left(\lambda x - x^2/2\right)$$

$$\lambda = \sqrt{\frac{2\epsilon_{si}}{qN_D}\left(V_B - V_F - kT/q - V\right)}$$

$$\psi(\lambda) = q\left(V_F + V + kT/q\right)$$

$$\psi(x_m) \approx \psi(0) = qV_B \quad \text{if image force lowering is small.}$$

Put $$\beta = \frac{1}{kT}\left(\psi(x) - \psi(\lambda)\right)$$

$$= \frac{1}{kT}\frac{q^2N_D}{\epsilon_{si}}\left[\lambda^2/2 - \lambda x + x^2/2\right]$$

$$= \frac{q^2N_D}{2kT\epsilon_{si}}\left(\lambda - x\right)^2$$

Substitute t^2 for β

$$t = +\left(\frac{q^2 N_D}{2kT\epsilon_{si}}\right)^{1/2}(\lambda - x) \qquad \frac{dt}{dx} = -\left(\frac{q^2 N_D}{2kT\epsilon_{si}}\right)^{1/2}$$

From equation (A7)

$$\frac{1}{V_d} = -\exp\left[\frac{\psi(\lambda) - qV_B}{kT}\right]\int_{x=x_m}^{x=\lambda}\frac{q}{\mu_n kT}\exp\left[\frac{\psi(x)-\psi(\lambda)}{kT}\right]\left(\frac{2kT\epsilon_{si}}{q^2 N_D}\right)^{1/2}dt$$

$$= -\exp\left[\frac{-q(V_B - V_F - kT/q - V)}{kT}\right]\frac{q}{\mu_n kT}\left(\frac{2kT\epsilon_{si}}{q^2 N_D}\right)^{1/2}\int_{\beta=\frac{q}{kT}(V_B - V_F - kT/q - V)}^{\beta=0}\exp(t^2)\,dt$$

$$= +\frac{q}{\mu_n kT}\left(\frac{2kT\epsilon_{si}}{q^2 N_D}\right)^{1/2}\exp(-y^2)\int_{t=0}^{t=y}\exp(t^2)\,dt$$

where $y^2 = q/kT\,(V_B - V_F - kT/q - V)$

Hence $$\frac{1}{V_d} = \frac{D(y)}{V_D} \qquad \text{.....(A9)}$$

where $$V_D = \frac{\mu_n kT}{\sqrt{2}\,q\,L_D}$$

and $L_D = \left(\frac{kT\epsilon_{si}}{q^2 N_D}\right)^{1/2}$ is the effective Debye diffusion length, and D(y) is the Dawson function $D(y) \equiv \exp(-y^2)\int_{t=0}^{t=y}\exp(t^2)\,dt$

which satisfies the differential equation $\frac{dD}{dy} = 1 - 2yD$

and whose value can be found from tables[50] or by numerical integration.

Discussion of Parameters in the Current-Voltage Relationship

If minority carrier current can be neglected then equation (A8) gives an expression for the total current density. It is convenient to

define a saturation current density

$$J_s \equiv \frac{q N_c v_c}{1 + v_c/v_d} \exp\left(\frac{-q V_B}{kT}\right) = \frac{J_{TH}}{1 + v_c/v_d} \qquad \ldots\ldots (A10)$$

J_{TH} is the limiting value of J_S when $v_d \gg v_c$ and there is no diffusion limitation to the current flow. In this case the value of the collection velocity $v_c = v_{co}$ can be deduced from the same considerations used in the thermionic emission theory[39, 49]. Neglecting quantum mechanical tunnelling and scattering the value is $v_{co} = A^* T^2 / q N_c$

and when this value is inserted in equation (A8), the current-voltage expression becomes

$$J = A^* T^2 \exp\left(\frac{-q V_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

i.e. equation (5) of the thermionic emission theory.

Crowell and Sze[15] have shown that tunnelling and phonon scattering reduce the collection velocity by factors f_q and f_p respectively. The value of f_q is obtained by averaging the tunnelling probability over the distribution of carriers incident on the barrier. It is a function of temperature and electric field at the barrier, but is always less than unity for conditions where the thermionic emission currents dominate the tunnelling currents. Electrons that cross the potential energy maximum at x_m can be scattered back by optical or acoustic phonons before they reach the metal so that only a fraction f_p get through. The value of f_p is obtained by averaging the probability of phonon emission over the distribution of carriers crossing the barrier and like f_q, it is a function of electric field temperature. Thus the effective collection velocity v_c is given by $v_c = v_{co}\ f_p\ f_q$ where $f_p\ f_q$ has a value close to 0.5 over much of the range of the range of electric field but falls rapidly for

fields below 10^5 volt m^{-1}.

The full expression for the saturation current density is now

$$J_S = \frac{q N_c f_p f_q v_{co}}{1 + D(\beta^{1/2})/\delta_v} \exp\left(\frac{-q V_B}{kT}\right) \qquad \text{.....(A11)}$$

where $\delta_v = v_D/v_c$ is a useful parameter which is almost independent of applied voltage. Using the following relationships,

$$v_D = \frac{\mu_n kT}{q}\left(\frac{q^2 N_D}{2kT\epsilon_{si}}\right)^{1/2} \qquad v_c = f_p f_q \frac{A^* T^2}{q N_c}$$

$$A^* = \left(\frac{4\pi q k^2}{h^3}\right) m_t^* \qquad N_c = 2\left(\frac{2\pi m_d^* kT}{h^2}\right)^{3/2}$$

where m_t^* is the electron effective mass for emission over the barrier (see equation (6), Chapter 2) and m_d^* is the effective mass for the density of states function, we can express δ_v as

$$\delta_v = \frac{\mu_n}{m_t^*}\left(\frac{\pi N_D}{\epsilon_{si}}\right)^{1/2} (m_d^*)^{3/2} \left(\frac{1}{f_p f_q}\right)$$

If μ_n and $f_p f_q$ were independent of field, then δ_v would be bias independent and mainly a function of doping density N_D as shown in the Figure below[24].

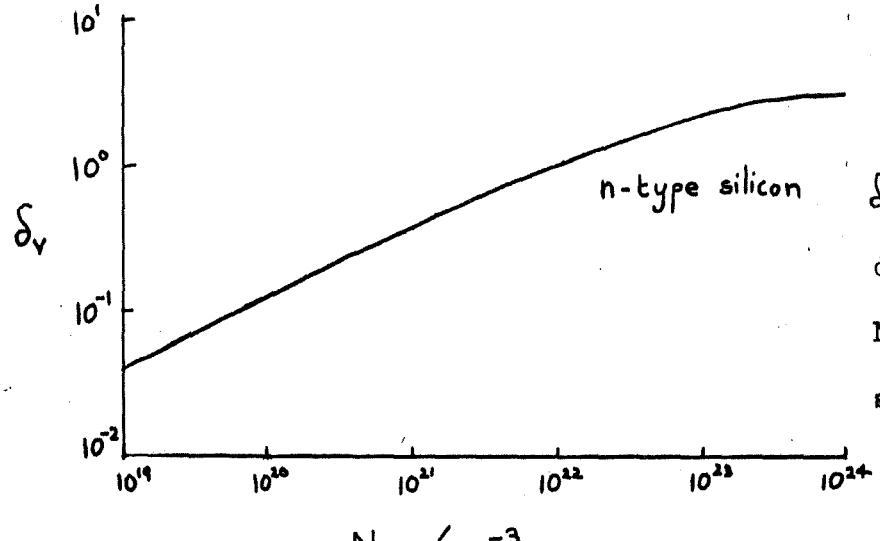


Figure 52 δ_v as a function of donor concentration N_D for n-type silicon.

However, for high barriers and reverse bias, the internal electric field may exceed 10^6 volt m^{-1} and the mobility is no longer constant[70]. Conversely, for low barriers and forward bias the internal field may be below 10^5 volt m^{-1} where the product $f_p f_q$ starts to decrease[15]. This will increase the value of δ_v but a more important effect will be the reduction in J_s through the influence of the term $f_p f_q$ in v_c on the numerator of equation (A10).

Formulation of Theoretical Predictions for Comparison with Experiment

Although equations (A8) and (A9) represent the predictions of thermionic diffusion theory, these analytical expressions are not convenient for comparison of experiment and theory. There are two approaches which can be used to reformulate the predictions embodied in equations (A8) and (A9). The first is to recognise that the 'saturation current' J_s is a voltage dependent parameter which can easily be evaluated from experimental values of current and voltage.

$$J_s \text{ (experimental)} = \frac{I}{S\left[\exp\left(qV/kT\right) - 1\right]}$$

The second approach is based upon the use of the parameter n or 'diode ideality factor' and it will be shown that the usefulness of this parameter is limited when it is varying rapidly as a function of voltage - in other words, in the region of greatest interest.

Saturation Current Variation

The theoretical value of the saturation current is given by equation (A11) which was derived assuming that the barrier height V_B was constant. If image force lowering of the barrier is small ($\Delta V_B < kT/q$) then its effect can be included by rewriting equation (A11) as

$$J_s = \frac{f_p f_q\, q N_c V_{co}}{1 + D/\delta_{..}} \exp\left[-q\left(\frac{V_B - \Delta V_B}{kT}\right)\right] \quad \text{.....(A12)}$$

Treating f_p f_q as constant Crowell and Beguwala[24] calculated $\frac{J_s}{J_{TH}} = \frac{1}{1+D/\delta_V}$ as a function of β and presented their results graphically. The present work has included the effects of image force lowering and presented below are the predicted values of $\frac{J_s}{J_{TH}(V=0)} = \exp\left[-q\left(\frac{\Delta V_B(V=0)-\Delta V_B(V)}{kT}\right)\right]\left(1+D/\delta_V\right)^{-1}$ as a function of β with N_D as a parameter. J_{TH} $(V=0)$ is the value of the saturation current density obtained from the thermionic emission model including image force lowering, but neglecting diffusion effects.

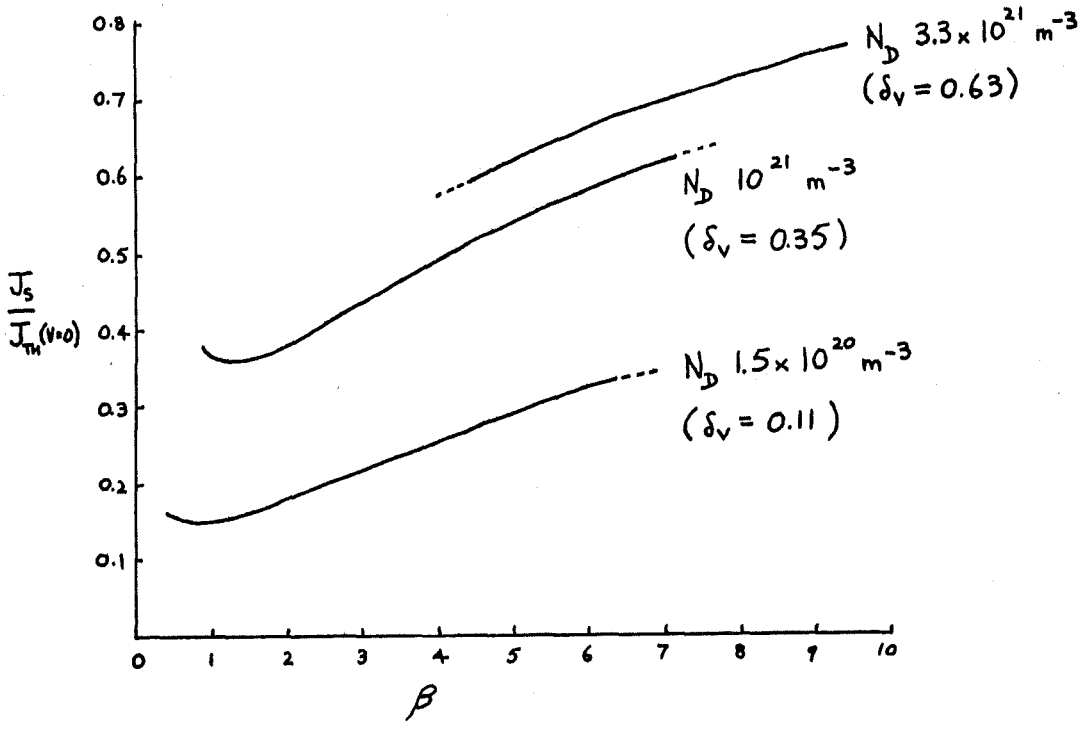


Figure 53 Predicted decrease in saturation current, due to diffusion and image force effects, as a function of band bending β. These predicted values of saturation current were obtained using a numerical integration method to evaluate the Dawson function (see Appendix C).

'n value' Variation

Although the diode n value is usually defined by $\frac{1}{n} = \frac{kT}{q}\frac{d}{dV}\ln(J)$, this definition is only useful for forward voltages $V \gg kT/q$. Following Crowell and Beguwala[24] a more useful definition of n, which is valid for forward and reverse bias, is

$$\frac{1}{n} \equiv \frac{kT}{q}\frac{d}{dV}\ln\left\{\frac{J}{1-\exp(-qV/kT)}\right\}\Bigg|_V \qquad \text{.....(A13)}$$

where the n value is a function of voltage. Integrating equation (A13)

$$\int_{V_o}^{V}\frac{q\,dV}{n(V)\,kT} = \left[\ln\left\{\frac{J}{1-\exp(-qV/kT)}\right\}\right]_{V_o}^{V}$$

hence

$$J(V) = J(V_o)\,\frac{\exp\left(\int_{V_o}^{V}\frac{q\,dV}{n(V)\,kT}\right)}{1-\exp(-qV_o/kT)}\left[1-\exp\left(-qV/kT\right)\right] \qquad \text{..(A14)}$$

where $J(V_o)$ is the saturation current density at some initial voltage V_o. Consider the case when n is a slowly varying function of voltage such that, throughout the range of integration, it can be treated as constant $n = n(V_o)$. Then (A14) reduces to

$$J(V) = \frac{J(V_o)}{\exp(qV_o/kT)-1}\exp\left\{q/kT\,(V-V_o)\left[\frac{1}{n(V_o)}-1\right]\right\}\left[\exp\left(qV/kT\right)-1\right] \qquad \text{.....(A15)}$$

but $\dfrac{J(V_o)}{\exp(qV_o/kT)-1} = J_s(V_o)$ from equation (A10).

Choosing $V_o = 0$, (A15) becomes

$$J = J_s(0)\exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(\frac{-qV}{kT}\right)\right]$$

which corresponds to the usual formulation in terms of n value (Equation (7), Chapter 2) when $V \gg \frac{kT}{q}$. However, it must be

remembered that this expression for the current-voltage relationship cannot be used when n is changing rapidly as a function of applied voltage.

To calculate the n value, we combine equations (A8) and (A10) in the form

$$J = J_{TH}\left(1 + \frac{D(\beta^{1/2})}{\delta_V}\right)^{-1}\left[\exp\left(qV/kT\right) - 1\right]$$

Thus

$$\frac{J}{1-\exp\left(-qV/kT\right)} = J_{TH}\left(1 + \frac{D(\beta^{1/2})}{\delta_V}\right)^{-1}\exp\left(qV/kT\right)$$

$$\frac{d}{dV}\ln\left\{\frac{J}{1-\exp\left(-qV/kT\right)}\right\} = \frac{d}{dV}\ln\left(J_{TH}\right) - \frac{\delta_V}{(\delta_V + D)}\frac{d}{dV}\left(\frac{D}{\delta_V}\right) + q/kT$$

Neglecting image force lowering effects, the first term on the right is zero and $\frac{d\beta}{dV} = -q/kT$ so that

$$kT/q\,\frac{d}{dV}\ln\left\{\frac{J}{1-\exp\left(-qV/kT\right)}\right\} = \frac{1}{2}\,\frac{(1 - 2\beta^{1/2}D)}{(\delta_V + D)}\,\frac{1}{\beta^{1/2}} + 1$$

Hence

$$\frac{1}{n} = \frac{\delta_V + 0.5\beta^{-1/2}}{\delta_V + D(\beta^{1/2})} \qquad \text{.....(A16)}$$

and using this relation the n value can be calculated as a function of band bending β .

Image force lowering can be included by considering the variation in J_{TH}, the thermionic emission saturation current,

$$J_{TH} = A^{*}T^{2}\exp\left[-q\left(\frac{V_B - \Delta V_B}{kT}\right)\right]$$

where $$\Delta V_B = \left\{ \frac{q^3 N_D}{8\pi^2 \epsilon_{si}^3} \left(V_B - V_F - kT/q - V \right) \right\}^{1/4}$$

so $$\frac{kT}{q} \frac{d}{dV} \ln(J_{TH}) = \frac{d\,\Delta V_B}{dV}$$

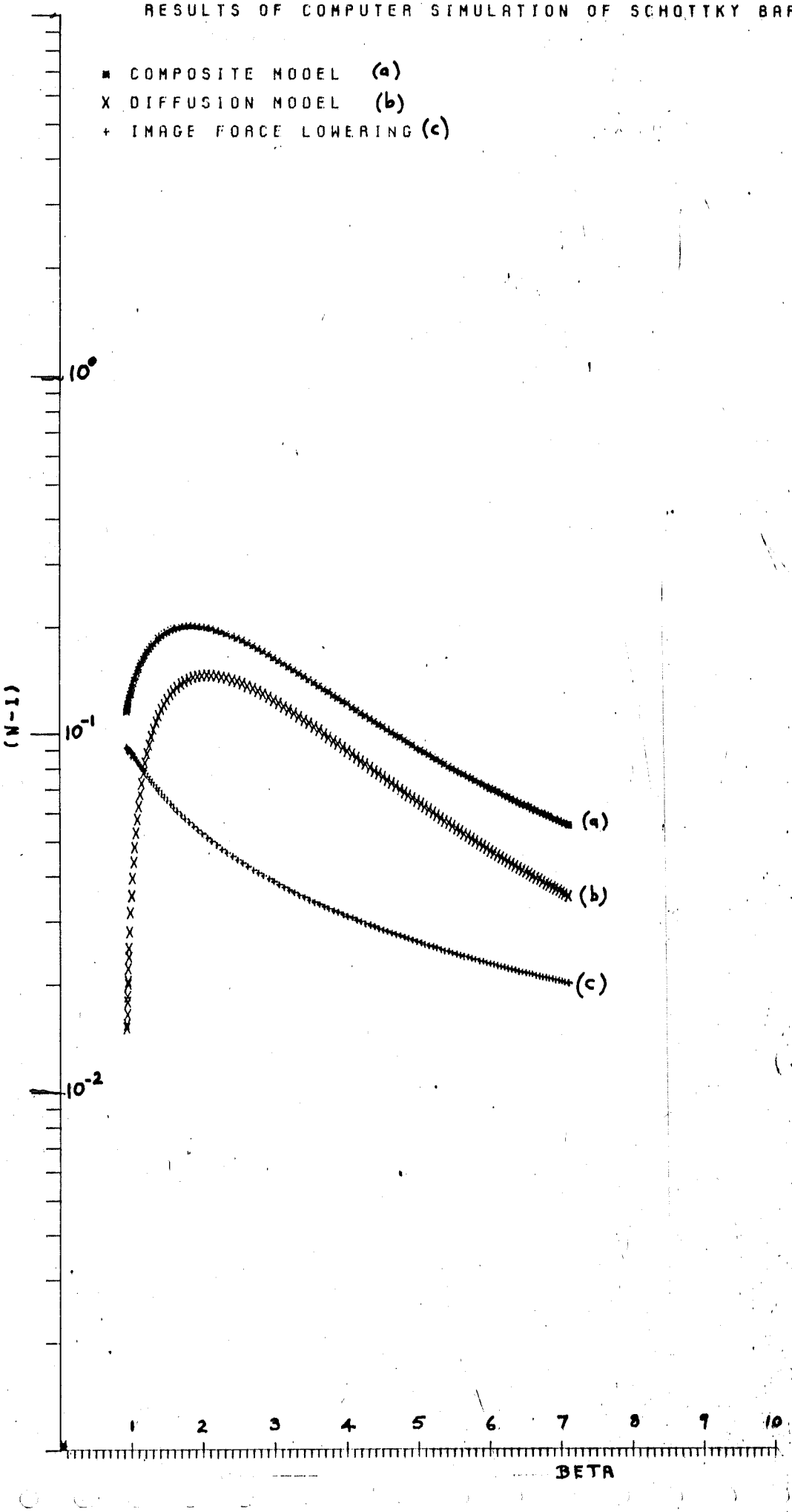
$$= \frac{-\Delta V_B}{4(V_B - V_F - kT/q - V)} = -\frac{1}{4} \left[\frac{q^3 N_D}{8\pi^2 \epsilon_{si}^3} \right]^{1/4} \left[\frac{kT}{q} \beta \right]^{-3/4}$$

The expression for the n value, equation (A16), becomes

$$\frac{1}{n} = \frac{\delta_V + 0.5\beta^{-1/2}}{\delta_V + D(\beta^{1/2})} - \frac{1}{4} \left[\frac{q^3 N_D}{8\pi^2 \epsilon_{si}^3} \right]^{1/4} \left[\frac{kT}{q} \beta \right]^{-3/4} \quad \text{.....(A17)}$$

The Figure overleaf shows the value of (n - 1), calculated using expression (A17), as a function of β. Also shown are the individual values of the two terms in expression (A17), for $N_D = 10^{21}\ m^{-3}$.

Figure 54


RESULTS OF COMPUTER SIMULATION OF SCHOTTKY BARRIER
■ COMPOSITE MODEL (a)
X DIFFUSION MODEL (b)
+ IMAGE FORCE LOWERING (c)
10⁰
10⁻¹
10⁻²
(N-1)
(a)
(b)
(c)
1
2
3
4
5
6
7
8
9
10
BETA

APPENDIX B

DERIVATION OF AN EXPRESSION FOR DIODE AC RESISTANCE

Diode Model

The Figure[55] shows the partition of the diode model. I_m and V_m represent the externally measured current and voltage, while V represents the part of this voltage that appears across the 'ideal' diode. The series resistance is split into two components because R_S, the resistance of the quasi-neutral epitaxial region, is sensitive to changes in voltage and temperature, whereas R_L, representing the resistance of the substrate, back contact and external leads, is not. The resistance of the alloyed back contact is almost negligible. An upper limit on its value can be calculated[71] by treating the back contact as a gold silicon junction where the dominant current transport mechanism is tunnelling, since the donor concentration is greater than $3 \times 10^{24}\ m^{-3}$. The calculated value of junction resistance is $0.25\ \Omega$.

The current-voltage relation of the 'ideal' diode is represented by the equation

$$I_m = \frac{f_p f_q A^* S T^2 \exp\left[\frac{-q}{kT}(V_B - \Delta V_B)\right]\left[\exp\left(\frac{qV}{kT}\right) - 1\right]}{1 + D/\delta_v} \qquad \text{.....(B1)}$$

which is derived from equation (A11) of the Thermionic-Diffusion model given in Appendix A.

For small temperature variations, the series resistance R_S can be written[40],

$$R_S\ (V, T) = R_S\ (V, T_A)\ \left(\frac{T}{T_A}\right)^{2.5}$$

assuming electron mobility is the main temperature dependent factor[40] contributing to the variation of R_S, for the donor concentrations used in this work. The variation in R_S due to changes in the depletion region width can be expressed as

$$R_S\ (V, T) = R_S\ (0, T)\ \frac{(x_{EP1} - \lambda(V))}{(x_{EP1} - \lambda(0))}$$

as in equation (26). These two expressions can be combined as

$$R_S\ (V, T) = R_S\ (0, T_A)\left(\frac{T}{T_A}\right)^{2.5}\ \frac{(x_{EP1} - \lambda(V))}{(x_{EP1} - \lambda(0))} \qquad \text{.....(B2)}$$

By inspection of the diode model shown in the Figure

$$V_m = V + I_m\ (R_S + R_L)$$

For small changes

$$\Delta V_m = \Delta V + I_m \Delta R_S + (R_S + R_L)\Delta I_m$$

and $\Delta R_S = \frac{d R_S}{dV}\ \Delta V \qquad \Delta I_m = \frac{d I_m}{dV}\ \Delta V$

Hence $$\frac{\Delta V_m}{\Delta I_m} = \frac{\Delta V}{\Delta I_m} + I_m \frac{dR_s}{dV}\frac{\Delta V}{\Delta I_m} + (R_S + R_L)$$

$$R_{AC} = \frac{d V_m}{d I_m} = \left(\frac{d I_m}{dV}\right)^{-1}\left(1 + I_m \frac{d R_s}{dV}\right) + (R_S + R_L) \qquad \text{.....(B3)}$$

I_m is a function of voltage and temperature so

$$\frac{dI_m}{dV} = \left.\frac{\partial I_m}{\partial V}\right|_T + \left.\frac{\partial I_m}{\partial T}\right|_V \frac{dT}{dV} \qquad \ldots\ldots(B4)$$

where $\frac{dT}{dV}$ is written as a total derivative because the ambient temperature is considered constant and the only changes in T are caused directly by the increased power dissipation when V is increased.

Derivation of $\left.\frac{\partial I_m}{\partial V}\right|_T$

Differentiating equation (B1) logarithmically

$$\frac{1}{I_m}\frac{\partial I_m}{\partial V} = \frac{\partial}{\partial V}\left\{\ell n\left(f_p f_q A^* S T^2\right) - \ell n\left(1+\frac{D}{\delta_v}\right) - \frac{q}{kT}\left(V_B-\Delta V_B\right) + \ell n\left[\exp\left(\frac{qV}{kT}\right)-1\right]\right\} \qquad \ldots\ldots(B5)$$

and considering each term in turn.

$\frac{\partial}{\partial V}\ell n\left(f_p f_q A^* S T^2\right)$ will be neglected at this stage as $f_p f_q$ is a very slowly varying function of voltage.

$$\frac{\partial}{\partial V}\ell n\left(1+\frac{D}{\delta_v}\right) = \frac{1}{\delta_v + D}\frac{\partial}{\partial V}D(\beta^{1/2}) = \frac{\left(1-2\beta^{1/2}D(\beta^{1/2})\right)}{(\delta_v+D)\,2\beta^{1/2}}\left(\frac{-q}{kT}\right)$$

$$= \frac{q}{kT}\left(\frac{D-0.5\beta^{-1/2}}{D+\delta_v}\right) \qquad \ldots\ldots(B6)$$

If image force lowering is the major contribution to ΔV_B then

$$-\frac{q}{kT}\frac{\partial}{\partial V}\left(V_B-\Delta V_B\right) = \frac{q}{kT}\frac{\partial \Delta V_B}{\partial V} = \frac{q}{kT}\left[\frac{-\Delta V_B}{4\left(V_B-V_F-\frac{kT}{q}-V\right)}\right]$$

$$= \frac{-q}{4kT}\left[\frac{q^3 N_D}{8\pi^2 \epsilon_{Si}^3}\right]^{1/4}\left(V_B - V_F - \frac{kT}{q} - V\right)^{-3/4} \qquad \ldots\ldots(B7)$$

$$\frac{\partial}{\partial V} \ln\left[\exp\left(\frac{qV}{kT}\right) - 1\right] = \frac{q}{kT}\,\frac{\exp\left(\frac{qV}{kT}\right)}{\left(\exp\left(\frac{qV}{kT}\right) - 1\right)} = \frac{q/kT}{\left(1 - \exp\left(\frac{-qV}{kT}\right)\right)} \qquad \ldots\ldots(B8)$$

Substituting (B6), (B7), and (B8) back into (B5)

$$\left.\frac{\partial I_m}{\partial V}\right|_T = \frac{qI_m}{kT}\left\{\frac{-(D - 0.5\beta^{1/2})}{(D + \delta_V)} - \frac{\Delta V_B}{4\left(V_B - V_F - \frac{kT}{q}\right)} + \frac{1}{\left(1 - \exp\left(\frac{-qV}{kT}\right)\right)}\right\} \ldots(B9)$$

Derivation of $\left.\frac{\partial I_m}{\partial T}\right|_V$

Differentiating equation (B1) logarithmically,

$$\frac{1}{I_m}\frac{\partial I_m}{\partial T} = \frac{\partial}{\partial T}\left\{\ln\left(f_p f_q A^* S T^2\right) - \ln\left(1 + \frac{D}{\delta_V}\right) - \frac{q}{kT}\left(V_B - \Delta V_B\right) + \ln\left[\exp\left(\frac{qV}{kT}\right) - 1\right]\right\}$$

$$= \frac{2 f_p f_q A^* S T}{f_p f_q A^* S T^2} + \frac{\left(1 - 2\beta^{1/2} D(\beta^{1/2})\right)}{\delta_V + D(\beta^{1/2})}\,\frac{\beta^{-1/2}}{2}\,\frac{q}{kT^2}\left(V_B - V_F - \frac{kT}{q} - V\right)$$

$$+ \frac{q}{kT^2}\left(V_B - \Delta V_B\right) + \left(\frac{-qV}{kT^2}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right]^{-1}$$

$$\frac{\partial I_m}{\partial T} = \frac{I_m}{T}\left\{2 + \frac{(0.5 - \beta^{1/2} D)}{\delta_V + D}\beta^{1/2} + \frac{q}{kT}\left(V_B - \Delta V_B\right) - \frac{q/kT}{\left(1 - \exp\left(\frac{-qV}{kT}\right)\right)}\right\} \ldots(B10)$$

By substitution of numerical values it is found that the second term is negligible (~ 0.1). For $V > \frac{3kT}{q}$ the last term becomes $\left(\frac{-qV}{kT}\right)$.

Derivation of $\frac{dT}{dV}$

$\frac{dT}{dV} = \frac{dT}{dP}\frac{dP}{dV} = \Theta_w \left(I_m + V\frac{dI_m}{dV}\right)$ where Θ_w is the value of thermal resistance appropriate to changes in dissipated power at a frequency w. (See Appendix D). Substituting the above expressions back into (B4).

$$\frac{dI_m}{dV} = \left.\frac{\partial I_m}{\partial V}\right|_T + \frac{I_m}{T}\left\{2 + \frac{q}{kT}\left(V_B - \Delta V_B - V\right)\right\}\left[\Theta_w\left(I_m + V\frac{dI_m}{dV}\right)\right]$$

$$\frac{dI_m}{dV}\left\{1 - \frac{I_m V \Theta_w}{T}\left[2 + \frac{q}{kT}\left(V_B - \Delta V_B - V\right)\right]\right\} = \left.\frac{\partial I_m}{\partial V}\right|_T + \frac{I_m^2 \Theta_w}{T}\left[2 + \frac{q}{kT}\left(V_B - \Delta V_B - V\right)\right] \quad \ldots(B11)$$

In the limit of very low power dissipation in the diode, the second terms on each side of equation (B11) can be neglected and $\frac{dI_m}{dV} = \left.\frac{\partial I_m}{\partial V}\right|_T$

The second term on the left-hand side of equation (B11) becomes significant when $\frac{I_m V \Theta_w}{T}\left[2 + \frac{q}{kT}\left(V_B - \Delta V_B - V\right)\right] \sim 10^{-3}$

Taking $\Theta_{4KH_Z} = 10^{\circ}C\ \text{watt}^{-1}$ as a typical value,[72] the critical power level is $I_m V_m \approx 3$ mW which corresponds to $I_m \approx 10$ mA. The second term on the right-hand side of equation (B11) becomes significant when equal to 10^{-3} $\left(\frac{qI_m}{kT}\right)$ which is the approximate value of $\left.\frac{\partial I_m}{\partial V}\right|_T$

Approximately:

$$\frac{I_m^2 \Theta_w}{T}(20) \approx 10^{-3}\frac{qI_m}{kT}$$

$$I_m \approx \frac{10^{-3}}{25.10^{-3}}\frac{300}{20.10} \approx 60\ \text{mA}$$

Derivation of $\frac{dR_S}{dV}$

R_S is a function of voltage and temperature so that

$$\frac{dR_S}{dV} = \left.\frac{\partial R_S}{\partial V}\right|_T + \left.\frac{\partial R_S}{\partial T}\right|_V \frac{dT}{dV}$$

$$\left.\frac{\partial R_S}{\partial V}\right|_T = \frac{-R_S(0,T_A)}{(x_{EPI}-\lambda(0))}\left(\frac{T}{T_A}\right)^{2.5}\frac{d\lambda}{dV} = \frac{R_S(0,T_A)}{2(x_{EPI}-\lambda(0))}\left(\frac{T}{T_A}\right)^{2.5}\left[\frac{2\epsilon_{Si}}{qN_D(V_B-V_F-\frac{kT}{q}-V)}\right]^{1/2}$$

$$\left.\frac{\partial R_S}{\partial T}\right|_V = 2.5\,R_S(0,T_A)\,\frac{(x_{EPI}-\lambda(V))}{(x_{EPI}-\lambda(0))}\,\frac{T^{1.5}}{T_A^{2.5}}$$

As before $\frac{dT}{dV} = \theta_w\left(I_m + V\frac{dI_m}{dV}\right)$, hence

$$\frac{dR_S}{dV} = \frac{R_S(0,T_A)}{(x_{EPI}-\lambda(0))}\left\{\frac{1}{2}\left(\frac{T}{T_A}\right)^{2.5}\left[\frac{2\epsilon_{Si}}{qN_D(V_B-V_F-\frac{kT}{q}-V)}\right]^{1/2}\right.$$

$$\left. + 2.5\,(x_{EPI}-\lambda(V))\left(\frac{T^{1.5}}{T_A^{2.5}}\right)\theta_w\left[I_m + V\frac{dI_m}{dV}\right]\right\} \qquad \text{.....(B12)}$$

Substituting typical values into the above expression shows that the second term on the right is negligible in comparison with the first term for currents below 10 mA.

Diode AC Resistance

Substitution of the above expressions back into (B3) yields the result,

$$R_{AC} = R_S(V,T) + R_L + \frac{kT}{qI_m}\left\{-\frac{(D-0.5\beta^{-1/2})}{(D+\delta_v)} - \frac{\Delta V_B}{4\left(V_B - V_F - \frac{kT}{q} - V\right)}\right\}^{+}$$

$$\left\{\frac{1}{1-\exp\left(\frac{-qV}{kT}\right)}\right\}^{-1}\left\{1 + \frac{I_m}{2}\frac{R_S(0,T)}{(x_{EPI}-\lambda(0))}\left[\frac{2\epsilon_{Si}}{qN_D\left(V_B - V_F - \frac{kT}{q} - V\right)}\right]^{1/2}\right\} \quad \ldots.(B13)$$

which is valid for diode currents below 10 mA. Above this level of current, the terms which have been neglected in equations (B11) and (B12) would be expected to become increasingly significant.

Using the expression for the n value given in Appendix A equation (A17),

$$\frac{1}{n} - 1 = -\frac{(D-0.5\beta^{-1/2})}{(D+\delta_v)} - \frac{\Delta V_B}{4\left(V_B - V_F - \frac{kT}{q} - V\right)}$$

then equation (B13) reduces to

$$R_{AC} = R_S(V,T) + R_L + \frac{nkT}{q(I_m + nI_S)}\left\{1 + \frac{I_m \times 0.5 R_S(0,T)}{(x_{EPI}-\lambda(0))}\left[\frac{2\epsilon_{Si}}{qN_D\left(V_B - V_F - \frac{kT}{q} - V\right)}\right]^{1/2}\right\} \quad \ldots(B14)$$

where I_S is the saturation current ,

$$I_s = \frac{I_m}{\exp\left(\frac{qV}{kT}\right) - 1}$$

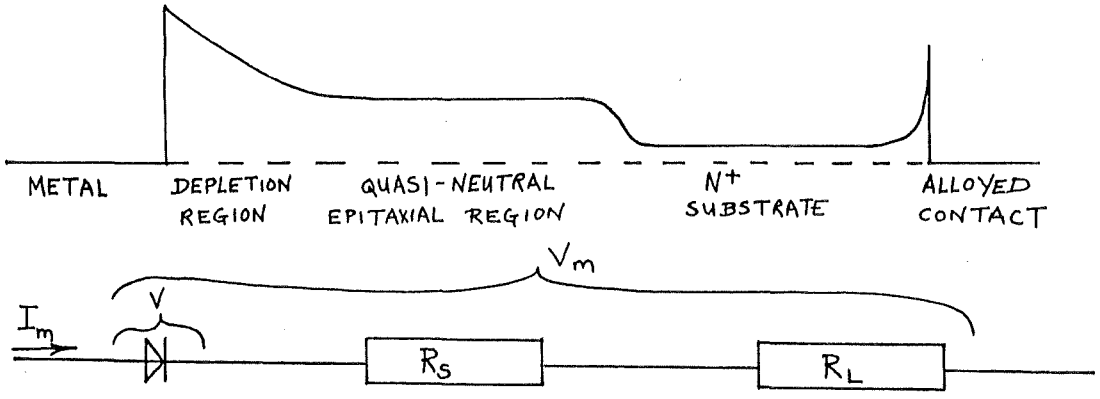


Figure 55 Partition of diode model into three components; 'ideal' diode, epitaxial layer resistance, substrate and back contact resistance.

APPENDIX C

COMPUTER DIODE SIMULATION PROGRAM

Description

The program is based on the thermionic-diffusion model of Crowell and Sze[15] but also includes image force lowering, diode self-heating and variation of undepleted epitaxial layer width causing changes in the series resistance. A brief description of its operation is given below.

The input to the program consists of experimentally measured values of diode current, voltage and AC resistance, which are to be compared with the model predictions calculated from the values of the model parameters. These are as follows (where the Fortran coding is given in brackets) : barrier height V_B (VBO), ambient temperature T_A (TA), series resistance components R_L and R_S (RL and REPI), saturation current I_S at V = 0 (ISO), impurity concentration N_D (ND), epitaxial layer thickness x_{EPI} (EPI), velocity ratio δ_V (DELTAV), thermal resistance Θ_{DC} (TRDC), and in addition various constants such as ϵ_{si} (EPSI) and q (Q).

The program takes the first experimental current and voltage readings, and estimates the diode voltage using the value of series resistance from the model. This first estimate of diode voltage is then used to calculate the band bending, image force lowering, depletion layer width λ and the thermionic-diffusion theory saturation current. From this last parameter, a second estimate of the diode voltage is made, which is compared with the previous estimate, and if these are within 10^{-5} volt the program then prints out the calculated parameters including diode temperature. If the second estimate of voltage is not within 10^{-5} volt, the calculation

sequence iterates until two successive values are within this range. In practice the values converge very rapidly to a self consistent answer. The sequence is then repeated for the subsequent experimental current readings.

For each current reading, the computer output lists the experimental and predicted values of voltage and AC resistance. For convenience in checking closeness of fit between the model and the experimental date, the program also calculate and lists the mean difference, root mean square difference and χ^2.

Program Listing and Output

(see following pages).

```
FORTRAN    200        SOURCE LISTING AND DIAGNOSTICS                    PROGRAM: NONAME

001           DIMENSION XI(14),XV(14),XG(14)
002           DIMENSION INP(20)
003           REAL ITH
004           REAL NC
005           REAL IM,IS,ISO,ND
006           DATA XI/.11,.19,1.1,1.827,1.957,3.215,4.44,7.305,10.0,13.6,
             1 17.21,19.93,22.65,24.7/
007           DATA XG/4.587,6.997,24.575,32.11,33.16,40.38,44.64,50.03,52.6,
             1 54.43,55.31,55.61,55.71,55.675/
010           DATA XV/47.8,61.8,121.8,147.,151.,184.4,212.,272.,323.,389.,455.,
             1 503.,553.,589./
011           NDATA=14
012           EBB=0
013           C=2.14E-2
014           VBO=0.51
015           TA=294.44
016           RSO=15.3
017           RSO=14.7
020           REPI=14.27
021           RL=1.0
022           RSO=REPI+RL
023           ISO=2.334E-5
024           EPI=15.E-6
025           ND=1.E21
026           NC=2.8E25
027           READ(2,91)INP
030        91 FORMAT(20A3)
031        92 FORMAT(1X,20A3)
032           WRITE(3,92)INP
033           VF=ALOG(NC/ND)*.8613E-4*TA
034           TR=1./TA
035           DELTAV=0.35
036           EPSI=11.7*8.86E-12
037           Q=1.602E-19
040           FR=2.*EPSI/(ND*Q)
041           FB=VBO-VF
042           TRAC=11.5
043           TRDC=260.
044           ACC=.0001
045           BB=FB-0.8613E-4*TA
046           DFI=SQRT(BB)
047           DFI=C*SQRT(DFI)
050           FI=-1.161E4*(VBO-DFI)
051           FM=SQRT(FR*BB)
052           B=BB/(0.8613E-4*TA)
053           X=SQRT(B)
054           D=SIMPS(0.,X,.0035,N)*EXP(-B)
055           AASTAR=ISO/(TA*TA*EXP(FI/TA))*(1.+D/DELTAV)
056           RS=RSO
057           T=TA
060           ITH=ISO*(1.+D/DELTAV)
061           WRITE(3,93)VBO,RSO,ISO,ITH,EPI,ND,VF,TA,DELTAV
062        93 FORMAT(/5H VBO=,E10.4,5H RSO=,E10.4,5H ISO=,E10.4,/5H ITH=,E10.4,
             1 5H EPI=,E10.4,5H  ND=,E10.4,/15H FERMI VOLTAGE=,E10.4,6H TAMB=,
             2 E10.4,8H DELTAV=,E10.4//)
063           WRITE(3,94)
064        94 FORMAT(1X,43H CURRENT     VOLTAGE   IMPEDANCE  V-JUNCTION,
             1 29H T-AMBIENT  R-SERIES     BETA ,13X,22H IS(CBB)    IMAGE FORCE,
             2///)
065           GBAR=0.
066           VBAR=0.
```

```
      GCHI=0.
      VCHI=0.
      SUMSQ=0.
      SUM2=0.
      DO 90 I=1,NDATA
      XG(I)=1000./XG(I)
      IF(XG(I)-100.)30,32,32
   30 D=0.31
      GOTO33
   32 D=0.20
   33 XG(I)=XG(I)-D
      XV(I)=XV(I)*.001
      XI(I)=XI(I)*.001
      VM=XV(I)
      IM=XI(I)
      V=VM-IM*RS
    2 TF=0.8613E-4*T
      TT=T*TR
      BB=FB-V-TF
      B=BB/TF
      IF(B)17,17,19
   17 WRITE(3,18)B
   18 FORMAT(26H NEGATIVE BAND BENDING OF ,E10.4,7H (KT/Q))
      ESB=1
      BB=0.
      B=0.
      NDATA=I-1
      GOTO95
   19 CONTINUE
      DFI=SQRT(BB)
      DFI=C*SQRT(DFI)
      FI=-1.161E4*(VBO-DFI)
      RS=RL+REPI*(EPI-SQRT(FR*BB))*TT*TT*SQRT(TT)/(EPI-FW)
      X=SQRT(B)
      E=.0035/D
      IF(E-ACC)20,20,21
   20 E=ACC
   21 D=SIMPS(0.0,X,E,N)*EXP(-B)
      IS=AASTAR*T*T*EXP(FI/T)/(1.+D/DELTAV)
      VO=V
      V=TF*ALOG(1.+IM/IS)
      VM=V+IM*RS
      T=TA+TRDC*IM*VM
      RES=RS+(1.+1M*0.5*REPI*SQRT(FR*TT/BB)*TI*TT/(EPI-FW))/
     1 (IM/TF*(1./(1.-EXP(-V/TF))-.25*DFI/BB-(D-.5/X)/(D+DELTAV)))
      IF(ABS(VO-V)-1.E-5)3,3,2
    3 CONTINUE
      DG=XG(I)-RES
      DV=XV(I)-VM
      GBAR=GBAR+DG
      VBAR=VBAR+DV
      SUMSQ=SUMSQ+DG*DG
      SUM2=SUM2+DV*DV
      GCHI=GCHI+DG*DG/RES
      VCHI=VCHI+DV*DV/VM
      WRITE(3,4)IM,XV(I),XG(I),VM,RES,V,T,RS,B,D,IS,DFI,DV,DG
    4 FORMAT(/3(1X,E10.4)/2(11X,9(1X,E10.4)/))
      XV(I)=DV
      XG(I)=DG
   90 CONTINUE
   95 CONTINUE
      F=NDATA
      GBAR=GBAR/F
      VBAR=VBAR/F
      ZG=GBAR*SQRT((F-1.)/SUMSQ)
      ZV=VBAR*SQRT((F-1.)/SUM2 )
      SUMSQ=SQRT(SUMSQ/F)
      SUM2=SQRT(SUM2/F)
      WRITE(3,100)VBAR,GBAR,SUM2,SUMSQ,VCHI,GCHI,
     1 ((XV(I),XG(I)),I=1,NDATA)
  100 FORMAT(//13H DIFFERENCES:/,5H MEAN,6X,2(1X,E10.4)/5H RMS ,6X,
     1 2(1X,E10.4)/6H CHISQ,5X,2(1X,E10.4)//14(11X,2(1X,E10.4)/))
      NDA=NDATA-1
      WRITE(3,60)NDA
   60 FORMAT(1X,I3, 20H DEGREES OF FREEDOM./)
      IF(EBB)802,802,800
  800 WRITE(3,801)
  801 FORMAT(50H SEE HENISCH $7.5,P203                              )
  802 CONTINUE
      STOP
      RETURN
      END
```

```
FORTRAN     200        SOURCE LISTING AND DIAGNOSTICS                    PROGRAM: F

001             FUNCTION F(X)
002             F=EXP(X*X)
003             RETURN
004             END
```

```
FORTRAN     200        SOURCE LISTING AND DIAGNOSTICS                    PROGRAM: SIMPS

001             FUNCTION SIMPS(XL,XU,EPS,N)
002             NMAX=127
003             N=0
004             FANDL=F(XL)+F(XU)
005             OLD=0.0
006             DX=XU-XL
007             SIMPS=0.0
010             EVENS=0.0
011             ODDS=0.0
012          98 H=DX*0.5
013             X=XL+H
014             OLD=SIMPS
015             ODDS=ODDS+EVENS
016             EVENS=0.0
017           1 EVENS=EVENS+F(X)
020             X=X+DX
021             N=N+1
022             IF(X-XU)1,2,2
023           2 DX=H
024             SIMPS=(FANDL+4.*EVENS+2.*ODDS)*H/3.
025             IF(SIMPS)4,3,4
026           3 IF(ABS(OLD-SIMPS)-EPS)5,5,99
027           4 IF(ABS(1.-OLD/SIMPS)-EPS)5,5,99
030          99 IF(N-NMAX)98,5,5
031           5 ERR=ABS(OLD-SIMPS)
032             RETURN
033             END
```

D7AS1

VBO= .5100E+00 RSO= .1527E+02 ISO= .2334E-04
ITH= .3533E-04 EPI= .1500E-04 ND= .1000E+22
FERMI VOLTAGE= .2597E-00 TAMB= .2944E+03 DELTAV= .3500E+00

CURRENT	VOLTAGE	IMPEDANCE	V-JUNCTION	T-AMBIENT	R-SERIES	BETA		IS(C&B)	IMAGE FORCE
.1100E-03	.4780E-01	.2178E+03							
	.4760E-01	.2170E+03	.4591E-01	.2944E+03	.1533E+02	.7060E+01	.2065E+00	.2152E-04	.1392E-01
	.2047E-03	.7950E+00							
.1900E-03	.6180E-01	.1427E+03							
	.6150E-01	.1422E+03	.5858E-01	.2944E+03	.1534E+02	.6560E+01	.2163F+00	.2094E-04	.1367E-01
	.3022E-03	.5186E+00							
.1100E-02	.1218E+00	.4038E+02							
	.1210E+00	.4030E+02	.1041E-00	.2945E+03	.1542E+02	.4765E+01	.2675F+00	.1846E-04	.1262E-01
	.7550E-03	.8484E-01							
.1827E-02	.1470E+00	.3083E+02							
	.1463E+00	.3080E+02	.1180E-00	.2945E+03	.1544E+02	.4214E+01	.2909F+00	.1757E-04	.1224E-01
	.7353E-03	.3526E-01							
.1957E-02	.1510E+00	.2985E+02							
	.1502E+00	.2983E+02	.1200E-00	.2945E+03	.1545E+02	.4138E+01	.2946F+00	.1744E-04	.1218F-01
	.8054E-03	.1553E-01							
.3215E-02	.1844E+00	.2445E+02							
	.1837E+00	.2447E+02	.1339E-00	.2946E+03	.1548E+02	.3587E+01	.3244F+00	.1648E-04	.1175E-01
	.6950E-03	-.1699E-01							
.4440E-02	.2120E+00	.2209E+02							
	.2120E+00	.2215E+02	.1431E-00	.2947E+03	.1551E+02	.3223E+01	.3480F+00	.1584E-04	.1144E-01
	-.6600E-05	-.5552E-01							
.7305E-02	.2720E+00	.1968E+02							
	.2712E+00	.1974E+02	.1575E-00	.2950E+03	.1557E+02	.2655F+01	.3918F+00	.1489E-04	.1091E-01
	.7727E-03	-.6673E-01							
.1000E-01	.3230E+00	.1870E+02							
	.3228E+00	.1875E+02	.1665E-00	.2953E+03	.1563E+02	.2297F+01	.4238F+00	.1439E-04	.1052E-01
	.1950E-03	-.5027E-01							

.1360E-01	.3890E+00	.1806E+02							
	.3889E+00	.1807E+02	.1751E-00	.2958E+03	.1572E+02	.1953E+01	.4574E+00	.1411E-04	.1011E-01
	.9210E-04	-.4390E-02							
.1721E-01	.4550E+00	.1777E+02							
	.4537E+00	.1770E+02	.1814E-00	.2965E+03	.1582E+02	.1699F+01	.4826F+00	.1417E-04	.9767E-02
	.1343E-02	.6706E-01							
.1993E-01	.5030E+00	.1767E+02							
	.5020E+00	.1754E+02	.1851E-00	.2970E+03	.1590E+02	.1550F+01	.4971F+00	.1439E-04	.9549E-02
	.9740E-03	.1295E+00							
.2265E-01	.5530E+00	.1764E+02							
	.5503E+00	.1745E+02	.1881E-00	.2977E+03	.1599E+02	.1426F+01	.5086F+00	.1476E-04	.9358E-02
	.2668E-02	.1940E+00							
.2470E-01	.5890E+00	.1765E+02							
	.5868E+00	.1740E+02	.1900E-00	.2982E+03	.1607E+02	.1347E+01	.5154F+00	.1514E-04	.9230E-02
	.2179E-02	.2469E+00							

DIFFERENCES:

MEAN	.8367E-03	.1352E+00
RMS	.1122E-02	.2725E-00
CHISQ	.4695E-04	.1241E-01

.2047E-03	.7950E+00
.3022E-03	.5186E+00
.7550E-03	.8484E-01
.7353E-03	.3526E-01
.8054E-03	.1553E-01
.6950E-03	-.1699E-01
-.6600E-05	-.5552E-01
.7727E-03	-.6673E-01
.1950E-03	-.5027E-01
.9210E-04	-.4390E-02
.1343E-02	.6706E-01
.9740E-03	.1295E+00
.2668E-02	.1940E+00
.2179E-02	.2469E+00

13 DEGREES OF FREEDOM.

APPENDIX D

THERMAL ANALYSIS

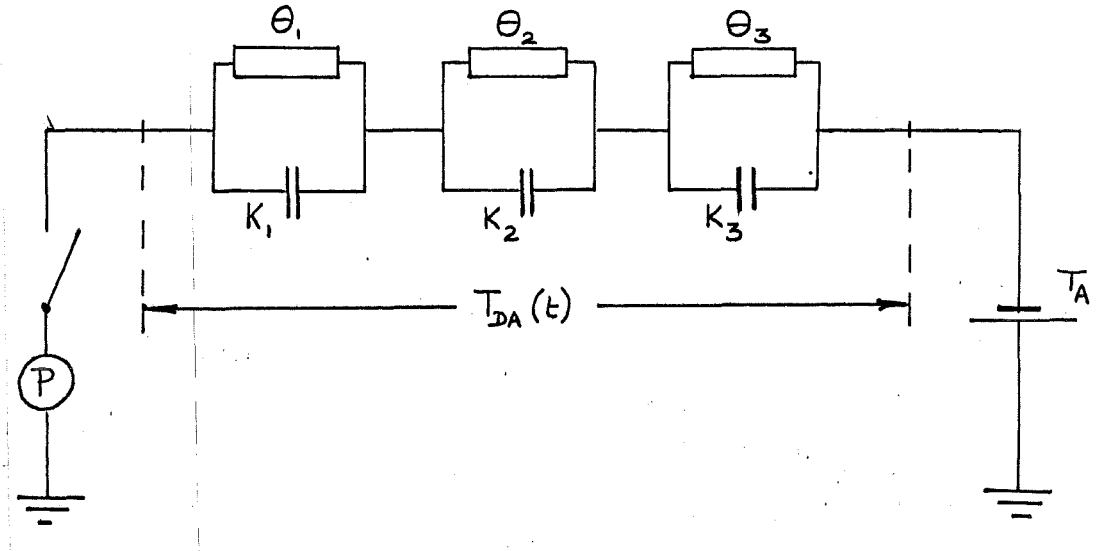


Figure 56

Figure 56 shows a thermal equivalent circuit for the diode, developed from the model of Strickland[73]. The power dissipation P(Watts) is analogous to current in an electrical network, thermal resistance Θ (^{o}C watt^{-1}) is analogous to electrical resistance, thermal capacitance K (joule $^{o}C^{-1}$) is analogous to electrical capacitance, and temperature T(^{o}C) is analogous to voltage. T_{DA} (t) is the temperature difference between the metal semiconductor barrier and the ambient, which is a function of time. T_A represents the constant ambient temperature.

The number of Θ_n K_n pairs used in the model depends upon the accuracy of representation required. Many previous treatments[74, 75] have associated the Θ_n and K_n with parts of the physical structure of the device. (eg, Θ_1 the spreading resistance through the silicon from the active region to the substrate, Θ_2 the silicon substrate to metal header bond resistance, Θ_3 the header to ambient resistance). A more general treatment is to use the experimental measurements to determine

the number and value of components needed .

The sum $\sum_n \theta_h = \theta_{DC}$ where θ_{DC} is the total thermal resistance which can be determined by measuring T_{DA} under a steady power dissipation P, $\theta_{DC} = \frac{T_{DA}}{P}$. The other components can be determined from the temperature decay of the diode after an instantaneous removal of the power dissipation at a time designated as zero. The experimental cooling curve (plot of ln T_{DA} against t) should approach a straight line (see Figure 32 Chapter 5 for an experimental result) which will represent the contribution of the network with the largest time constant $\tau_{TH} = \theta_m K_m$ The difference between the cooling curve and the straight line will represent the contribution of networks with shorter time constants. The difference can be plotted again on a logarithmic scale against time and the plot should approach a straight line representing the contribution of the network with the second largest time constant. This procedure can be continued until a straight line plot is obtained which continues down to time zero, or, until the temperature differences are of the same order as the experimental error.

Once the thermal network has been established, then the thermal response of the system can be predicted for sinusoidal or step changes in the power dissipation. In general, the magnitude of the effective thermal impedance θ_w appropriate to a sinusoidally varying component of power dissipation P_W at a frequency w, will be less than θ_{DC}. At a frequency of 4 kHz the appropriate value[72] of θ_w is expected to be of the order of $10^{\circ}C$ watt^{-1} which corresponds to the physical model of thermal spreading resistance through the silicon $\theta_1 = \frac{s}{2D}$ which is calculated to be $13^{\circ}C$ watt^{-1} for D = 260 μm (diode diameter) and s^{-1} = 1.45 watt cm^{-1} $^{\circ}C^{-1}$ (thermal conductivity of silicon[40]). The experimentally determined values of θ_{DC} are of the order of $200^{\circ}C$ watt^{-1} (see Section 5.1.4 (c) Chapter 5).

ADDENDUM

Limitations of the theory due to hot electron effects.

In the thermionic-diffusion theory developed in Appendix A, the electron temperature T_e was assumed equal to the lattice temperature T_o. However, when the electrons move under the influence of an electric field, they gain energy so that their effective temperature is increased.[81] One result is that electron mobility μ_n is no longer constant, but becomes a function of field through its dependence on T_e and this is known as the hot electron effect.

In the case where the hot electron effect is neglected, the current density J_n is given by

$$J_n = q n \mu_n E + q D_n \frac{dn}{dx}$$

and D_n and μ_n are connected by the Einstein relation $D_n = \frac{kT}{q}\mu_n$. In a metal semiconductor barrier, despite the large built-in electric fields, when $J_n = 0$ μ_n and D_n must have their equilibrium values because the electron temperature must be everywhere equal to the lattice temperature. However when a current flows, the electron temperature T_e may change from T_o and μ_n and D_n are then functions of T_e. Under these conditions, the current density is given by

$$J_n = q n \mu_n(T_e) E + q \frac{d}{dx}\left(n D_n(T_e)\right)$$

The electron temperature is evaluated by considering the equation of conservation of energy for electrons

$$J_n E = n B(T_e) + \frac{d}{dx} S(T_e)$$

where $nB(T_e)$ is the rate at which electrons lose energy to the lattice by electron phonon collisions and $S(T_e)$ is the flux of energy in the positive x direction.

Calculation of β

In the discussion of results (Chapter 6) experimental values of

$\beta = \frac{q}{kT}\left(V_B - V_F - V - \frac{kT}{q}\right)$ are quoted. The value of V_B used in this expression was taken from the appropriate I-V characteristics (± 5 mV error) V_F was calculated as $\frac{kT}{q} \log_e \frac{N_c}{N_D}$ where the donor concentration N_D was found from the C-V measurements. V was taken as $V_m - I_m R_{ES}$ and hence was dependent upon the value of R_{ES} which was obtained from the AC Resistance measurements. The possible error in β arising from error in V_B and V_F was of the order of $\pm$ 0.4 ($\pm$ 10 mV) independent of current , whereas the error due to R_{ES} error would increase at high currents. However, even at 10 mA an error of $\pm$ 2.5 Ω in R_{ES} would only cause an error of $\pm$ 1.0 in β .Thus the maximum error in β was of the order of $\pm$ 1.4 .

There is some doubt as to whether the -kT/q term arising from consideration of the effect of the reserve region should be included in the expression for β . Although the reserve region reduces the effective surface electric field, β arises from the potential change through the barrier, and so will not be affected in the same way. This would contribute an additional uncertainty in β of 1.0 .

Physical significance of $\beta \leq 0$

For applied voltages such that $\beta > 0$, there is still a depletion region in the semiconductor which limits the current flow in addition to the effect of the series resistance of the bulk semiconductor. When the applied voltage is such that $\beta = 0$, then the depletion region has been removed, and the thermionic-emission theory suggests that there is no barrier to current flow other than the bulk semiconductor and the current density should be $n\bar{v}/4$ where n is the electron density in the conduction band, and $\bar{v}$ is the average thermal velocity of the electrons in the semiconductor.

The experimental results suggest that this current density has not been reached at the flat band condition $\beta = 0$, presumably because

(i) the diffusion mechanism has reduced n at the surface, and (ii) electron 'cooling' effects have reduced $\bar{v}$ below its value in the bulk semiconductor. Hence the 'bottleneck' to current flow has not been completely removed at $\beta = 0$, and for additional increases in current flow, a component of the applied voltage appears across the barrier in addition to the flat band voltage. Negative values of β indicate the size of this additional component in units of kT/q. It is not suggested that the additional voltage is in any way due to the creation of a negative space charge region near the barrier.

REFERENCE

(81) STRATTON R., Phys. Rev. 126, 2002 (1962)

APPENDIX E

PUBLISHED PAPERS

PAPER 1

'CURRENT DIFFUSION EFFECTS IN TITANIUM N SILICON SCHOTTKY DIODES'
Reprinted from Solid State Electronics, Volume 17, 1974.

PAPER 2

'EVIDENCE FOR CURRENT DIFFUSION EFFECTS IN SILICON SCHOTTKY BARRIERS RESULTING FROM MEASUREMENTS ON TITANIUM-SILICON DIODES'
Reprinted from Institute of Physics Conference Series No. 22, Metal Semiconductor Contacts, U.M.I.S.T. Manchester, April 1974.