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Ultra High Density Scanning Electrical Probe Phase-Change Memory for Archival Storage

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The potential for using probe-based phase-change memories for the future archival storage at densities of around 1 Tbit/in.^{2} is investigated using a recording medium comprising a Si/TiN/DLC/GeSbTe/diamond-like carbon (DLC) stack together with a conductive PtSi tip for writing and reading. Both experimental and computational simulation results are presented. The simulations include a physically-realistic threshold switching model, as well as the effects of thermal boundary resistance and electrical contact resistance. The simulated bit size and shape correspond closely to that written experimentally.

The archival sector is becoming increasingly important, due to the introduction of legal requirements governing the storage of data, but also as a consequence of the ever-increasing amount of digital data generated in our everyday life. Probe storage, in which a two-dimensional array of probes write and read data in parallel, as exemplified by IBM's prototype probe-storage system,[1)] has the potential to provide the huge capacities needed for digital archiving. A putative archival probe storage system might have a capacity of 200 to 1000 Tbyte (implying a multiple medium/array format), a streaming data rate of around 500 Mbyte/s, a media/tip lifetime of 20 to 50 years, a read cyclability of 10^6 and a power consumption of less than 300 W. To achieve such performance targets requires the ability to write and read bits at densities of at least 1 Tbit/in.^{2} and at data rates of at least 1 Mbit/s per probe (and an array size of 1000 to 10,000 probes), while at the same time "guaranteeing" long media and probe (tip) lifetimes. We address the achievement of such targets by the use of wear-resistant electrical write/read probes together with specially designed phase-change storage media that have previously demonstrated the potential for ultra high density storage.[2–4)]

Invariably in probe storage the most significant factor in determining the size of a recorded mark, and hence the achievable storage density, is the tip size of the probe itself. However, in a practicable probe storage system a probe tip may have to endure several kilometres of scanning, so a wear-resistant tip is required. Fortunately there has been much recent progress in the development of ultra sharp, wear-resistant tips.[5)] While physically sharp tips are a pre-requisite for techniques that rely on the formation of physical indents to store data, this is not necessarily the case for electrical probe storage (the subject of this note). In electrical probe storage it is the electrical contact area that is important, rather than the physical contact area. Thus, tip designs are possible that have small electrical contact area, for high density writing and reading, but a larger physical contact area, for the reduction of tip-medium pressure (and potentially therefore tip-media wear). Such tips have been developed by IBM Zurich, with a small, highly conducting PtSi region "encapsulated" by a much larger, non-conducting SiO_2 region; these tips have far superior wear characteristics compared to conventional tips,[6)] and have been used in this note to write and read data in phase-change media. The phase-change medium stack used here consists of a 10 nm $Ge_2Sb_2Te_5$ (GST) layer sandwiched between a 4 nm diamond-like-carbon (DLC) capping layer and a 20 nm DLC underlayer, on a 10 nm TiN bottom electrode on the top of a Si substrate. It is well-known that chalcogenide alloys such as GeSbTe are easily oxidized, resulting in a degradation of their properties, and therefore need to be encased by some form of protective layer. DLC films are a good choice for protective layer since they can be readily fabricated with a wide range of electrical (and thermal) conductivities, and present a good barrier to oxidation.[7)] For the experimental writing and reading of bits we used a 60 nm contact diameter PtSi tip, write voltages (applied between the tip and the TiN electrode) in the range 3 to 5 V and pulse durations of around 1 μs. A schematic of the recording arrangement is shown in Fig. 1, along with both experimental and simulated mark (bit) shapes as well an experimental current–voltage (I–V) curve.

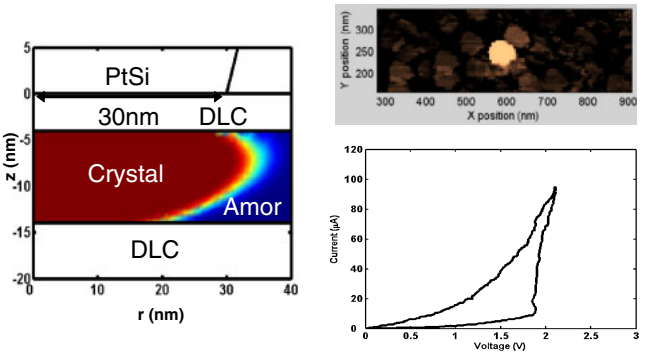

Fig. 1. (Color online) (a) Simulated crystalline bit (top left) and (b) experimentally recorded bit readback (top right) using current contrast with the maximum readout current being approximately 8 μA (readout voltage = 1 V); also shown [(c) bottom right] is the experimental I–V curve for the recording medium, showing the characteristic threshold-type switching exhibited by GeSbTe type materials.

The physical mechanisms that determine the write and read performance of electrical probe memories using phase-change media involve electrical, thermal and phase-transformation processes. We have previously described a comprehensive (pseudo-three-dimensional) computational (COMSOL Multiphysics™) model for all such processes, simultaneously solving the (time-resolved) Laplace, heat

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conduction and Johnson–Mehl–Avrami–Kolmogorov (JMAK) equations.[2] In this note however we have improved our previous simulation capabilities by including a more physically-realistic model for the well-known threshold switching effect that occurs in amorphous chalcogenides.[8] Accordingly the electrical conductivity σ_{am} of the GeSbTe layer in the amorphous phase is described by the equation:

$$\sigma_{am}(T,E) = E^{-1} \cdot 2q(N_{T1} + N_{T2}) \frac{\Delta z}{\tau_0} \exp\left(-\frac{E_C - E_F}{kT}\right) \times \sinh\left(\frac{qE}{kT}\frac{\Delta z}{2}\right)(1+\gamma), \quad (1)$$

where (as explained in ref. 8) N_{T1} (here $5 \times 10^{24}\,m^{-3}$) is the concentration of a deep traps at energy E_{T1} aligned with the Fermi level, N_{T2} (here also $5 \times 10^{24}\,m^{-3}$) is the concentration of a shallow traps at energy E_{T2} close to the conduction band, E is the electric field inside the GeSbTe layer, q is the unit charge, Δz is the intertrap distance (5 nm), τ_0 is the attempt-to-escape time for a trapped electron (10^{-15} s), γ is a non-equilibrium term and $(E_C - E_F)$ was taken to be 0.35 eV. Recently, it has also been shown that thermal boundary resistance (TBR) plays a significant role in determining the temperature distribution within phase-change devices.[9,10] We have therefore also modified our previous model to include TBR effects and found that the temperature in the recording layer is particularly affected by the TBR at the interface between the bottom DLC layer and GeSbTe film. The value of TBR used in the simulations presented here is $2.5 \times 10^{-8}\,m^2\,K/W$, taken from ref. 10. Another practical complication that should be taken into account is the electrical contact resistance between the tip and the sample (capping layer in our case), since this increases the whole system resistance and can influence written mark size and shape for a given write pulse. In our simulation, the electrical contact resistance is calculated directly using[11]

$$R_{contact} = \frac{\rho_{sample} + \rho_{tip}}{4\left\{r^2 - \left[r - \left(\frac{9F^2}{16rE^{*2}}\right)^{1/3}\right]^2\right\}^{1/2}}, \quad (2)$$

where ρ_{sample} and ρ_{tip} are the resistivities of the sample and tip, respectively, r is the radius of tip apex, F is the tip loading force, and E^* is the effective Young's modulus (here 5 GPa). According to this expression, the value of the contact resistance for the PtSi tip is approximately 80 kΩ for a tip force of 300 nN (typical for that applied during writing) and for $\rho_{sample} = 0.01\,\Omega m$ and $\rho_{tip} = 0.3 \times 10^{-6}\,\Omega m$. The predicted written bit size and shape, using this more physically-realistic recording model, is shown in Fig. 1(a), assuming a 4 V, 1.0 µs write pulse (see Table I for material parameters used in the simulation). The GeSbTe layer was assumed initially to be in the amorphous phase, and it can be seen that a crystalline mark of approximately 60 nm in diameter is formed and extends throughout the entire thickness of the GeSbTe layer (this is important to ensure good readout contrast — see ref. 2). Experimental recording experiments were also carried out using this same media structure and PtSi tip design. A typical experimentally recorded bit is shown in Fig. 1(b), in this case for a write pulse of 2.8 V [chosen to be above the threshold voltage measured from "static" *I–V* curves — see Fig. 1(c)] and 1.0 µs duration (chosen to meet a requirement of ~1 Mbit/s data rate per tip), where it can be seen that the bit is also around 60 nm in diameter and exhibits good electrical (current) contrast, in line with our simulations. Note that the energy needed to record a bit is quite small, being only 0.33 nJ in the experimental case and 0.53 nJ for the simulation (corresponding to write currents of 117 and 132 µA, respectively). This implies a relatively low writing power for a "real" system [e.g., at 1 Mbit/(s·tip) the total write power would be only around 330 mW for 1000 tips operating in parallel].

Table I. Characteristic parameters used in the simulation.

	Tip	Capping	Under	Bottom electrode	Substrate
Thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$)	25	5	10	12	149
Electrical conductivity ($\Omega^{-1} \cdot m^{-1}$)	3.3×10^6	100	200	5×10^6	N/A
Density ($kg \cdot m^{-3}$)	12400	2800	2800	5400	2330
Heat Capacity ($J \cdot kg^{-1} \cdot K^{-1}$)	250	540	540	400	720

In summary, the recording performance of a scanning probe phase-change memory based on a Si/TiN/DLC/GeSbTe/DLC medium stack and using a PtSi electrical tip for writing and reading has been investigated both experimentally and by simulation. We have concentrated on a write-once type system where crystalline marks are written into an amorphous starting matrix. We have shown that a crystalline mark size as small as 60 nm can be readily produced using a relatively low voltage pulse of around 1 µs in duration, and that smaller tip contact areas would result in smaller written marks, demonstrating the capability of this technique in achieving 1 Tbit/in.^{2} areal density and 1 Mbit/(s·tip) data rate. Combining the methods used here with the recently developed mark-length recording strategy for phase-change probe storage systems,[3] which has the potential to increase densities by a factor of 50 to 100%, offers the capability for multi-Terabit-per-square-inch probe storage.

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