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SELF-ALIGNED GALLIUM ARSENIDE HETEROJUNCTION BIPOLAR TRANSISTOR USING REFRACTORY METALLISATION.

A thesis submitted by

Jean Marie Michel Desire, B.Eng (Hons)

in partial fulfilment of the requirements for the

Degree of Master of Philosophy

of the Council for National Academic Awards

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I dedicate this thesis

to

my Little Lady

MARIE JOELLE

who, with her unfailing support,

constant care and patience,

and her righteous will to fight

past hope and reason,

inspired me to complete this work.

May Our Lord GOD bless her always

and

May the light that shines in her lovely eyes

shine on me

forever.

SELF-ALIGNED GALLIUM ARSENIDE HETEROJUNCTION BIPOLAR TRANSISTOR USING REFRACTORY METALLISATION.

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ABSTRACT

Improvements in epitaxial growth and processing technologies have revived a great deal of interest in the heterojunction bipolar transistor (HBT). In this project, AlGaAs/GaAs HBTs have been fabricated using a new self-aligned process which exploits the characteristics of some refractory metals deposited by sputtering to obtain a T-shaped contact structure for the emitter. Wet and dry etching techniques were used to fabricate the T-shaped contact.

A refractory metallisation system consisting of sequentially sputtered layers of Ge/Mo/Ni was investigated for contacting the emitter of the transistor. After alloying in a thermal furnace at 750°C for 30 minutes in a nitrogen atmosphere, a low specific contact resistance of 2×10^{-6} ohm-cm^2 was measured by standard transmission line model (TLM) for measurement of contact resistance. A metallisation system consisting of sequentially evaporated Au/Zn/Au was used for the base and Ni/AuGe/Ni/Au was used for the collector. Alloying with the same conditions as above gave specific contact resistances of 1.2×10^{-6} ohm-cm^2 for the base and 8.6×10^{-6} ohm-cm^2 for the collector.

As an alternative to ion implantation, zinc diffusion was used as an alternative technique to dope the base contact region. The acceptor concentration profile of the diffused region was studied by 'Hall and Stripe' technique and a surface concentration of 1×10^{20} cm^{-3} was measured. This highly doped base contact region can be used to achieve low ohmic contact to the base. Results show that for devices designed with similar dimensions for both processes, the new self-aligned process shows a net improvement in the frequency response of the devices (f_t= 10.7GHz and f_{max}=9.8GHz for self-aligned and f_t=8.0GHz and f_{max}=7.9GHz for conventional 8um HBT).

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CHAPTER 1: INTRODUCTION

Silicon (Si) is now the most important material for semiconductor technology and Gallium Arsenide (GaAs) has been, since the early beginnings of this technology, one of the other materials in the limelight. Some of the electronic properties of GaAs are very promising to the device designer when compared to those of Si, e.g. the larger bandgap, which allows operation over an even wider range of temperature and implies that the intrinsic carrier concentration in GaAs is low enough that it is possible to make very high resistivity, semi insulating GaAs, which helps reduce device and interconnect capacitance to a low level. Also, higher electron mobility and high peak electron velocity in the bulk material enable faster operation at lower power. Finally, the band structure of GaAs and related compounds allows light-emitting devices to be made.

However, GaAs also has some shortcomings when compared to Si. First of all, it is much more difficult to produce single crystals of GaAs than of silicon and the crystal growth technology itself is relatively much more expensive for the former. Furthermore, during device manufacturing at elevated temperatures, additional difficulties come from the dissociation of the GaAs compound because of the high volatility of As as well as the high susceptibility of GaAs substrates to slippage.

Despite its shortcomings, GaAs has found its application in both optoelectronics and high frequency and even ultra-high frequency discrete devices [1]. Integrated circuits based on GaAs have been developed during recent years, but so far, these ICs do not overcome the frequency (or switching speed) limitation,

mainly because of the time constant associated with the large structures (and therefore large parasitic capacitances and resistances) in comparison to the very high frequency required. It is therefore essential to develop new technologies that will enable the fabrication of smaller devices down to submicron dimensions. One such technology is the `self-aligned´ fabrication process which allows more than one process step to be performed with only one mask, thus resulting in a minimum number of process steps and a possible increase in yield.

Current practice for the fabrication of NPN HBTs utilises sequentially deposited layers of AuGe and Ni for n type GaAs, with subsequent annealing above the AuGe eutectic temperature to produce low ohmic contact resistance. The disadvantages of this liquid alloying technique are that due the exact and restrictive temperature control, the subsequent interfaces are very irregular (non planar) and there is lateral spreading of the contact area. For the self-aligned HBT technology where high temperature ($\geq 700^{\circ}C$) processing steps are required, it is essential to use metallisation schemes involving solid state diffusion. Refractory alloys such as germanides (analogous to refractory silicides for silicon devices) are ideal for GaAs technology.

HBTs have recently come to the forefront of semiconductor technology as devices for very high speed applications [2,3]. AlGaAs/GaAs HBT structures have a number of inherent advantages over Si bipolars, including the following:-

- Due to the wide bandgap emitter, a much higher base doping concentration can be used, decreasing the base resistance. The emitter injection efficiency is not impaired because the barrier

for hole injection at the base-emitter junction is larger than the corresponding barrier for electron injection.

- Emitter doping can be lowered, and minority carrier storage in the emitter can be made negligible, reducing base-emitter capacitance.

- Semi-insulating substrates help reduce pad parasitics and allow convenient integration of devices.

- Improved frequency response because of higher current gain and lower base resistance.

- Wider temperature range of operation.

The performance of today's HBT is determined not only by the vertical structure of the layers but also by the dimensions of the transistor. By applying a `self-aligned' fabrication process to HBTs, it is possible to reduce the device dimensions and the the associated parasitics considerably, thus resulting in higher speed performance.

In comparison with FETs, HBTs have many intrinsic advantages:

- The key distances that govern electron transit time are established by epitaxial growth, not by lithography, which allows high f_t with modest processing requirements. High performance may be obtained without submicrometre lithography;

- The "control region" of the device, the base-emitter junction, is very well shielded from the output voltage, leading to low output conductance g_0; taken together with the high transconductance g_m, enormous values of voltage amplification factor g_m/g_0 are attainable;

- Breakdown voltage is directly controllable by the epitaxial structure of the device;

Principal disadvantages of HBTs when compared to FETs are:

- Finite current gain at dc due to electron-hole recombination;

- The need to access several different layers of the vertical structure, which can lead to non-planar structures in some circumstances. This non-planarity complicates device processing, although it does not preclude monolithic integration of HBTs.

This thesis describes one possible self-aligned process for the HBT. Efforts are concentrated upon the initial part of the process whereby a T-shaped contact structure of refractory metals is defined for the emitter of the HBT. This contact structure is then used as a mask to the implantation of the base contact regions, thus allowing for critical alignment of the emitter contact to the active emitter area and the base contact and consequently reducing the number of fabrication steps. The concept of self-alignment is extended into subsequent steps of the fabrication and where the possibility arises, alternative routes are studied.

CHAPTER 2: LITERATURE SURVEY

2.1.0: Aluminium Gallium Arsenide (AlGaAs)/ Gallium Arsenide (GaAs) heterojunction bipolar transistors.

Heterojunction transistors have been widely studied since Shockley proposed wide-gap emitter transitors with a high injection efficiency of minority carriers [5]. The heterojunction transistor structure proposed by Kroemer [6] in 1957 promised improved performance over the transistor structures in use then. Since that time, considerable effort has been put into further investigations of AlGaAs/GaAs HBT theory [7-29] and structures [30-59]. Heterojunctions with well understood electrical properties have been available only since the advent of molecular beam epitaxy (MBE) in the 1970's, and more recently by means of metal-organic vapour phase epitaxy (MOVPE). Sze [7] deals with principles of semiconductor devices, which can be applied to heterojunction devices, Milnes and Feucht [8] discuss heterojunctions, Casey and Panish [9] provide information on heterojunction material parameters, and Harrison [10] discusses semiconductor band structure, including heterojunctions. Although various methods of fabricating heterojunctions have been used, notably metal-organic chemical vapour deposition (MOCVD), liquid phase epitaxy (LPE) and vapour phase epitaxy (VPE), this literature survey will focus mainly on AlGaAs/GaAs HBTs produced by MBE, but the principles and fabrication techniques can be applied to material and devices produced by the other systems mentioned.

Anderson [11] developed a model in which the conduction band discontinuity at the interface of the heterojunction was assumed to be the difference between the electron affinities of the two materials forming the junction. Later, Kroemer [12] pointed out that it would be desirable to be able to calculate the relative mis-alignment of the bands of an abrupt heterojunction from the bulk properties of the two semiconductors. Another model [13] assumes that the mechanisms for Schottky barrier formation and heterojunction formation are the same and can be deduced from the arguments based on the effective density of states. Other approaches [14] use pseudo-potential calculations to determine these quantities. Uncertainties, both experimental and theoretical, are so large as to prevent one distinguishing between the models,. as pointed out by Freeouf and Woodall [15], and the most simple model based on Anderson's rule [11] will be assumed to be correct for our purpose.

Recent theoretical investigations of some properties of HBTs have been carried out as follows:

Details of the temperature dependence of current gain in HBTs were reported for the first time by Chand et al. [16].

The high power performance of a microwave HBT was first demonstrated by Kim et al. [17], who showed that the device was suitable for pulsed operation and that its power generation capability is potentially better than that of a conventional GaAs MESFET.

While investigating emitter-base bandgap grading effects on HBT characteristics, Yoshida et al. [18] found that the bandgap grading influenced not only the electron injection but also both

the carrier recombination and the hole injection, thus resulting in a significant common-emitter current gain dependence on the graded layer thickness.

Yamauchi and Ishibashi [19] derived equivalent circuit parameters of graded bandgap base HBTs by analysing static and microwave device characteristics. Additionally, they simulated ECL ring oscillators using these parameters and found that the simulated propagation delay time of ECL gates agreed well with experimental results.

The influence of an undoped spacer layer in the emitter-base junction on HBT characteristics was investigated experimentally and theoretically by Ito [20]. He found that the ideality factors of the base current became larger according to the spacer layer thickness and explained such behaviour in terms of a localised recombination in the spacer layer at the hetero-interface.

Rao et al. [21] fabricated HBTs with non-alloyed graded regions for ohmic contacts to the base and emitter. The graded-gap contacts were capable of withstanding high temperature processing and contact resistivities of 5×10^{-7} ohm-cm^2 and 3×10^{-6} ohm-cm^2 were measured for n type and p type contact structures respectively.

A description and analysis of the theories governing the nature and magnitude of the conduction and valence band discontinuities in heterojunctions was given by Unlu and Nussbaum [22].

Baets [22b] presented a classification of heterojunctions in III-V semiconductors and discussed their advantages. He also studied a limited set of devices that take advantage of the main

properties of the III-V heterojunctions and described the application of heterojunctions in laser diodes.

Dagli [23] used device physics to obtain an expression for the small signal output impedance of an HBT. He found that, when external parasitics are sufficiently reduced so that intrinsic time delays become the dominant limitations to figh frequency performance, the output resistance can be negative over certain bands of frequencies due to transit time delays. Recently, Dagli et al. [24] explained the above mentioned behaviour in terms of the phase delay of the common base current gain. They also discussed the generality and relevance of these observations to other types of transistors and the utilisation of the negative output conductance to enhance high frequency operation.

In order to, investigate the effect of a graded layer on collector current uniformity, Takano et al. [25] fabricated abrupt HBTs and graded HBTs by MOCVD. They demonstrated that bandgap grading in the emitter of the HBTs improved the uniformity of the collector current as well as the current gain and also the standard deviation of the threshold voltage.

Masselink et al. [26] studied electron velocity at high electric fields in AlGaAs/GaAs modulation-doped heterostructures. Their measurements indicated that the peak velocity for electrons in the heterostructures was lower than for electrons in bulk low-doped GaAs and they explained this result in terms of modified intervalley transfer, real space transfer, and an enhanced scattering with polar optical phonons.

The high frequency performance limitations of millimetre-wave HBTs were investigated by Das [27]. He combined charge

control and carrier velocity saturation concepts to calculate the performance limitations of HBTs with submicrometre emitter stripe width, and ultra submicrometre base and collector-base depletion widths and suggested that any further improvements of f_{max} in HBTs will depend on the future technological advancements needed to effectively reduce the emitter contact resistance, the extrinsic base resistance, the metallisation resistance and the collector-base extrinsic capacitance elements.

The effect of off-axis implant on the characteristics of advanced self-aligned bipolar transistors utilising a sidewall-spacer technology was studied by Chuang et al. [28]. Results showed that the off-axis implant caused orientation-dependent perimeter punchthrough at one of the emitter edges and orientation-dependent perimeter tunneling at the other emitter edge.

The extensive investigations of the theory of HBTs are of course very strongly related to specific device structures and fabrication process parameters, and what appears to be the first HBT structure having application for either high frequency operation or integration with certain types of light emitting devices was proposed by Dumke et al. [29]. The structure involved liquid phase epitaxially grown layers of GaAs and AlGaAs and the devices were fabricated by first depositing onto the substrate a large area ohmic contact which served as the collector contact. Then, the emitter contact was deposited through a metal mask and the latter contact also served to protect the emitter region when the unwanted part of the emitter layer was removed by a selective etching technique. Following that, the revealed portions of the

base layer were contacted by a final metal deposition. The most important advantage of the structure was that it enabled a thin, (1500Å) highly doped p type base region to be obtained.

Using the same LPE technique for fabricating the HBT layers, Konagai and Takahashi [30] used two kinds of etchants to expose the p type base region and found that a $KI+I_2$ solution was a useful selective etchant for $Al_x Ga_{1-x} As$ for $x>0.4$ and $(NaOH+H_2O_2)$ solution for $x<0.4$. They thus obtained thinner base widths ($W_b \leqslant 1um$) and higher common emitter current gains ($\beta=350$) than the structures proposed by Dumke et al. [29]. A schematic of the HBT structure fabricated by Konagai and Takahashi is shown in figure 2.1.0 .

Mesa type transistors (figure 2.1.1) were processed on LPE material by Bailbe et al. [31]. A large area ohmic contact was first deposited on to the back of the collector and to the emitter. The emitter contact was then defined by photolithography and etching, followed by the first selective mesa etch to the base using $KI+I_2$ solution. The emitter was then protected by photoresist and the base layer metallised, followed by the base contact engraving and second selective mesa etch to the collector. Best common emitter current gain value for a device with base width $W_b=0.5um$ was 850.

Still exploiting the LPE grown layer structure, Beneking and Su [32] adopted an interdigitated mask to further reduce the base resistance. The collector and emitter contact were defined as before [29,30], but the base contact regions were heavily doped p type by diffusing zinc through windows defined in a layer of SiO_2 150nm thick. Multilayer metallisation consisting of Ni/AuZn was

FIGURE 2.1.0: Schematic drawing of the HBT structure fabricated by Konagai et al. [Ref:30]

FIGURE 2.1.1 : Schematic drawing of the HBT structure fabricated by Bailbe et al. [Ref: 31]

used for the base contact. Current gains h_{FE} ranged from 20 to 300.

Ito, Ishibashi and Sugeta [33,34] fabricated HBTs (figure 2.1.2) on MBE material using conventional lift-off processes. Base and collector layers were recessed by wet chemical etching. Multilayered metallisations used to realise low ohmic contact resistance on n type and p type layers were AuGe/Ni and Cr/Au respectively. Proton implantation was used to provide interdevice isolation. A cut-off frequency f_t=25GHz was achieved. Ito et al. [34] also investigated current gain in HBTs with heavily doped bases. They used AuGe/Ni/Ti/Au for the emitter and collector and Cr/Au for the base. Practical high current gain ($\beta \geqslant 80$) over a wide temperature range was demonstrated with base doping of 2×10^{19} cm^{-3}. Ito et al. [35] also fabricated devices (figure 2.1.5) that demonstrated no emitter crowding effect nor Kirk effect. The limitation on f_t in those fabricated devices was found to be caused mainly by the emitter series resistance.

A novel self-aligned base structure for HBTs with a buried V-groove isolation (figure 2.1.3) was proposed and achieved by Ohshima et al. [36]. They used an SiO_2 dummy emitter as an implantation mask for Mg ions. Rapid thermal annealing was then employed to form self-aligned p^+ base extrinsic regions within the emitter. The dummy emitter was then replaced with a AuGe/Au emitter. The V-groove buried silicon nitride device isolation process was then performed. Oxygen implantation is used to isolate the base-collector extrinsic region and reduce junction capacitance. Via-hole etching followed by metallisation was used to make contact to the collector layer. Using this fabrication

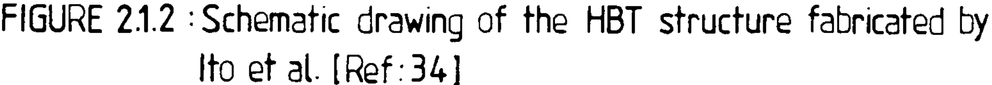


FIGURE 2.1.2 : Schematic drawing of the HBT structure fabricated by Ito et al. [Ref: 34]

FIGURE 2.1.3 : Schematic drawing of the HBT structure fabricated by Ohshima et al. [Ref: 36]

process, a 1/8 frequency divider with an input frequency of more than 20GHz was realised and the self-aligned HBTs were of the order of 1-6 times faster than the conventional HBTs.

Dubon-Chevallier et al. [37] reported on the first HBT with base doping level as high as 2×10^{20} cm^{-3}. Material growth conditions were investigated to keep perfect surface morphology and to avoid dopant diffusion phenomenon even at ultra high doping levels. Maximum DC current gain of 15 was observed for a base thickness of 450Å. With an emitter-base capacitance down to $1fF/\mu m^2$ and a base sheet resistance below 150Ω/square, such HBTs structures (figure 2.1.4) were optimised for high speed logic and microwave applications.

Daoud-Ketata et al. [38] presented a new self-aligned technology using refractory metals to contact the emitter layer, thus enabling the annealing process subsequent to p type implantation, as the contact also acts as a mask for the implantation. The HBT structure is shown in figure 2.1.6 .

A multiple self-alignment process for HBTs using one mask was developed by Inada et al. [39] to form emitters, emitter contacts, buried small collectors, base contacts and base contact leads. A schematic of the HBT structure is shown in figure 2.1.7.

Malik et al. [40] worked on graded bandgap bases fabricated by MBE. They found that the use of an undoped setback layer of 200-500Å to offset Be diffusion in the emitter resulted in significant current gain increases. Typical processing steps included Zn diffusion to make contact to the base, wet chemical etching to reach the collector and the isolation regions, silicon nitride patterning to serve as dielectric crossovers on the

FIGURE 2.1.4 : Schematic drawing of the HBT structure fabricated by Dubon-Chevallier et al. [Ref: 37]

FIGURE 2.1.5 : Schematic drawing of the HBT structure fabricated by Ito et al. [Ref: 35]

FIGURE 2.1.6 : Schematic drawing of the HBT structure fabricated by Daoud-Ketata et al. [Ref:38]

FIGURE 2.1.7 : Schematic diagram of the HBT structure fabricated by Inada et al. [Ref:39]

FIGURE 2.1.8 : Schematic drawing of the HBT structure fabricated by Malik et al. [Ref: 40]

FIGURE 2.1.9 : Schematic drawing of the HBT structure fabricated by Rezazadeh et al. [Ref: 41]

mesa edges and conventional lift-off processes to contact the emitter, base and collector. DC current gains up to 1150 were obtained. The device structure is shown in figure 2.1.8 .

In studying the role of electron traps in the DC performance of HBTs prepared by MBE, Rezazadeh et al. [41] parabolically graded the emitter-base junction and incorporated two 100Å undoped GaAs spacer layers before and after the base region. A mesa etching technique was used to fabricate the devices (figure 2.1.9) and ohmic contacts to the emitter and collector were provided by evaporation of Ni/AuGe/Ni/Au and to the base by Au/Zn/Au. Very high current gains of up to 3000 were obtained.

HBTs using a proton implanted external collector layer and a highly doped base layer were fabricated by Nakajima et al. [42], who investigated the influence of the proton implantation on the base-collector junction characteristics. Their devices (figure 2.1.10) produced an f_t of 50GHz and an f_{max} of 70GHz.

A fully planar HBT (figure 2.1.11) was fabricated by Tully [43,44]. The process utilised a two-step epitaxial deposition with an intervening selective ion implant of bases. The process, called the aluminum lift-off (ALL) process, involved refractory metal contacts. Large test devices fabricated had dc gains of $\beta = 600$.

Kim et al. [45] used selective wet chemical etching to delineate the emitter mesa and access the base and collector contacts. They obtained current gains up to $\beta = 2050$ and unity-current gain cut-off frequency $f_t = 24GHz$ for devices with the structure shown in figure 2.1.12 .

FIGURE 2.1.10 : Schematic drawing of the HBT structure fabricated by Nakajima et al.[Ref:42]

FIGURE 2.1.11 : Schematic drawing of the HBT structure fabricated by Tully et al.[Refs:43,44]

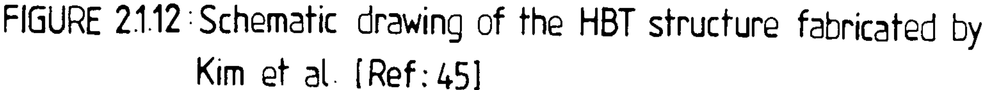


FIGURE 2.1.12 : Schematic drawing of the HBT structure fabricated by Kim et al. [Ref: 45]

FIGURE 2.1.13 : Schematic drawing of the HBT structure fabricated by Eda et al. [Ref: 46]

Emitter-base-collector self-aligned HBTs using wet etching processes were realised by Eda et al. [46]. The simple fabrication process produced HBTs with an f_t=18GHz but the process still needed to be optimised. A schematic of the structure of their device is shown in figure 2.1.13 .

Asbeck et al. [47,48] concentrated their efforts on MBE wafers. They used Be implantation to form the p^+ extrinsic base regions which make contact to the base layer. With the same photoresist pattern, oxygen was implanted deeper into the material to decrease the extrinsic base-collector capacitance. Via holes were etched into the wafer to make contact to the buried collector layer. Isolation was achieved principally by Boron bombardment of the surface outside the active transistor areas. The interlevel dielectric used was silicon nitride. Interconnect resistors were fabricated with NiCr. With a small emitter contact (1.6um x 5um), a maximum current gain of 30 and an f_t of 40GHz were obtained for devices with the structure shown in figure 2.1.14 . Asbeck et al. [49] also fabricated the first self-aligned HBT (figure 2.1.15) which included ion implantation to reduce the base resistance. With their substitutional emitter technique, the base implant and the emitter contact patterns were defined with the same mask. Arbitrary contact materials could be used, allowing optimisation of the contact resistances. They then improved on that same self-aligned HBT technology with a process based on the dual lift-off method [50] to produce devices with the structure shown in figure 2.1.16 . Extrapolated current gain cut-off frequency f_t of 55GHz and a maximum frequency of oscillation f_{max} of 105 GHz were obtained. Asbeck, Miller and

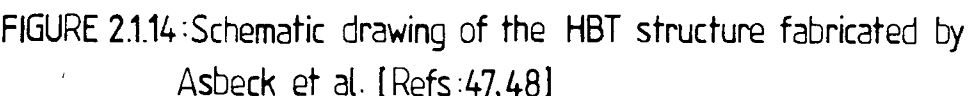
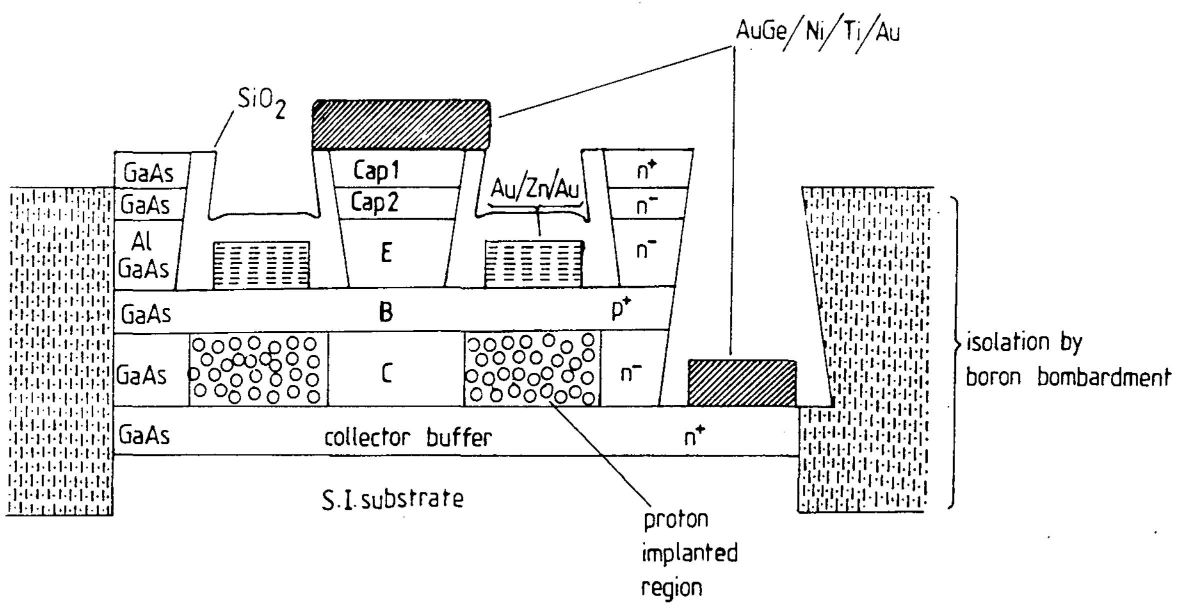


FIGURE 2.1.14: Schematic drawing of the HBT structure fabricated by Asbeck et al. [Refs: 47,48]

FIGURE 2.1.15: Schematic drawing of part of the HBT structure fabricated by Asbeck et al. [Ref: 49]



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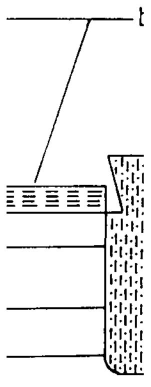

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Chang [51] also used a process which involved selective etching to define the base contact regions and they obtained a f_t of 45GHz was obtained with devices (figure 2.1.17) fabricated using this process.

Tiwari et al. [52,53] studied the transport and related properties of GaAs double heterostructure bipolar junction transistors with AlGaAs emitters and collectors (figure 2.1.18) utilising both graded and abrupt junctions. They demonstrated how the various transport and storage factors are interlinked with device design and technological factors. Tiwari [54] later demonstrated that large current densities in HBTs with heterostructure collectors caused an excess electron barrier leading to an increase in minority carrier charge storage in the base and a decrease in current gain of the device. The use of a p type refractory ohmic contact in self-aligned devices was also demonstrated by Tiwari et al. [55].

The fabrication of the first fully planar PNP HBT (figure 2.1.19) was reported by Sunderland et al. [56]. The devices were fabricated using ion implantation into AlGaAs/GaAs heterostructures grown by MOCVD. Incremental current gains of 100 were observed for transistors with 22µm x 4µm emitters. No emitter size effect was observed.

A self-aligned HBT technology using polyimide for insulating the emitter contact from the base contact was demonstrated by Morizuka et al. [57]. A 1µm emitter-width HBT with the structure shown in figure 2.1.20 produced a f_{max} of 86GHz. The process was also applied to the fabrication of frequency divider ICs, and an operation frequency of 18GHz was obtained with good

FIGURE 2.1.18 : Schematic drawing of the HBT structure fabricated by Tiwari. [Refs: 52,53]

FIGURE 2.1.19 : Schematic drawing of the HBT structure fabricated by Sunderland et al. [Ref: 56]

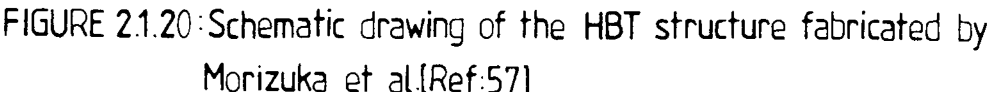


FIGURE 2.1.20: Schematic drawing of the HBT structure fabricated by Morizuka et al.[Ref:57]

FIGURE 2.1.21: Schematic drawing of the HBT structure fabricated by Hayama et al.[Ref:58]

reproducibility.

Structure optimisation, uniformity consideration, and high-speed circuit performance for an AlGaAs/GaAs HBT were reported by Hayama et al. [58]. The HBT was fabricated in a fully self-alignment manner using only a single photoresist mask for achieving submicrometre-dimension devices (figure 2.1.21).

Another self-aligned fabrication technolgy for AlGaAs/GaAs HBTs for high speed digital circuits was demonstrated by Nagata et al. [59]. They also demonstrated the possibility of combining the oxygen implantation technique [47,48] to this self-aligned structure, so that better switching speeds (<10 ps/gate) could be attained.

The early investigations of the mechanisms of heterojunctions and their use in bipolar transistor technology yielded an impressive amount of device physics analysis which suggested ways in which variation of certain physical properties could improve device performance. It is obvious from the above survey that technologies which have been developed over the past few years and those under investigation today are following a trend aiming at exploiting those physical properties to the full. The two main goals of the investigations are: (1) to obtain device geometry and structure control which will yield HBTs with high cut-off frequency and (2) to ensure that the technology is economically justifiable. Table 2.1.0 provides a brief summary of HBT structures fabricated to date.

FIGURE 2.1.22: Schematic drawing of the HBT structure fabricated by Nagata et al.[Ref:59]

TABLE 2.0.0: Summary of 'AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[30] Konagai and Takahashi	i) Deposit SiO_2; ii) Define base contact by etching AlGaAs with a suitable etchant; iii) Metallise emitter; iv) Metallise base; v) Metallise back collector.		Current gain varies as a fractional power of the emitter current and the value of this power is independent of temperature. Common emitter current gain β = 350 was observed in the transistor with a thin base base width ($W_b/L_n \simeq 0.1$).
[31] Bailbe et al.	i) Metallise emitter and back collector; ii) Photoengraving of emitter contact + selective mesa etch to the base; iii) Photoengraving and base contact definition; iv) 2nd selective mesa etch to the collector.		For circular transistors with a junction surface area $A_E \simeq 10^{-4}$ cm^2 and base thickness 0.5µm, performance was as follows: $(h_{FE})_{max}$ 850 & $(f_t)_{max}$ 1GHz.
[34] Ito et al.	i) Deposit AuGe/Ni/Ti/Au (900/100/1000/2000 Å) on to n type GaAs; ii) Deposit Cr/Au (200/2000 Å) on to p type GaAs; iii) Alloy at 370°C for 30s in a pure H_2 atmosphere.		DC characteristics: Current gains up to 90 for HBT with emitter size 50 x 50 μm^2; Microwave characteristics: For V_{CE} = 3V & I_C = 10 mA, $(f_t)_{max}$=25GHz & f_{max}=8GHz.

TABLE 2.0.0: Summary of 'AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[35] Ito et al.	(i) Metallisations performed by conventional lift-off processes; (ii) Base and collector layers were recessed by wet chemical etching; (iii) Proton implantation was used to provide inter-device isolation;		A gain-bandwidth product f_t = 25GHz was achieved at V_{CE} = 3V and collector current density J_c =1 x 10^{-4} A/cm^2 . Limitation on f_t was mainly caused by the emitter series resistance.
[37] Dubon-Chevallier et al.	(i) Etch first mesa to the base and deposit contact metals; (ii) Etch to contact n^+ buffer layer and deposit emitter-collector contacts; (iii) Alloy at 800°C/min to 400°C;		DC performance: Maximum current gain = 15 at I_c = 20mA for a device with W_b = 40nm.
[38] Daoud-Ketata et al.	(i) Deposit emitter contact and delineate with RIE; (ii) Perform p type implantation to the base with emitter contact as a mask. Then, anneal to activate p type dopant and ohmic contact; (iii) Etch to collector; (iv) Isolate by H^+ implantation; (v) Metallise collector, then base.		An arsenic overpressure is necessary for the formation of an ohmic contact using refractory metals to contact the emitter.

TABLE 2.0.0: Summary of 'AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[39] Inada et al.	(i) Form base islands by implanting O^+ down to the collector layer using Al masks; (ii) Remove Al masks. Deposit SiO_2 by CVD, deposit Al and form dummy emitters; (iii) Define external bases by wet etching; (iv) Define collectors & contacts.		For an HBT with emitter size 1 x 20 μm^2 & a small buried collector isolated by O^+ implantation, the performance was as follows: f_t = 54GHz & f_{max} = 42GHz.
[46] Eda et al.	(i) Deposit emitter contact metals and define emitter mesa by wet etching; (ii) Deposit base contact metals and define base mesa by wet etching; (iii) Deposit collector contact metals and define collector mesa down to isolation.		This extremely simple process yielded an f_t of 18GHz and an f_{max} of 13GHz. Very high speed operation above 40GHz can be expected by optimising the process.
[42] Nakajima et al.	(i) Perform H^+ implantation into extrinsic collector; (ii) Define emitter-base and collector junction areas by RIBE; (iii) Define SiO_2 sidewall; (iv) Deposit metal contacts;		For HBTs with emitter-base junctions between 1 x 10 μm^2 and 5 x 10 μm^2 and base-collector junctions between 3 x 12 μm^2 and 7 x 12 μm^2, f_t varied between 35GHz and 50GHz and f_{max} between 42GHz and 70GHz.

TABLE 2.0.0: Summary of 'AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[41] Rezazadeh et al.	(i) Etch down to access base, collector and semi-insulating substrate; (ii) Deposit contacts to emitter and collector (Ni/AuGe/Ni/Au) and to the base (Au/Zn/Au); (iii) Anneal.		For linearly graded emitter-base, a poor current gain h_{FE} = 10-15 was observed and for parabolically graded emitter-base, a very high gain of 3000 was observed at I_c = 17mA and I_b = 14μA.
[40] Malik et al.	(i) Diffuse zinc to make contact to the base; (ii) Etch down to the collector and semi-insulating GaAs; (iii) Pattern Si_3N_4 to form dielectric crossovers on mesa edges; (iv) Metallise emitter, base and collector in one step.		For HBTs with graded bandgap bases and an undoped setback layer of 200-500A to offset Be diffusion in the emitter, maximum h_{FE}=1150 for W_b=0.18μm. Microwave S-parameter measurements yielded f_t=5GHz and f_{max}=2.5GHz.
[36] Ohshima et al.	(i) Use SiO_2 dummy emitter as implantation mask for Mg ions; (ii) Replace dummy emitter with AuGe/Au emitter & perform V-groove isolation; (iii) Isolate extrinsic base-collector by oxygen implar (iv) Etch via holes and form ~~collector contacts;~~		Process involves an SiO_2 dummy emitter as an implantation mask for Mg ions and a V-groove Si_3N_4 device isolation process. Self-aligned HBTs were 1-6 times faster than the conventional HBTs.

TABLE 2.0.0: Summary of 'AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[43,44] Tully et al.	i) Implant zinc ions to form the base region; ii) Grow emitter and cap layers & implant zinc to form base contact regions; iii) Deposit base contacts; iv) Deposit emitter and collector contacts;		Large test devices (125 x 125 μm^2 emitter, 100 x 100 μm^2 emitter contact, 200 x 300 μm^2 base-collector junction) fabricated using the aluminium lift-off (ALL) process, with refractory metal contacts, had dc gains of β = 600.
[52,53] Tiwari et al.	i) Define emitter contact and etch GaAs contact layer to undercut contact; ii) Perform ion implantation to form extrinsic base; iii) Use silicon nitride as dielectric.		Transistors with current gains of 300-500 have been achieved at small emitter dimensions of 1.6 x 4.0 μm^2 and at current densities exceeding 10^5 A/cm^2.
[56] Sunderland et al.	i) Perform contact implants through patterned SiO_2 layer; ii) Form emitter and collector contacts simultaneously; iii) Form base contacts.		Incremental current gains of 100 have been observed for transistors with 4 x 22 μm^2 emitters. No emitter size effect was observed.

TABLE 2.0.0: Summary of AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[57] Morizuka et al.	(i) Implant B^+ or H^+ to form isolation regions; (ii) Etch down to the base and metallise; (iii) Use polyimide as dielectric (iv) Metallise emitter; (v) Etch to the collector and metallise.		A 1um emitter-width SAHBT with f_{max} of 86GHZ was successfully fabricated.
[45] Kim et al.	(i) Delineate the emitter and base mesas and form contacts to emitter, base and collector. (ii) Passivate with silicon nitride.		Maximum values of current gain β ranged from 1000 to 2000 for HBTs with emitter dimensions varying between 2 x 9 μm^2 and 2 x 40 μm^2. f_t up to 24GHz were obtained.
[59] Nagata et al.	(i) Etch emitter mesa using RIBE; (ii) Form SiO_2 sidewall; (iii) Form contact pads; (iv) Perform inter-device isolation.		For an HBT with an emitter-base junction area of 3 x 9 μm^2 and a base-collector junction area of 9 x 12 μm^2, a current gain in the range 15-20 was obtained at a collector current density, J_c, of 1×10^4 A/cm^2.

TABLE 2.0.0: Summary of 'AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[58] Hayama et al.	(i) Selective implant of protons to define device active area; (ii) Define emitter contact and mesa; (iii) Define 1st sidewall and metallise base; (iv) Define 2nd sidewall and metallise collector.		Structure optimisation, uniformity consideration and high-speed circuit performance for AlGaAs/GaAs HBT are described.
[47,48] Asbeck et al.	(i) Implant Be to form extrinsic base regions and implant oxygen for extrinsic collector; (ii) Etch via holes to make contact to the buried collector layer.		For HBTs with multiple emitter fingers of nominally 1.2 um width, maximum current of 30 and an f_t of 40GHz were obtained.
[49] Asbeck et al.	(i) Dual level PR/PMMA patterning; (ii) Etch cap and emitter and implant to the base; (iii) Define SiO_2 sidewalls and metallise.		Incremental current gain for SAHBTs was found to vary depending on emitter size. Gain as high as 200 with emitter dimensions 8 x 20 um^2 but as low as 20 with emitter dimensions 1.5 x 4 um^2.

TABLE 2.0.0: Summary of 'AlGaAs/GaAs HBT structures' study

REFERENCES	MAIN FABRICATION STEPS	DEVICE STRUCTURES	COMMENTS
[50] Asbeck et al.	(i) Isolation implant; (ii) Uncover extrinsic base, implant protons, deposit base metal, deposit SiO_2 and lift off metal & SiO (iii) Form emitter contact; (iv) Uncover subcollector and deposit collector metal. (i) Deposit base and collector metals through via holes.		For an HBT with 3 emitter fingers of 1.2 x 9 μm^2 and a base-collector junction area of 100 μm^2, f_t was 55GHz and f_{max} was 105GHz.
[51] Asbeck et al.			A maximum f_t of 70GHz was obtained at V_{CE} = 1V but f_t dropped with increasing V_{CE} due to the increased transit times of electrons across the base-collector depletion region.

2.2.0: Ohmic contacts and metallisation schemes to Gallium Arsenide.

The quality of an ohmic contact to GaAs devices is one of the most significant factors affecting the performance of such a device [60]. Therefore, much effort has been spent on contact system development and many investigations have concentrated on finding metallisation schemes to both n and p type GaAs [64-87]. Rideout [61] has provided an excellent theoretical treatment of ohmic contacts to GaAs but admits (as do others) that "ohmic contact technology has developed thus far more as a technical art than as a science". The reproducibility of such contacts strongly affects the device cost while the integrity of such a contact is a major factor affecting device reliability [62,63]. Because of the large amount of literature which has been published on investigations of contact resistance, this review will be limited to those studies relevant to this project. A figure of merit defining good contact resistance is $< 9.9 \times 10^{-6}$ ohm-cm^2 .

2.2.1: Ohmic contact study to n type GaAs.

Prakash [64] used a simple technique for obtaining reproducible ohmic contacts to GaAs wafers with a resistivity of 1×10^{-3} ohm-cm by evaporating an alloy of AuGe (92:8 w/w %) onto the hot substrate (550°C) under specified conditions. The specific resistance of contacts thus made was about 2.3×10^{-5} ohm-cm^2 . The experimental results were explained by means of a quantum mechanical tunneling model and metallurgical considerations.

The strong influence of semiconductor surface preparation on contact resistance was investigated by Heime et al. [65]. They proved the superiority of sputter cleaning over wet chemical etching. The multilayer Ni/AuGe(88:12 w/w %)/Ni satisfied the following requirements: adhesion, wetting, temperature stability and smoothness. Optimisation of the alloying cycle led to the following contact resistances: 4×10^{-4} ohm-cm^{2} for a doping density of 2×10^{15} cm^{-3} to 1×10^{-6} ohm-cm^{2} for a doping density of 1×10^{18} cm^{-3} .

An analysis of the effects of the heating rate on ohmic properties in AuGe alloying was conducted by Yokohama et al. [66]. For a AuGe(88:12 w/w %) eutectic alloy film of 350Å thick and a subsequent Au film 3000Å thick on a GaAs epitaxial layer of 0.3-0.4µm thick with a doping density of 3×10^{16} cm^{-3} , a lowest value of 1×10^{6} ohm-cm^{2} was obtained after alloying at 450° C for 2.5 minutes. A Ni film of 50-100Å thick was used to improve the wettability of the AuGe eutectic alloy.

Yoder [67] correlated the electrical effects observed in several significant studies of the Ni/AuGe/Au contact structure and proposed that, instead of thinking in terms of Ni being a wetting agent, a more probable model is that the diffusion of Ni into GaAs provides a driving force for an `enhanced´ diffusion of the germanium into the GaAs. He stated that careful attention must be given to the GaAs surface to ensure homogeneity of the contact and he also established that refractory barrier metallisations are mandatory if the contact is to be fabricated by sintering.

The role of Ge in evaporated AuGe ohmic contacts was investigated in greater depth by Iliadis and Singer [68] who suggested that below the temperature when melting of the metals occurs, the Ge is concentrated in localised regions of the contact interface with the GaAs. Consequently, optimisation of the specific contact resistance requires the maximising of the recrystallised areas and hence, the pursuit of a deposition technology which maximises the area coverage of interfacial AuGe of the eutectic composition. Later, pursuing their study of the metallurgical behaviour of Ni/AuGe contacts, Iliadis and Singer [69] used Ni/Au/AuGe and Ni/AuGe contacts to show that the Ge incorporation is by a process of solid state diffusion rather than by the eutectic melting-recrystallisation mechanism found in AuGe contacts. In spite of the improvement in the homogeneity of the contact brought about by using Ni, the thermal stability of these contacts was found to be worse than the simple AuGe ones.

Transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) analyses of the interface structures of a Au/Ni/AuGe contact were performed by Kuan et al. [70] in order to determine the structural features which govern contact resistance. They found that relatively high contact resistance (4-6 x 10^{-4} ohm-cm^2) after alloying is correlated with the dominance of the Au/GaAs areas at the interface. Thus, to attain an ohmic contact with better reliability, they suggested that future efforts should concentrate on non Au-based metallisation schemes or non-alloyed contacts.

By varying annealing process parameters (anneal ramp rate, dwell temperature, dwell duration, anneal atmosphere) to minimise

AuGe(88:12 w/w %) ohmic contact resistance, Kulkarni [71] studied structural variations by Auger electron spectroscopy (AES) and observed that minimum contact resistivity occurs when the amount of the Ge in-diffusion approaches the amount of Ga out-diffusion.

The relation of contact resistance to heat treatment and microstructure was examined for Ge/Ni/Au, AuGe/Ni/Au and AuGe/Ni by Bruce and Piercy [72]. They found that the Ge/Ni/Au metallisation had the lowest contact resistance and the highest proportion of the Ni-Ge-As phase at the contact/GaAs interface. It was also the most stable with subsequent ageing at 330°C, this stability being attributed to the Ni-Ge-As phase acting as a diffusion barrier at the GaAs/contact interface.

In a study of AuGe based alloyed ohmic contacts to the two dimensional electron gas at the N^+/N III-V semiconductor hetero-interfaces, O´Connor et al. [73] showed that metallisations with auxiliary Ni layers had an order of magnitude lower resistance than those containing silver (Ag).

Tiwari et al. [74] demonstrated a sintered ohmic contact scheme which gave a comparable contact resistance (1×10^{-6} ohm-cm^2) to the commonly used AuGe system on 1×10^{17} cm^{-3} doped n type GaAs. The ohmic contact formation occurred by simultaneous synthesis of molybdenum germanide as a contacting metallurgy and a shallow n^+ type region formed in GaAs by germanium diffusion. The system also exhibited better temperature stability and smoother morphology, thus allowing tighter dimension controls.

Ohmic contacts for high temperature device applications up to 300°C have been developed by Anderson et al. [75]. The purpose

of that work was to fabricate refractory ohmic contacts with low specific contact resistance. Refractory metallisations used with epitaxial Ge layers were as follows, Ge/TiW, Ge/Ta, Ge/Mo and Ge/Ni. Optimum laser anneal conditions yielded specific contact resistances in the range 1-5 x 10^{-6} ohm-cm^2 on 2 x 10^{17} cm^{-3} GaAs, which is an order of magnitude improvement over thermally annealed Ni/Ge contacts.

Chen et al. [76] fabricated Pd/Ge/Au and Ge/Pd/Au sintered ohmic contacts. Specific resistances similar to those of conventional Ni/Ge/Au alloyed ohmic contacts were obtained but the sintered contacts had much smoother surfaces and their edges were very well defined. The authors established that the properties of these low resistance contacts were insensitive to the sintering temperature and to the thickness of the Pd and Ge layers or their order of deposition.

Agius et al. [77] have shown the feasibility of molybdenum germanide ohmic contact using an annealing procedure involving arsenic (As) overpressure at 800°C. To protect the active Ge/Mo film against subsequent chemical degradation, a tungsten (W) layer can be deposited as an overlayer. A specific contact resistivity of 1 x 10^{-6} ohm-cm^2 was obtained.

Low resistance Ni/In/W contact metallisation was developed by Murakami and Price [78]. The contact resistances were stable during subsequent annealings at 400°C for 100 hours and 500°C for 10 hours. Thermal stability and surface morphology of this contact were superior to those of conventionally used Au/Ni/Ge contacts.

Metallurgical and electrical properties of alloyed Ni/AuGe films on n type GaAs were studied by Robinson et al. [79]. His results indicated an exponentially decreasing Au concentration which only penetrates into the GaAs epitaxial layer to a depth less than the thickness of the as-deposited AuGe layer.

2.2.2: Ohmic contact study to p type GaAs

Experimental studies of an ohmic contact scheme prepared by a dc sputtering technique using Au/Zn (to improve Zn adhesion) on epitaxial GaAs over a wide carrier concentration (5×10^{17} cm^{-3} $< p < 2 \times 10^{19}$ cm^{-3}) were carried out by Livingstone, Duncan and Hutchins [80]. Sputtering was preferred as a deposition technique over thermal evaporation due to its simplicity and improved Zn adhesion. The authors demonstrated that the Au/Zn contacts yielded a reproducible ohmic contact after a 500°C alloy stage for $p < 1 \times 10^{19}$ cm^{-3}.

Sanada and Wada [81] concentrated on a Au/Zn/Au multilayer structure deposited by sequential evaporation on to the GaAs. For an optimum alloying temperature of 400°C and a maximum carrier concentration of 5×10^{18} cm^{-3}, a minimum specific contact resistance of 9×10^{-6} ohm-cm^2 was obtained. Auger analysis gave a straightforward indication that the low contact resistance is produced by the preferential incorporation of Zn atoms within the GaAs bulk during the alloying process.

Another method of making ohmic contacts to p type GaAs was developed by Chang and Yeh [82]. They used solid phase interdiffusion of multiple layers of Au/Zn/Au deposited by e-beam evaporation. Relatively low contact resistance (1×10^{-5} ohm-cm^2)

was reproducibly obtained for p type material with a hole concentration of 2×10^{18} cm^{-3} .

Contact resistance of non-alloyed metal contacts to shallow Zn implanted (≃1000A) p^+ GaAs was investigated by Su and Stolte [83], who showed that unalloyed contact structures such as Cr/Au and Ti/Pt/Au can yield good contact resistance (≃ 1×10^{-6} ohm-cm^2).

Brooks et al. [84] obtained specific contact resistances as low as 7×10^{-7} ohm-cm^2 for structures prepared by heat treating Zn/Pd/Au metallisation deposited on epitaxial GaAs layers with an acceptor concentration of 1.5×10^{19} cm^{-3} . They found that the unusually low contact resistance was due to the incorporation of Pd into the metallisation, and that the specific resistance was unaffected by the Au thickness. The contacts were reproducible, simple to fabricate, exhibited excellent adhesion and had a uniformly smooth surface morphology.

Papanicolaou and Christou [85] obtained a low resistivity ohmic contact ($\rho_c \leqslant 9 \times 10^{-7}$ ohm-cm^2) using a AuMg(96:4 w/w %) contact metal, a Mo diffusion barrier and Au overlay. These contacts exhibited excellent uniformity and adhesion to the GaAs. The electrical properties of this contact were shown to depend on the Mg composition with an optimum value at 4% Mg.

A very low resistivity alloyed AuMn(96:4 w/w %) ohmic contact was demonstrated by Dubon-Chevallier et al. [86]. A specific contact resistivity of 2×10^{-7} ohm-cm^2 was obtained on 2×10^{19} cm^{-3} epitaxial layers after optimum alloying with a cycle consisting of raising the temperature at 800°C/min to 400°C. Also, 2×10^{-6} ohm-cm^2 was obtained on 2×10^{20} cm^{-3}

doped layers without alloying. The contacts were stable and reproducible.

Metallisation schemes stable up to 550°C heat treatments were studied by Tandon et al. [87] and relatively good results were obtained with Pt/TiN/Ag, Mg/Pt/TiN/Ag, Pt/W/Ag, Mg/W/Ag, Pt/WN/Ag on Zn doped GaAs with $p = 1 \times 10^{18}$ cm^{-3}. Specific contact resistivities were in the range 1-3 x 10^{-4} $ohm\text{-}cm^2$.

2.2.3: Other contact resistance studies

Contact alloys were developed for use on a wide variety of GaAs devices such as high temperature transistors and Gunn oscillators by Cox and Strack [88]. The alloys were composed of Ag(90%wt.)In(5%wt.)Ge(5%wt.) for n type GaAs and of Ag(80%wt.)In(10%wt.)Zn(10%wt.) for p type GaAs. Specific contact resistance values obtained were well below 1 x 10^{-4} $ohm\text{-}cm^2$ on 0.1 ohm-cm or lower resistivity n or p type GaAs. Fabrication steps which require temperatures of up to 770 °C for already contacted devices could be performed.

In their studies on the metallurgical and electrical stability of Platinum (Pt) and Palladium (Pd) silicide contacts to GaAs, Marshall et al. [89] observed that the use of both silicides as contact metallisations gave a metallurgically more stable contact than Pt or Pd on GaAs. In investigating the feasibility of using solid phase epitaxy (SPE) to grow a highly doped Ge epitaxial layer on GaAs to form a non-alloyed ohmic contact, they obtained relatively low contact resistivities ($\simeq 2 \times 10^{-6}$ $ohm\text{-}cm^2$) using a Ge/Sb/Pd system.

Thin surface layers of GaAs were heavily doped (Se for n type and Zn for p type) by laser-assisted diffusion by Krauttle and Waschenswanz [90]. Ni/AuGe (n type) and Ni/AuZn (p type) were evaporated. Subsequent heat treatment at 450°C for 5 minutes gave a specific contact resistance of 3×10^{-6} ohm-cm^2 for both systems. The technique still needed to be optimised.

Chino et al. [91] conducted investigations to study how reliability of ohmic contacts in GaAs devices was affected by a metal which was in contact with the ohmic contacts, such as a heat sink metal or a bonding pad metal. They observed a degradation mechanism which was due to GaAs reaction with the metal which is contact with the ohmic contacts.

Studies on the theory of ohmic contacts to GaAs were performed by Braslau [92], Edwards et al. [93], Chern et al. [94], Reeves et al. [95], Harrison [96], Cohen [97] and Proctor et al. [98].

Table 2.1.0 summarises the work that has been described above and the literature shows that there is a very marked trend towards the use of metallisation schemes which can withstand high temperature processing steps and also be used for contacting devices which will be used in high temperature environments.

TABLE 2.10 :Summary of 'ohmic contact structures' study

REFERENCES	CONTACT STRUCTURE Metals / Thicknesses(Å)	METHOD OF DEPOSITION	HEAT TREATMENT	SPECIFIC CONTACT RESISTANCE(Ω-cm²)	COMMENTS
[64] Prakash	AuGe alloy with varying % of alloy and metal thickness	Thermal evaporation	Keep substrate temperature at 500°C during evaporation;	2.32×10^{-5}	AuGe alloy evaporated at 1×10^{-6} T on to 1.0×10^{-3} ohm-cm n type GaAs.
[65] Heime et al.	Ni/AuGe/Ni (50/700/300 Å)	Thermal evaporation	Forming gas (90%N_2+10%H_2); Increase temp. to 460°C in 1 min & immediate cooling(220°C/min);	1.0×10^{-6}	Alloy of AuGe(88:12 w/w%); Results obtained on GaAs with $n = 1 \times 10^{18}/cm^3$.
[66] Yokohama et al.	AuGe/Au (350/3000 Å)	Thermal evaporation	450°C for 2.5 mins in N_2; Wafer is put directly on heated Carbon block at 450°C;	1.0×10^{-6}	Alloy of AuGe(88:12 w/w%); Results obtained on epi GaAs 0.3 - 0.4 μm thick with $n = 3 \times 10^{16}/cm^3$.
[68] Iliadis & Singer	AuGe/Au (500/1000 Å)	Thermal evaporation	450°c for 2.5 mins in forming gas in a quartz furnace tube;	2.1×10^{-5}	Alloy of AuGe(88:12 w/w%); Results obtaind on epi GaAs 4 μm thick with $n = 3 \times 10^{16}/cm^3$.

TABLE 2.1.0 :Summary of 'ohmic contact structures' study

REFERENCES	CONTACT STRUCTURE Metals / Thicknesses (Å)	METHOD OF DEPOSITION	HEAT TREATMENT	SPECIFIC CONTACT RESISTANCE (Ω-cm^2)	COMMENTS
[69] Iliadis & Singer	i) AuGe/Au/Ni (350/1000/200 Å) ii) AuGe/Ni (350/200 Å) iii) AuGe/Au (350/1000 Å)	Thermal evaporation	Sintered at 450°C for 2.5 mins;	3.0×10^{-6}	Results obtained on n type GaAs with $n = 5 \times 10^{16}/cm^3$.
[71] Kulkarni et al.	i) AuGe (3000 Å) ii) AuGe (1500 Å) iii) AuGe (2500 Å)	Thermal evaporation	400°C for 5 mins;	2.34×10^{-5}	Results obtained on n type GaAs with $n = 3 \times 10^{17}/cm^3$.
[75] Anderson et al.	i) Ge(epi)/TiW (200/650 Å) ii) Ge(epi)/Ni (1000/1000 Å) iii) Ge/Ta & Ge/Mo (Thicknesses not stated).	e-beam evaporation for Ta, Mo and Ni and sputtering for TiW;	700°C in forming gas for 25 mins;	1.0×10^{-6}	Best results obtained with Ge/TiW on GaAs with $n = 2 \times 10^{18}/cm^3$
[76] Chen et al.	i) Pd/Ge/Au (300/400/2000 Å) ii) Ni/Ge/Au (300/400/3400 Å)	e-beam evaporation	450°C for 30 s ;	1.4×10^{-6} (Pd/Ge/Au) & 1.8×10^{-6} (Ni/Ge/Au)	Results for GaAs with $n = 1 \times 10\ /cm^3$ for Pd/Ge/Au and $n = 2.2 \times 10^{18}/cm^3$ for Ni/Ge/Au .

TABLE 2.10 :Summary of 'ohmic contact structures' study

REFERENCES	CONTACT STRUCTURE Metals / Thicknesses (Å)	METHOD OF DEPOSITION	HEAT TREATMENT	SPECIFIC CONTACT RESISTANCE (Ω-cm^2)	COMMENTS
[77] Agius et al.	Ge/Mo/W (150/150/3000 Å)	Ge: e-beam evaporation or DC sputtering; Mo: sputtering; W: sputtering;	Annealed under an As overpressure at 800°C for 15 mins;	1.0×10^{-6}	Metal films exhibited good adhesion to GaAs.
[80] Livingstone et al.	Zn/Au (100/1000 Å)	DC sputtering	Alloy at 500°C for 5 mins in dry N_2 ;	1.5×10^{-4}	Best results obtained on p type GaAs with $p = 2.03 \times 10^{19}/cm^3$.
[81] Sanada and Wada	Au/Zn/Au (300/370/2330 Å)	Thermal evaporation	Alloy in flowing N_2 gas at 400°C for 5 mins;	9×10^{-6}	Best results obtained on p type GaAs with $p = 5 \times 10^{18}/cm^3$.
[82] Chang and Yeh	Au/Zn/Au (500/150/3000 Å)	e-beam evaporation	Sintering at 450°C for 4 mins in N_2.	$\rho_c \leq 10^{-5}$	Reproducible results on p type GaAs with $p = 2 \times 10^{18}/cm^3$.

TABLE 2.10 : Summary of 'ohmic contact structures' study

REFERENCES	CONTACT STRUCTURE Metals / Thicknesses (Å)	METHOD OF DEPOSITION	HEAT TREATMENT	SPECIFIC CONTACT RESISTANCE (Ω-cm^2)	COMMENTS
[83] Su and Stolte	i) Cr/Au (500/3000 Å) ii) Ti/Pt/Au (500/1000/3000 Å)	e-beam evaporation	Anneal zinc-implanted GaAs at 700°C for 3 mins in an ambient of H_2-AsH_3 mixture;	9×10^{-7}	Contacts to shallow (≃1000Å) Zn-implanted GaAs were not alloyed; Best results obtained for Ti/Pt/Au;
[84] Brooks et al.	Zn/Pd/Au (300/500/3000 Å)	e-beam evaporation	Alloy at 470°C ;	7×10^{-7}	Best results obtained obtained on p type GaAs with doping concentration $p = 1.5 \times 10^{19}/cm^3$.

CHAPTER 3: EXPERIMENTAL DETAILS AND RESULTS

3.1.0: Fabrication of conventional HBTs

3.1.1: Surface preparation prior to processing

Cleanliness is crucial in achieving high yields and reproducible results in the production of any semiconductor device. Cleanliness is preserved by good environmental and slice handling techniques.

In addition to ambient cleanliness, a wafer must be cleaned before it undergoes any sort of processing. Cleaning refers to removal of undesired material from the wafer before subsequent process steps. These residues are often remnants from previous steps.

(a) Solvent cleaning;

Organic solvents are effective in removing oils, greases, waxes and organic materials such as positive photoresists. These solvents are especially useful as they do not react chemically with GaAs, metals and some dielectrics. Solvent cleaning must be carried out prior to any photolithography in order to provide a clean semiconductor surface so that the photoresist has a uniform thickness after spinning.

(b) Oxygen descum;

Oxygen descum is an additional cleaning step that is carried out usually after the solvent cleaning. It helps to remove materials that the solvents have failed to remove and is particularly useful for cleaning a sample that has been patterned with photoresist, since it is not permissible to use solvents after patterning as the pattern would be damaged by the solvents.

(c) Ammonia dip;

Wafers are immersed for 10s in a solution of ammonia/DI water (10:100 by vol.) prior to being loaded in the evaporator for metallisation. The ammonia solution etches the oxide (50-100Å) formed on the surface of the GaAs wafer, thus providing an oxide free surface to the subsequent metallisation. It is however important to dry the surface with nitrogen gas before loading in order to remove any moisture from the semiconductor surface and hence obtain maximum adhesion of the metals to the surface.

3.1.2: Fabrication of devices

The fabrication process for conventional HBTs was based on the process described by Asbeck et al. [47,48]. Eight photolithographic steps are generally used for fabricating circuits involving complete conventional structures but it must be noted that in this work, the fabrication of complete circuits is not considered and efforts are concentrated upon fabrication of devices alone. The six photolith levels involved in the fabrication of conventional devices are as follows:-

(i) Emitter metal:

The emitter contact pattern was defined by photolithography and metallisation was performed by sequentially evaporating Ni(50Å)/AuGe(600Å)/Ni(200Å)/Au(2000Å) and lifting off the metal in the unwanted regions.

(ii) Base contact region implant:

The base contact windows were defined by photolithography and oxygen was deep-implanted into the collector extrinsic region to reduce the extrinsic base-collector capacitance. With

(011)
(111) Ga
(001)
(010)
(100)
(101)
(110)
$(0\bar{1}1)$
$(1\bar{1}1)$ As
$(01\bar{1})$
$(11\bar{1})$ As
$(1\bar{1}0)$
$(10\bar{1})$
$(00\bar{1})$
$(0\bar{1}0)$
$(1\bar{1}\bar{1})$ Ga
$(0\bar{1}\bar{1})$

CROSS SECTION OF GROOVES
ETCHED INTO FRONT FACE OF WAFER

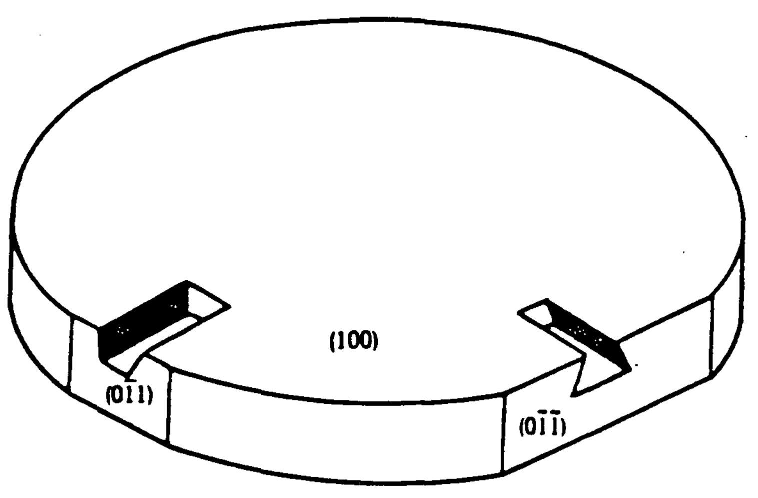
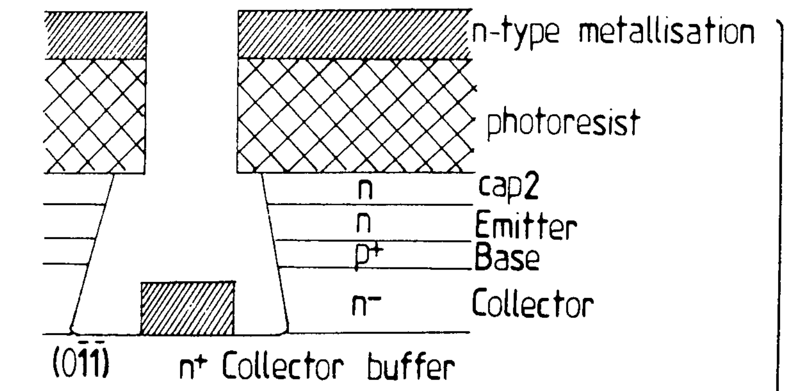
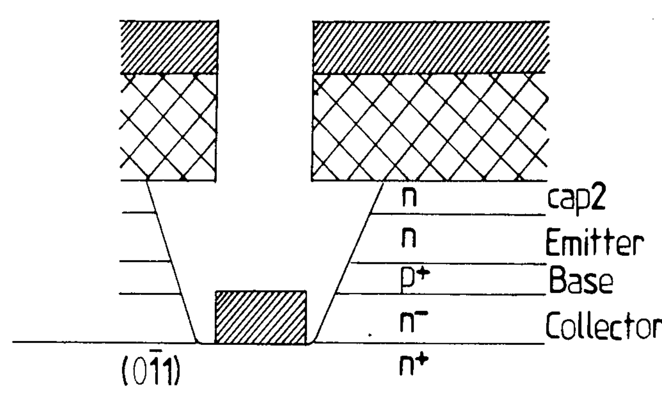


FIGURE 3.0.0 :Lattice planes and surface orientation in GaAs 2 inch wafers.

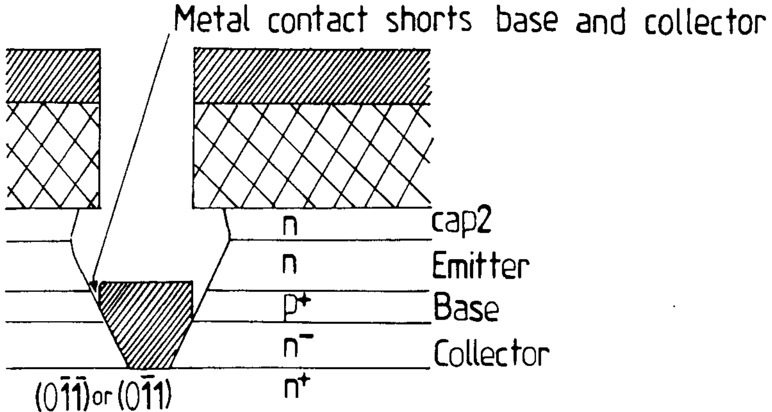


(a) Correct etched profile.

See figure 3.0.0



(b) Correct etched profile.



(c) Incorrect etched profile.

FIGURE 3.1.0 : Etchant must provide correct profile to prevent metals from making contact to layers of different conductivities at the same time.

the same photoresist pattern, Be was implanted to form the p^+ extrinsic base contact regions which make contact to the base layer. The photoresist was then removed and the base contact windows were re-defined by photolithography in order to ensure the required profile for lift-off since the implantation process would have destroyed the photoresist profile defined by the first photolithography for the base windows. Metallisation to the base is then performed by thermal evaporation of Au(200Å)/Zn(600Å)/Au(2000Å) followed by lift-off. An alternative procedure used previously consisted of etching down to the base layer after defining the base windows by photolithography, and depositing the metals stated above directly on to the base layer. The etchant used was a mixture of NH_3/H_2O_2/DI (8:3:400 by vol.).

(iii) Collector etch and metallisation:

The required pattern was defined by photolithography and via holes were etched into the wafer to make contact to the buried collector layer. The etchant used was a mixture of NH_3/H_2O_2/DI (4:16:800 by vol.). The same photoresist pattern then served as a mask for the metallisation of the collector, which was achieved by sequential electron-beam (e-beam) evaporation of Ni(50Å)/AuGe(600Å)/Ni(200Å)/Au(1500Å) and lift-off.

(iv) Isolation:

Electrical isolation was achieved principally by proton (H^+) bombardment of the wafer surface outside the active transistor areas.

(v) Polyimide/Silicon nitride windows:

The two dielectrics currently used in the fabrication process were polyimide and silicon nitride (Si_3N_4) which have

dielectric constants of 3.5 and 7.2 respectively. Despite the advantage that silicon nitride has in that it can be applied in thinner layers (and is thus useful in the fabrication of capacitors with large values), polyimide was selected for our purpose because of the ease and cheapness of fabrication of such films. The polyimide film was applied to the wafer by spinning in the same way as photoresist layers, followed by curing at 300°C. Photolithography, followed by reactive ion etching (RIE) were used to define windows in the polyimide layer and in addition to good step coverage of underlying layers, the polyimide film provided a quasi-planar surface suitable for further processing steps. The photoresist was then removed.

(vi) Bonding Pads:

The bonding pads were fabricated by photolithography followed by thermal evaporation of Ti(50Å)/Au(3000Å) and lift-off.

It must be noted that the choice of etchant for the collector etch (or base etch in the case of the alternative procedure being used for the base metallisation) must be made with the aim to provide windows with the required profiles to avoid shorting the contact metals to the semiconductor (figures 3.0.0 and 3.1.0 (a), (b) and (c)).

The HBTs were fabricated on MBE wafers MB 1233 and MB 1236 which had the layer structures described in Table 3.0.0. Half of each wafer was used for the conventional process and the other halves were used for processing self-aligned HBTs (SAHBTs) so that the performance of the transistors from each process can be compared.

The structure of a conventional HBT is shown in figure 3.1.1. A list of all the electrical measurement techniques used for this project is given in appendix A/1.. A typical example of the dc output characteristics for an 8um (emitter design width) device is shown in figure 3.1.4 (a) and (b). Note the difference in threshold voltage for the two characteristics, which clearly shows the importance of good contact metallisation for good threshold voltage. The frequency response of an 8µm HBT (measured on the Network Analyser on wafer probing) is given in figure 3.1.5. The values of f_t= 8.0GHZ and f_{max} = 7.9GHz were the highest values of transition frequency and maximum oscillation frequency obtained for an 8 um device fabricated by the conventional process. Lowest values for f_t and f_{max} were 7.7GHz and 7.1 GHz respectively.

3.1.3: <u>Contact resistance results for the conventional process</u>

Prior to the fabrication of the conventional devices, transmission line models (TLMs) for assessment of contact resistance were fabricated by depositing various metallisation systems on n type GaAs substrates with a doping profile similar to that of the emitter epitaxial layer. The metallisation systems studied were Ni/AuGe/Ni/Au with varying thicknesses of each metal layer. Rapid thermal annealing (RTA) and furnace annealing (FA) were used to electrically activate the contacts and contact resistance measurements were performed for different annealing times. The results are shown in Table 3.1.0. Best value of specific contact resistance (1.0×10^{-6} ohm-cm^2) was obtained for a RTA time of 40s at 450°C and a metallisation structure of

TYPICAL EPITAXIAL STRUCTURE OF HBTs				
Layer	Thickness (um)	Type	Doping (cm^{-3})	Al/As fraction
Cap1	0.075	n^+	2×10^{18}	0
Cap2	0.125	n	5×10^{17}	0
Grading	0.03	n	5×10^{17}	.30-0
Emitter	0.22	n	5×10^{17}	.30
Grading	0.03	n	5×10^{17}	0-.30
Base	0.1	p^+	3×10^{18}	0
Collector	0.7	n^-	3×10^{16}	0
Subcollector	0.6	n^+	1×10^{18}	0
Substrate		S.I	Undoped	

TABLE 3.0.0

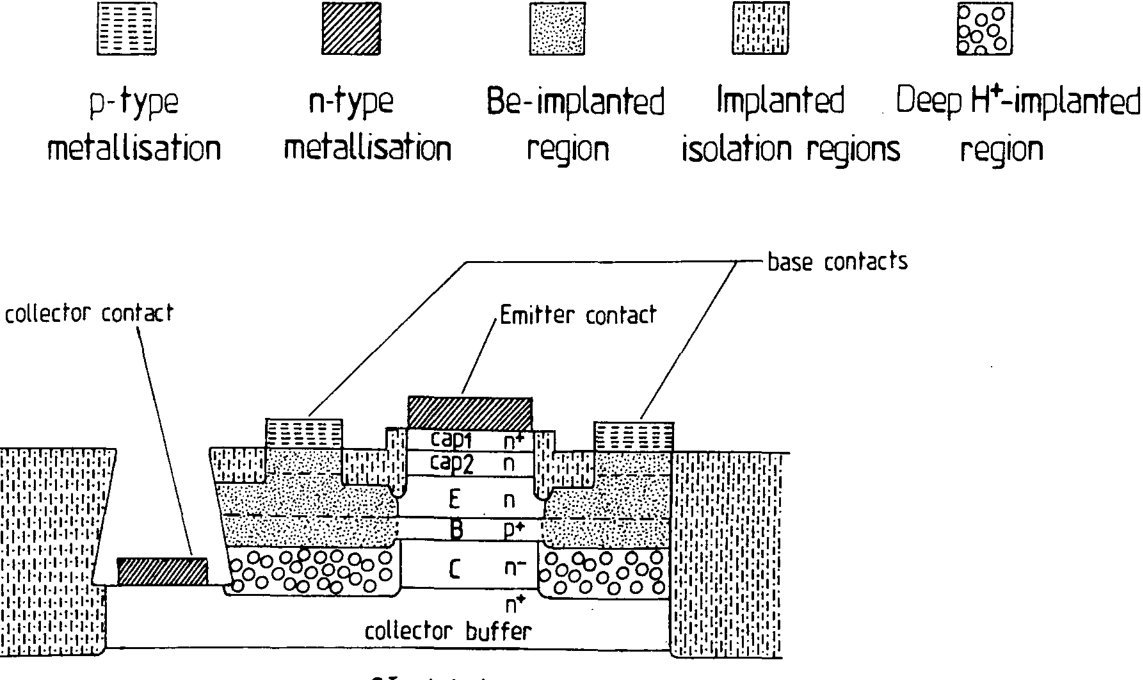


FIGURE 3.1.1 : Schematic drawing of the HBT structure fabricated by the conventional process.

Ni(50Å)/AuGe(600Å)/Ni(200Å)/Au(2000Å). The same metallisation structure on wafers with doping profiles similar to the collector buffer gave a specific contact resistance of 1.35 x 10^{-6} ohm-cm^2 for the same alloying conditions as above. These conditions were selected and applied to the fabrication of emitter and collector contacts of the conventional HBTs. TLMs for assessment of resistance of contacts fabricated as part of the conventional process were used to evaluate the specific contact resistance of the emitter and collector contact pads and the values obtained for specific contact resistance ρ_c were in close agreement (1.1 x 10^{-6} ohm-cm^2 for the emitter contacts and 1.4 x 10^{-6} ohm-cm^2 for the collector contacts) with those obtained previously. Figures 3.1.2 (a) and (b) give a clear indication of the morphology of the above mentioned contacts after the alloying process. Auger electron spectroscopy profiles of the contacts before and after alloying are shown in figures 3.1.2 (c) and (d).

Metallisation systems to p type GaAs were assessed prior to HBT fabrication using TLMs fabricated on p type GaAs substrates with doping profile similar to that of the beryllium implanted base contact regions. The metallisation systems studied were Ti/Zn/Au, Cr/Zn/Au and Au/Zn/Au. Results are shown in Table 3.1.0 and as above, the optimum conditions (alloy at 450°C for 40s by RTA) for a metallisation system consisting of sequentially evaporated Au(200Å)/Zn(600Å)/Au(2000Å) were selected and applied to the fabrication of base contacts in conventional HBTs. Figures 3.1.3 (a) and (b) give an overall view of the TLMs used to assess the contact resistance of the Au/Zn/Au metallisation system described above and Auger electron spectroscopy profiles

of the contacts before and after alloying are shown in figures 3.1.5 (c) and (d). Measurements of resistance of contacts fabricated as part of the conventional process gave similar values of ρ_c (1.4×10^{6} ohm-cm^2) to those obtained previously.

[CONVENTIONAL PROCESS]

TABLE 3.10 : Contact resistance results to n-type GaAs

CONTACT STRUCTURE Metals/ Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/ Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE (Ωcm^2) Best values
Au : 2000 Ni : 400 AuGe : 600 Ni : 50 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$1.0 - 1.2 \times 10^{-4}$ (40s) $1.25 - 1.4 \times 10^{-4}$ (40s)
Au : 2000 Ni : 300 AuGe : 600 Ni : 50 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$9.8 - 9.9 \times 10^{-5}$ (50s) $4.4 - 4.7 \times 10^{-5}$ (40s)
Au : 2000 Ni : 200 AuGe : 600 Ni : 50 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$1.0 - 1.1 \times 10^{-6}$ (40s) $1.35 - 1.5 \times 10^{-6}$ (40s)
Au : 2000 Ni : 100 AuGe : 600 Ni : 50 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$5.3 - 5.7 \times 10^{-4}$ (40s) non-ohmic

TABLE 3.10 : Contact resistance results to n-type GaAs

CONTACT STRUCTURE Metals/ Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/ Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\,cm^2$) Best values
Au : 2000 Ni : 400 AuGe : 600 Ni : 50 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace).	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$3.4 - 4.2 \times 10^{-5}$ (40s) $3.8 - 4.3 \times 10^{-5}$ (40s)
Au : 2000 Ni : 300 AuGe : 600 Ni : 50 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$4.75 - 5.5 \times 10^{-5}$ (50s) $2.7 - 4.7 \times 10^{-5}$ (40s)
Au : 2000 Ni : 200 AuGe : 600 Ni : 50 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$6.0 - 7.2 \times 10^{-6}$ (40s) $6.6 - 7.1 \times 10^{-6}$ (40s)
Au : 2000 Ni : 100 AuGe : 600 Ni : 50 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$6.5 - 8.8 \times 10^{-5}$ (40s) $8.0 - 9.2 \times 10^{-5}$ (40s)

TABLE 3.10 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\, cm^2$)
Au : 2000 Zn : 800 Ti : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	Best values $5.7 - 6.3 \times 10^{-4}$ (50s)
Au : 2000 Zn : 700 Ti : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$6.0 - 6.3 \times 10^{-4}$ (60s)
Au : 2000 Zn : 600 Ti : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$6.4 - 6.6 \times 10^{-5}$ (60s)
Au : 2000 Zn : 500 Ti : 200 GaAs substrate	RTA 450° for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$6.3 - 7.1 \times 10^{-5}$ (60s)

TABLE 3.10 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals/Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Ti : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	Best values $2.8 - 3.7 \times 10^{-4}$ (50s)
Au : 2000 Zn : 700 Ti : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$2.75 - 4.5 \times 10^{-4}$ (60s)
Au : 2000 Zn : 600 Ti : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$3.4 - 5.1 \times 10^{-5}$ (60s)
Au : 2000 Zn : 500 Ti : 200 GaAs substrate	RTA 550° for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$3.4 - 5.3 \times 10^{-5}$ (60s)

TABLE 3.10 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Cr : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	Best values $5.45 - 6.1 \times 10^{-4}$ (60s)
Au : 2000 Zn : 700 Cr : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$5.5 - 5.7 \times 10^{-4}$ (60s)
Au : 2000 Zn : 600 Cr : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$5.8 - 6.4 \times 10^{-5}$ (60s)
Au : 2000 Zn : 500 Cr : 200 GaAs substrate	RTA 450° for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$6.1 - 6.7 \times 10^{-5}$ (60s)

TABLE 3.10 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals/Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\, cm^2$)
Au : 2000 Zn : 800 Cr : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	Best values $1.75 - 1.9 \times 10^{-4}$ (60s)
Au : 2000 Zn : 700 Cr : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$2.2 - 2.7 \times 10^{-4}$ (60s)
Au : 2000 Zn : 600 Cr : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$2.3 - 3.4 \times 10^{-5}$ (60s)
Au : 2000 Zn : 500 Cr : 200 GaAs substrate	RTA 550° for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$2.1 - 4.3 \times 10^{-5}$ (60s)

TABLE 3.10 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Au : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	Best values $2.25 - 3.1 \times 10^{-6}$ (40s)
Au : 2000 Zn : 700 Au : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$2.2 - 2.5 \times 10^{-6}$ (40s)
Au : 2000 Zn : 600 Au : 200 GaAs substrate	RTA 450°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$1.4 - 1.9 \times 10^{-6}$ (40s)
Au : 2000 Zn : 500 Au : 200 GaAs substrate	RTA 450°for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$1.4 - 2.7 \times 10^{-6}$ (50s)

TABLE 3.10 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Au : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	Best values $1.6 - 1.8 \times 10^{-6}$ (60s)
Au : 2000 Zn : 700 Au : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$1.6 - 2.0 \times 10^{-6}$ (60s)
Au : 2000 Zn : 600 Au : 200 GaAs substrate	RTA 550°C for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$1.5 - 2.1 \times 10^{-6}$ (60s)
Au : 2000 Zn : 500 Au : 200 GaAs substrate	RTA 550° for 30s/40s/50s/60s in a N_2 atmosphere (optical furnace)	$p = 3 \times 10^{18}$	$1.4 - 2.0 \times 10^{-6}$ (60s)

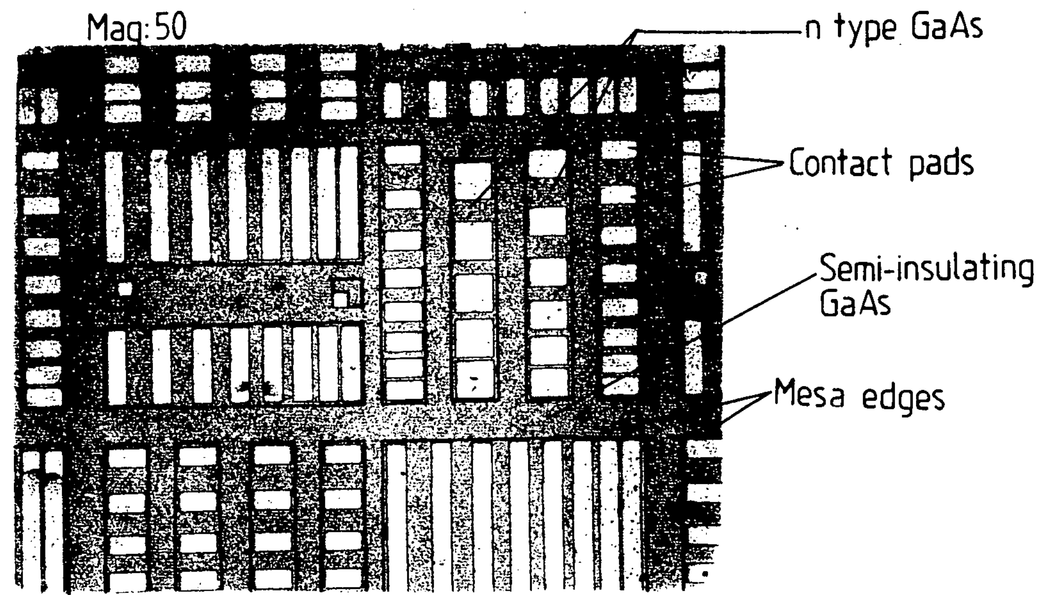


FIGURE 3.1.2(a) :Top view of TLMs for assessment of contact resistance. Contact pads consist of Au(2000Å)/Ni(200Å)/AuGe(600Å)/Ni(50Å)/GaAs alloyed at 450°C for 40s using RTA.

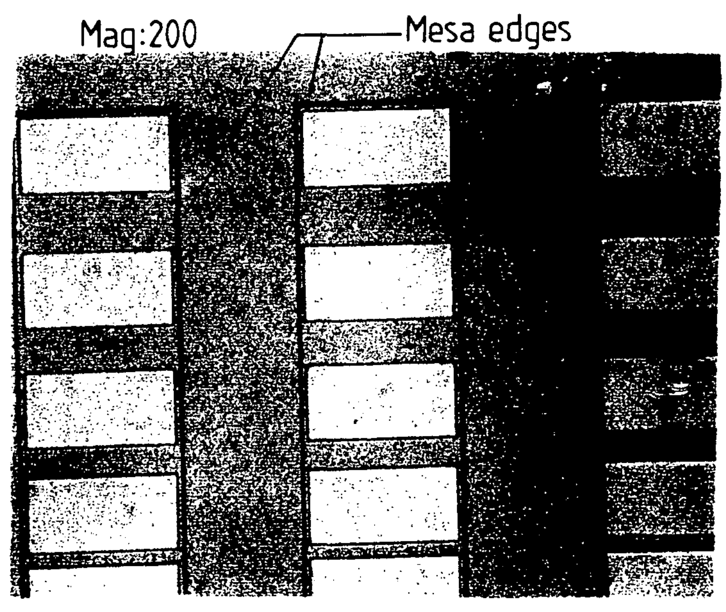
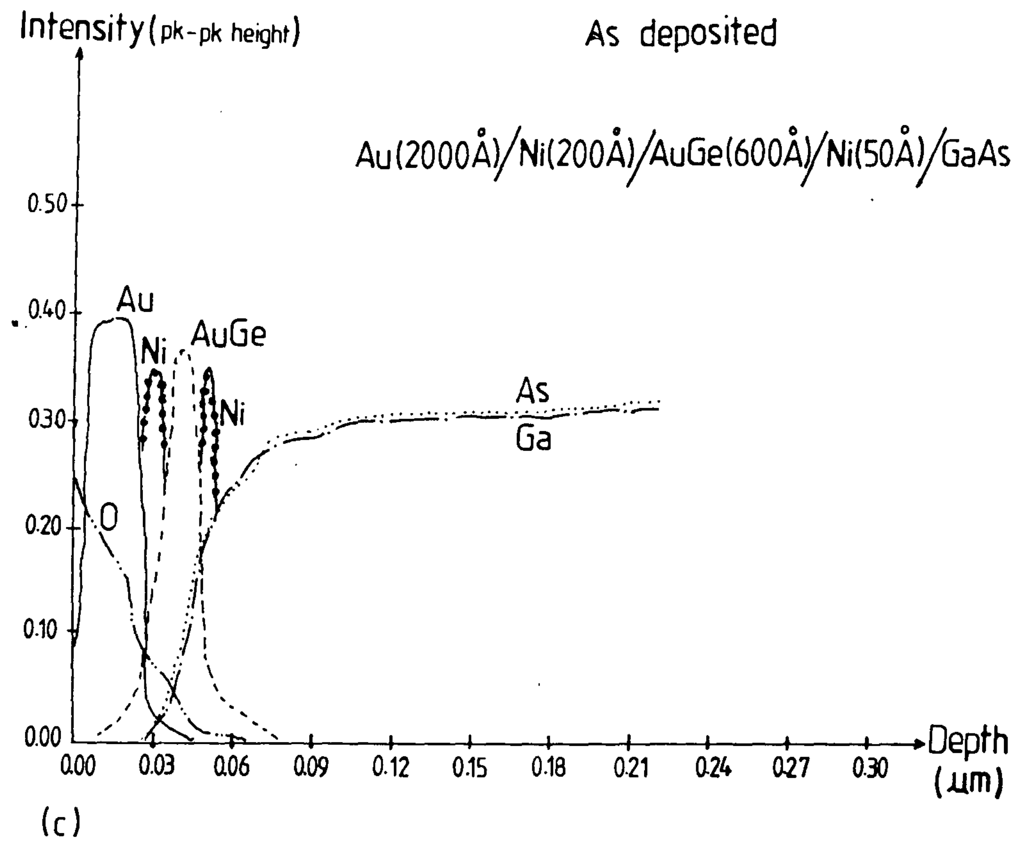
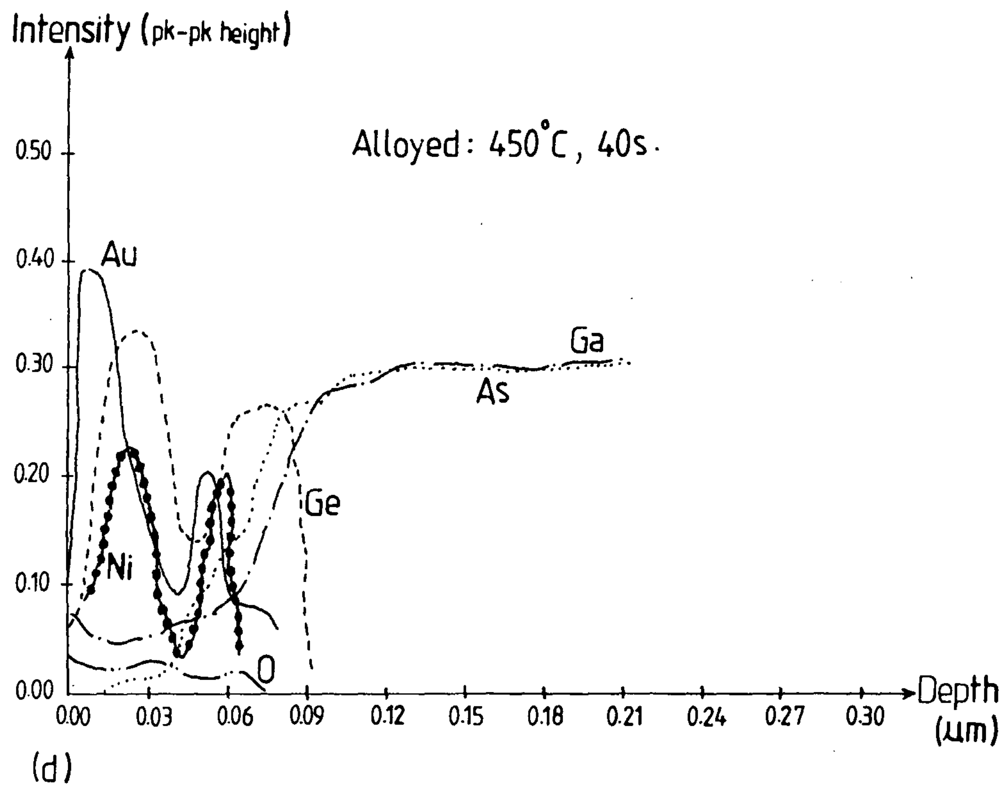


FIGURE 3.1.2(b) :Close up on TLMs pictured in (a) above shows smooth surface morphology of alloyed contacts.



(c)



(d)

FIGURE 3.1.2 :Auger Electron Spectroscopy profiles

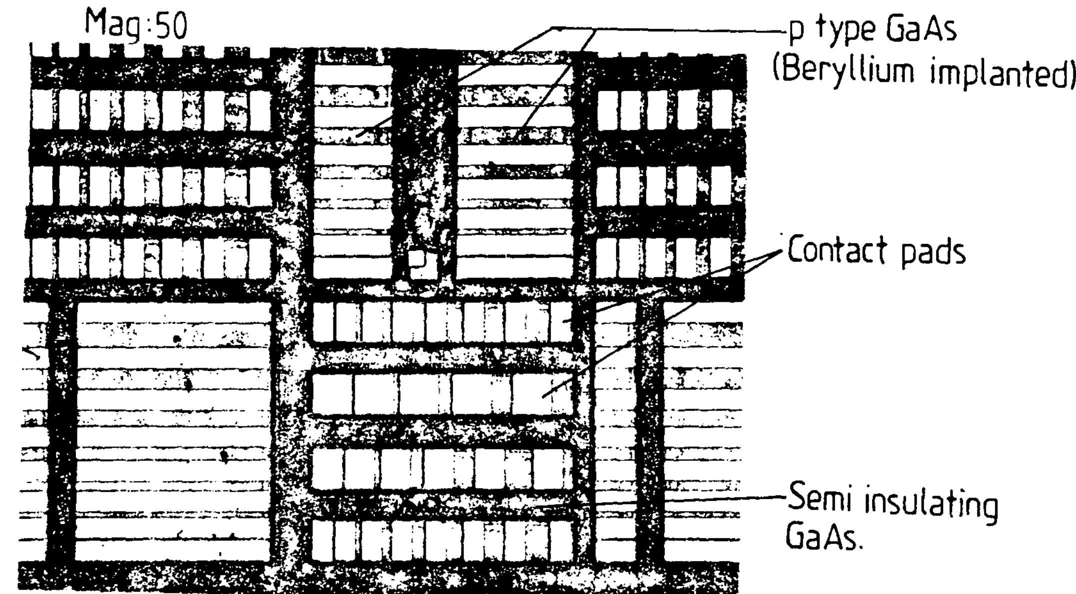


FIGURE 3.1.3(a): Top view of TLMs for assessment of contact resistance. Contact pads consist of Au(2000Å)/Zn(600Å)/Au(200Å)/GaAs alloyed at 450°C for 40s using RTA.

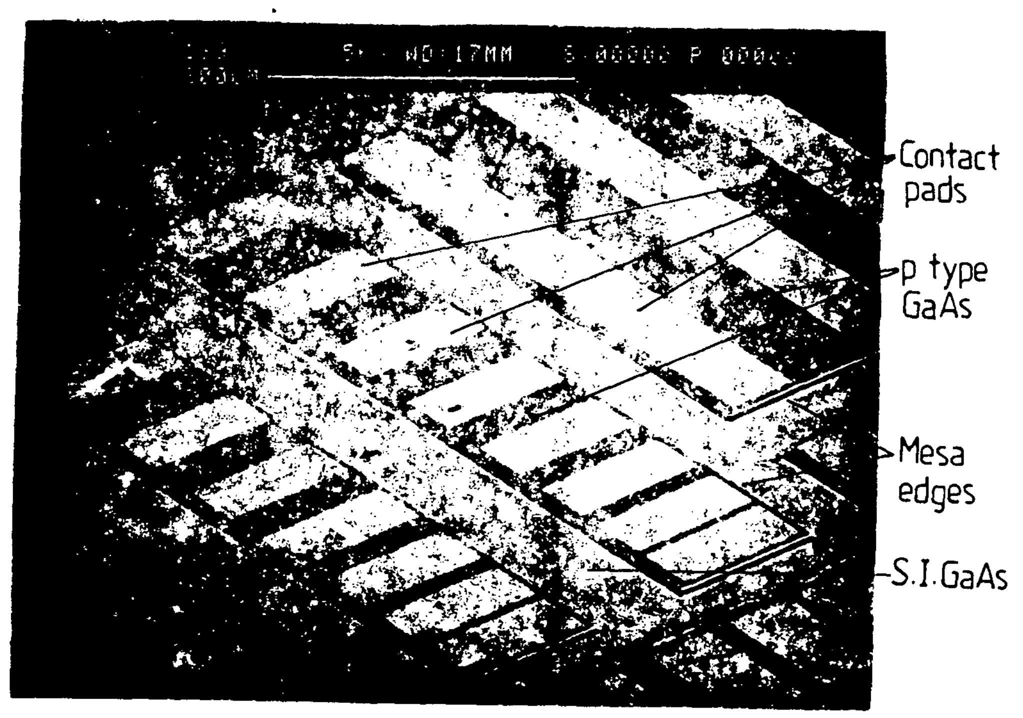
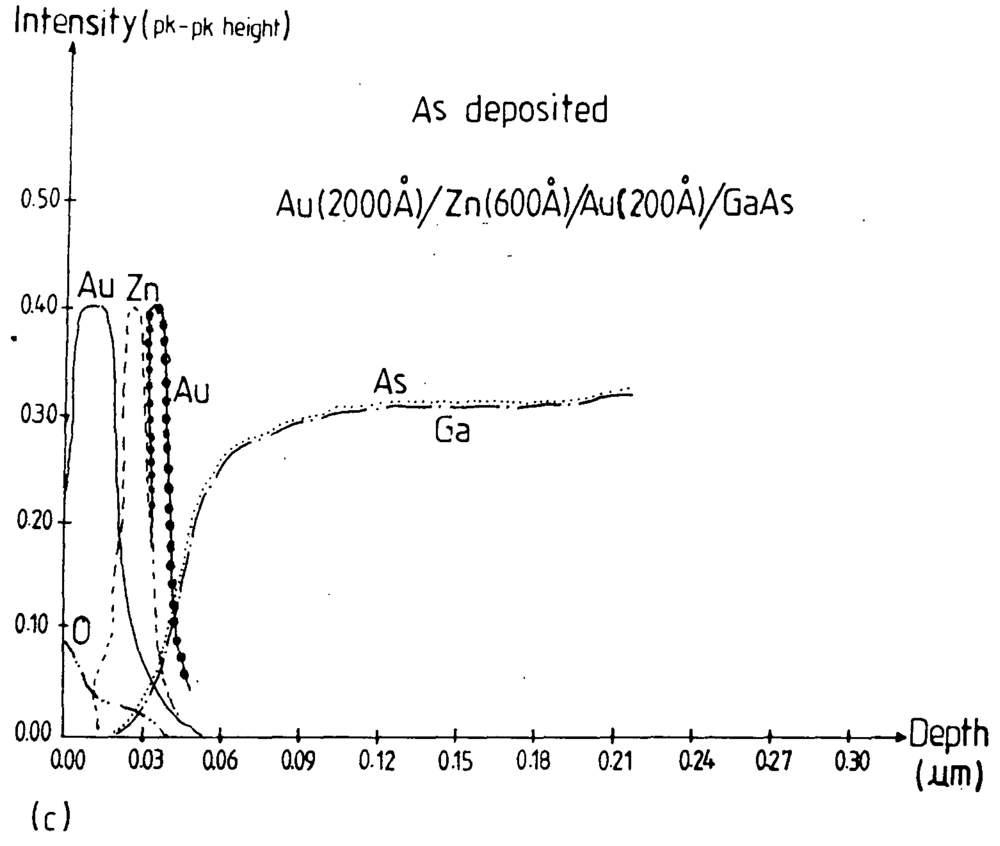
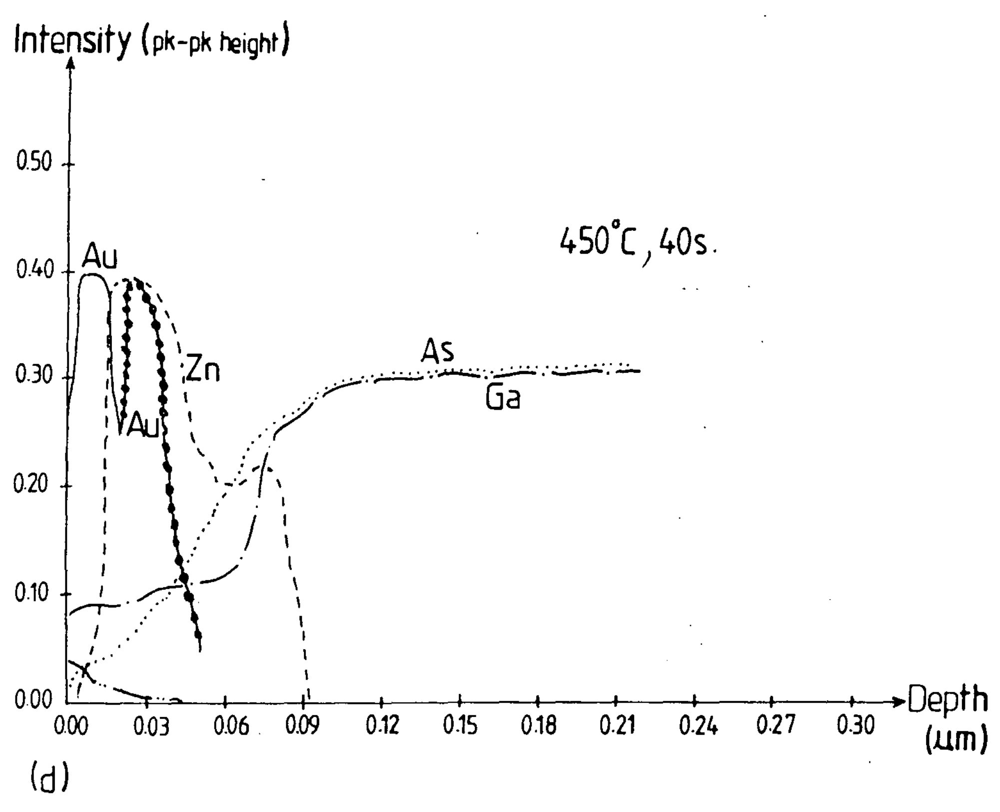


FIGURE 3.1.3(b): SEM micrograph of TLMs pictured in (a) above.

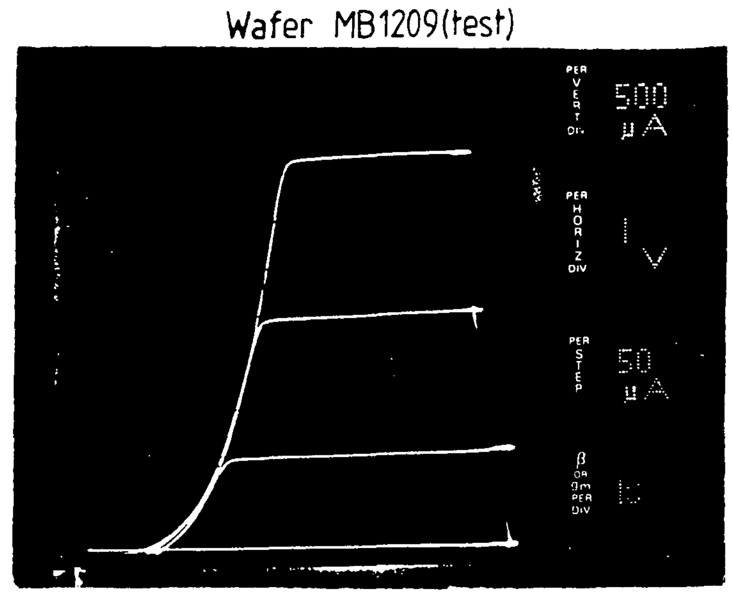


(c)

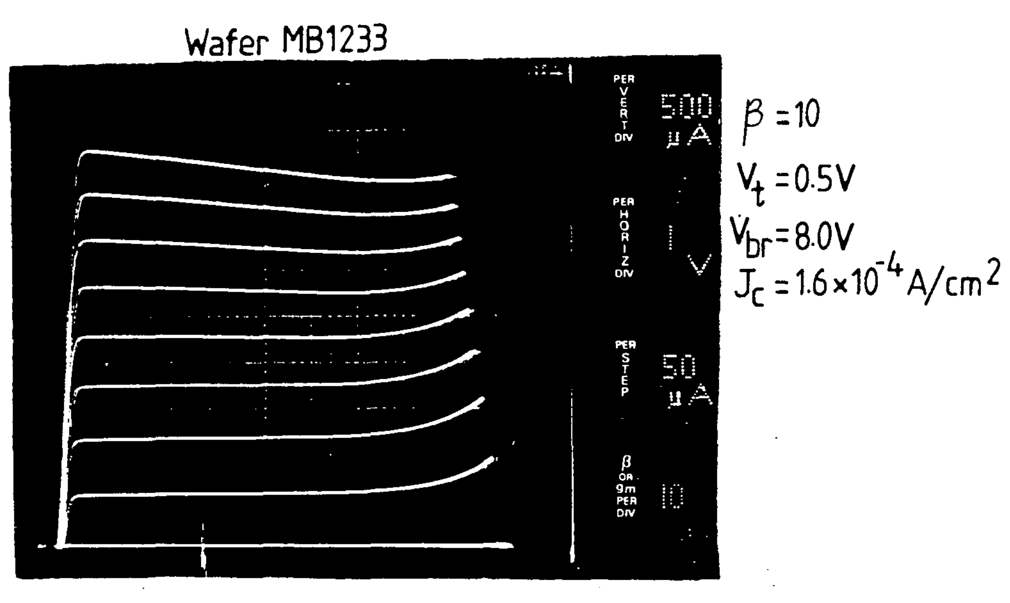


(d)

FIGURE 3.1.3 :Auger Electron Spectroscopy profiles



(a)Prior to ohmic contact alloying.



(b)After alloying.

FIGURE 3.1.4:Measured I-V characteristics for an 8µm HBT.

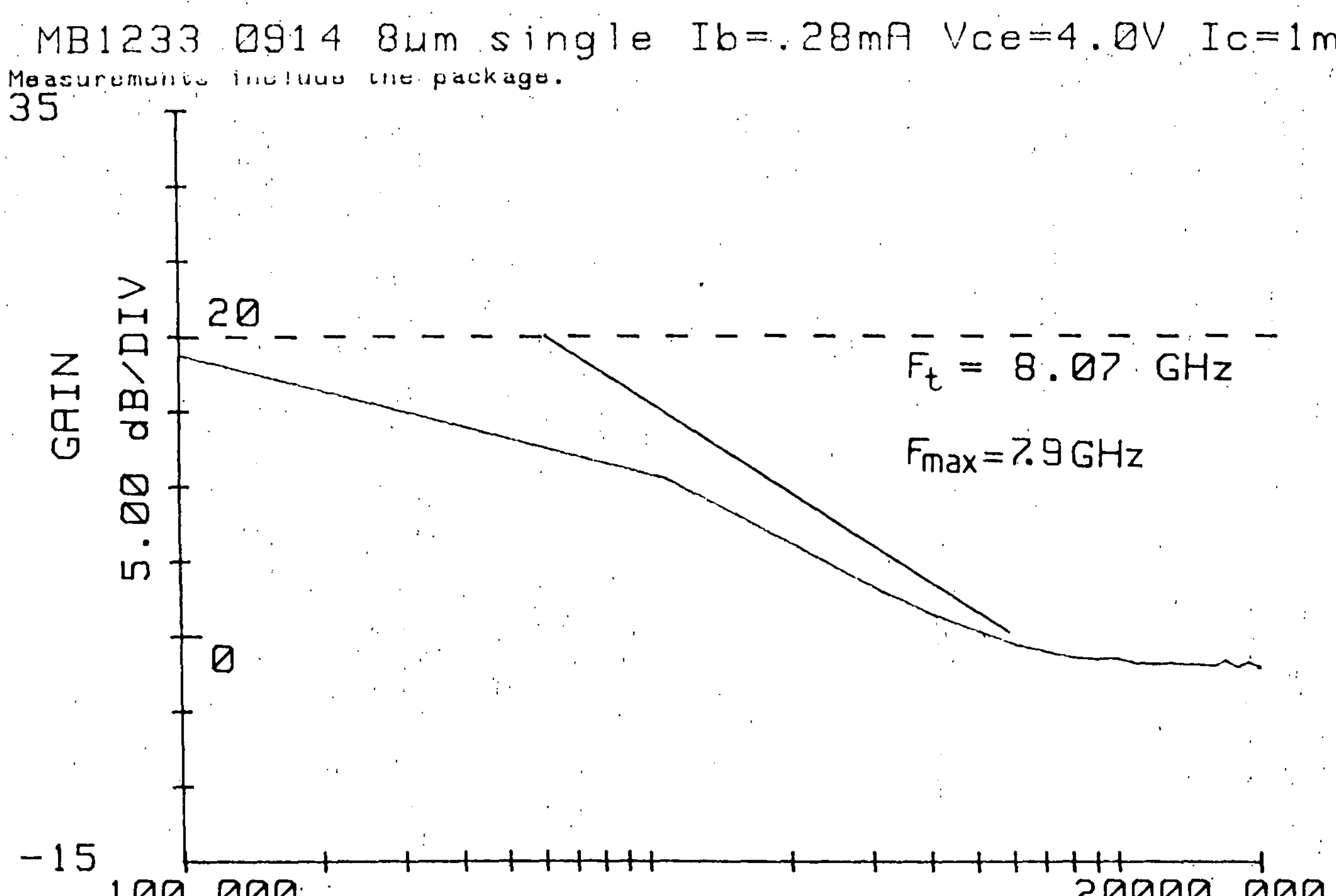


FIGURE 3.1.5: Current gain v/s frequency for a packaged 8 um HBT.

3.2.0: Fabrication of self-aligned HBTs

3.2.1: Surface preparation prior to processing

In addition to the techniques mentioned in section 3.1.1, a cleaning procedure used in the fabrication of self-aligned HBTs (SAHBTs) is `sputter cleaning´, also known as `sputter etch´. Prior to the deposition of refractory metals on to the emitter layer, it is necessary to clean the target (see Appendix A5) The reason for this clean is as follows: during the time that the sputtering system is open to air to load or unload it, the target will become contaminated by atmospheric pollution, by handling, or by chemical combination with the atmosphere to form an oxide or other compound. As a result, if this top layer was left on the target, the first period of sputtering would immediately transfer the contamination to the substrate. During the pre-sputtering period, when the first few atomic layers of the target are removed by sputtering, the shutter is thus left between the target and the substrate table, so that any contamination sputtered off deposits itself on to the shutter rather than the substrate. A similar `sputter clean´ procedure is then applied to the substrate, prior to deposition. In that way, any residual contamination present on the surface of the substrate is removed before metals are deposited.

In addition to the above, it is also standard practice for the sputtering system to be cleaned at regular intervals, with the emphasis being on the cleaning of the shutter and the inside of the chamber, to prevent accumulated layers of previously sputtered material to contaminate material used subsequently in the chamber.

3.2.2: Deposition of refractory metals

Refractory metals are those metals which show no oxidation or reactions at temperatures above 700°C. Their ability to withstand high temperature processing steps without deteriorating makes them very attractive for the self-aligned HBT process under investigation here. Properties of thin metal films on GaAs are important for understanding the behaviour of ohmic contacts. The growth of several metals on GaAs and other III-V compounds in molecular beam epitaxy systems have been studied recently [99].

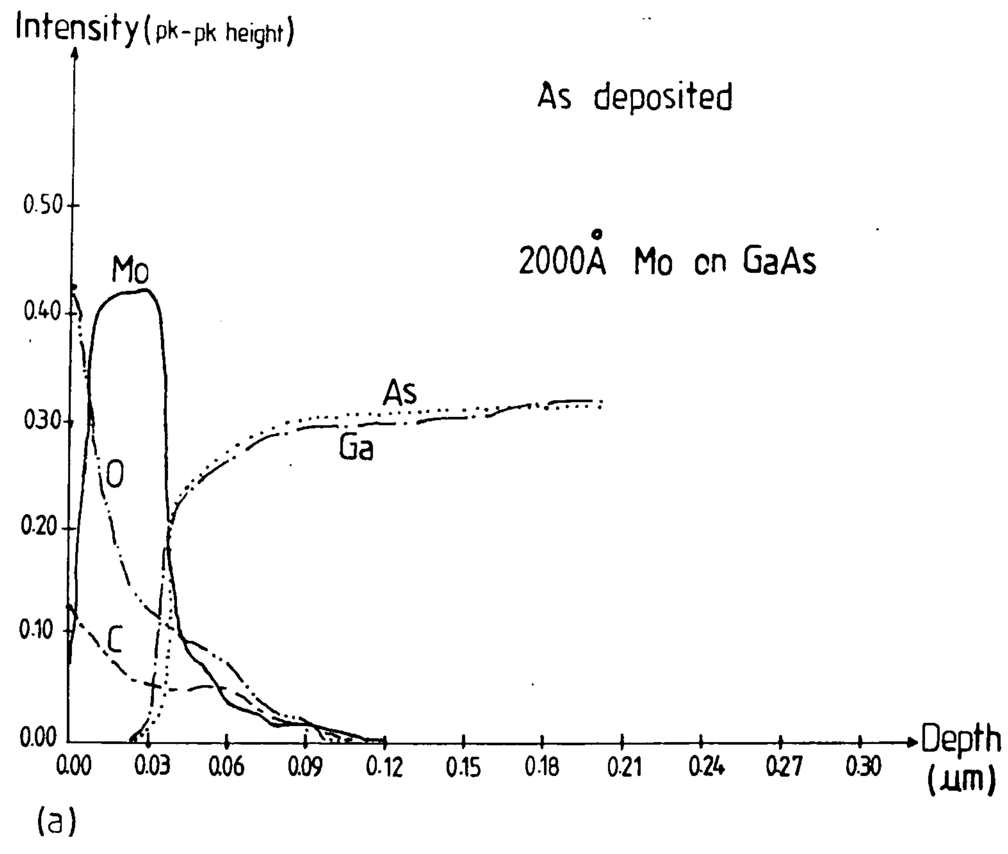
3.2.3: Optimising sputtering conditions

Three refractory metals (molybdenum, tungsten and nickel) are considered. Each of the metals mentioned above was first deposited individually on to separate semi-insulating GaAs at various Argon pressures and RF power settings. The sheet resistance of each deposited metal layer was then measured using a four-point probe and compared with the expected value of sheet resistance which is obtained from the following formula:

$$\text{Expected } R_{sh} = \frac{\text{Electrical resistivity of bulk metal at } 20^{\circ}\text{C}}{\text{Thickness of deposited layer}}$$

It must be remembered that prior to each deposition, the target is `sputter cleaned´ while the shutter is used to prevent any impurities from being deposited onto the substrates. After cleaning the target, some of the substrates were also cleaned prior to deposition.

The samples were then analysed by Auger electron spectrosopy (AES) which showed that a relatively large content of oxygen was present on the surface of the substrates that were not `sputter cleaned´ (figures 3.2.0, 3.2.1 and 3.2.2 (a) & (b)). The oxygen



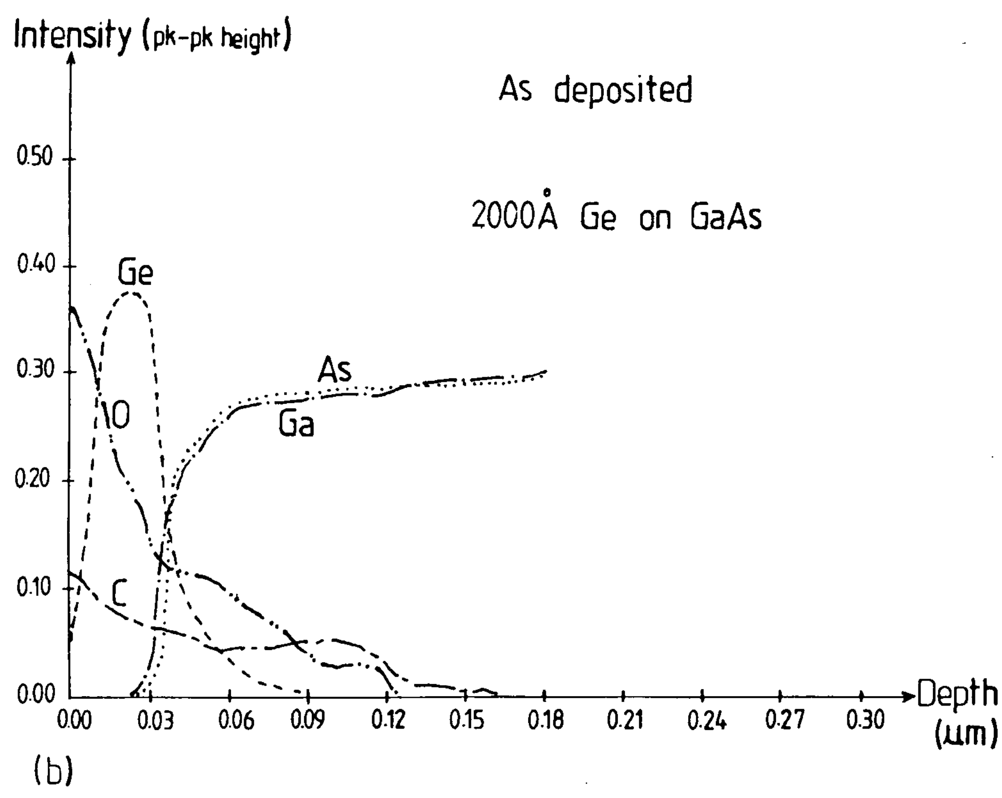
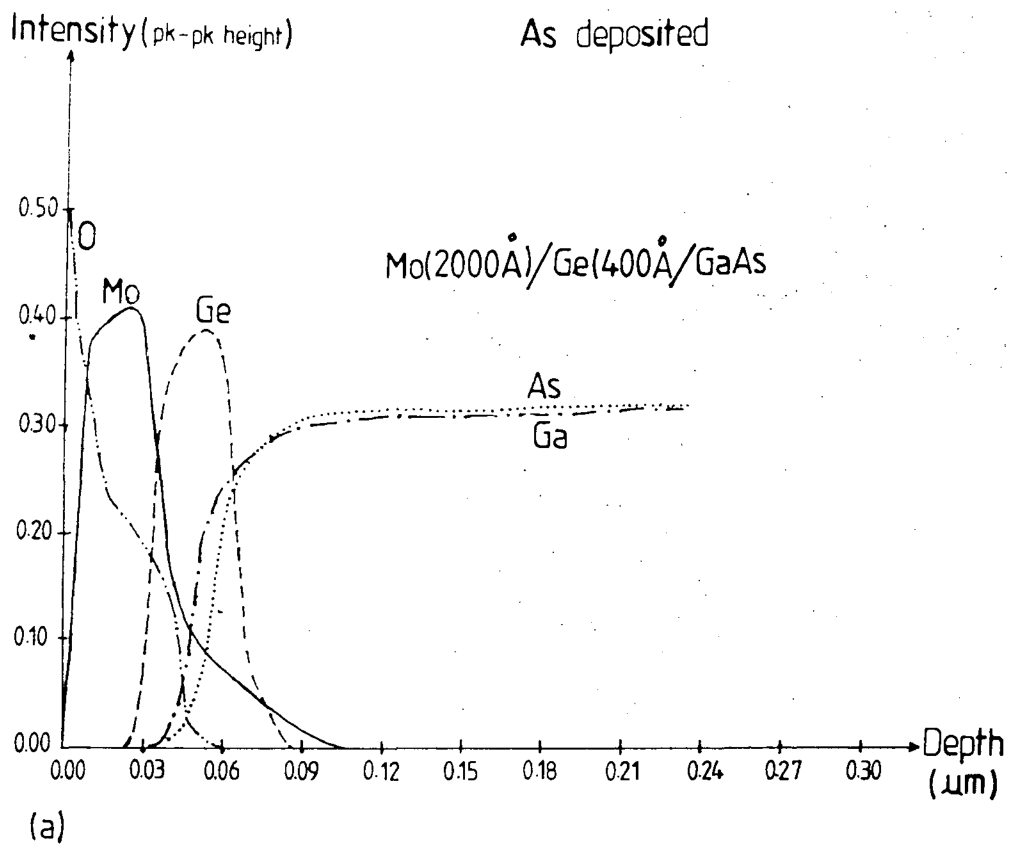


FIGURE 3.2.0 :Auger Electron Spectroscopy profiles



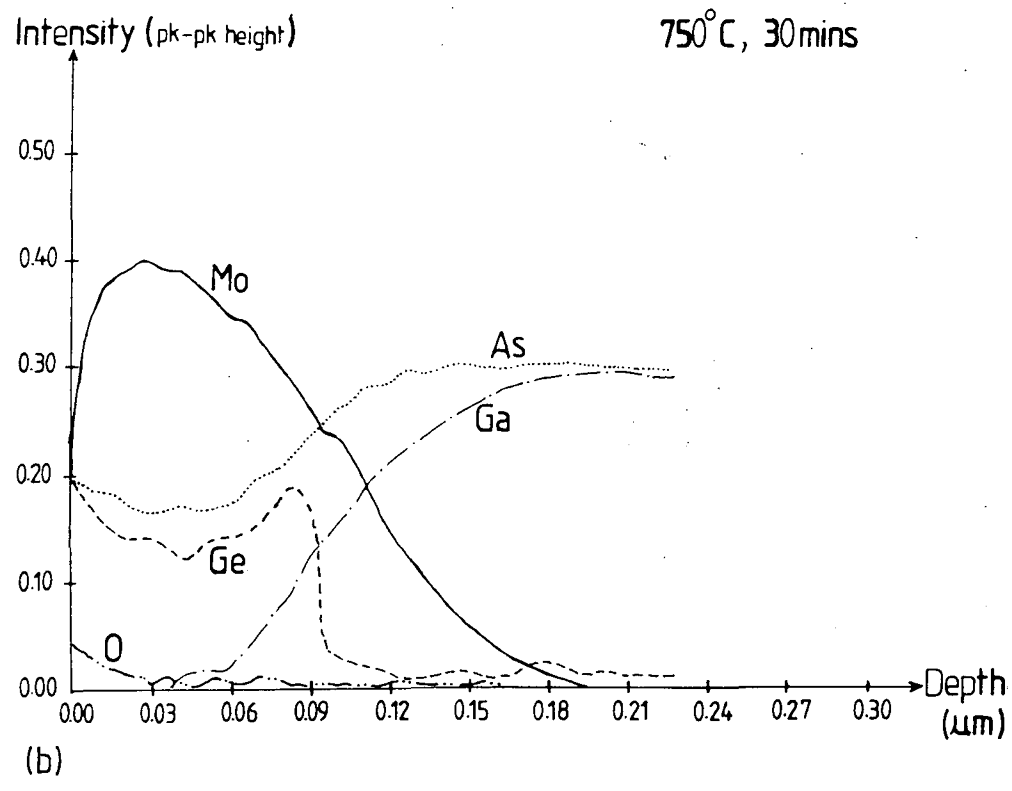
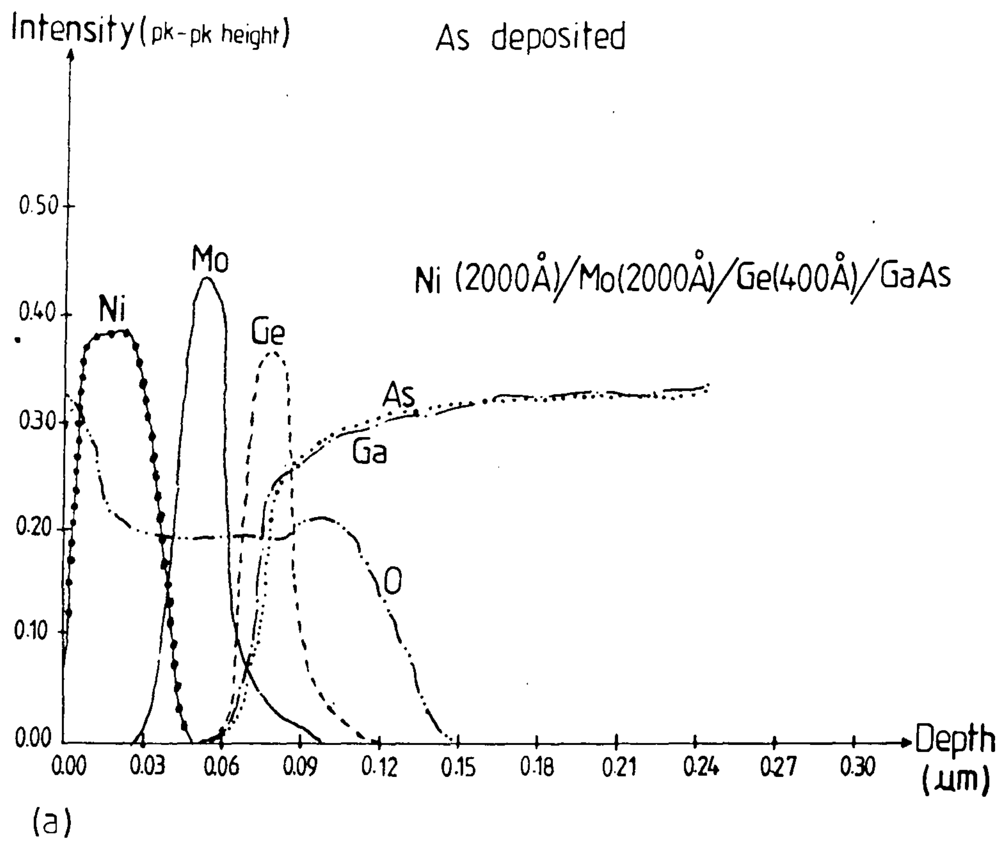


FIGURE 3.2.1 :Auger Electron Spectroscopy profiles



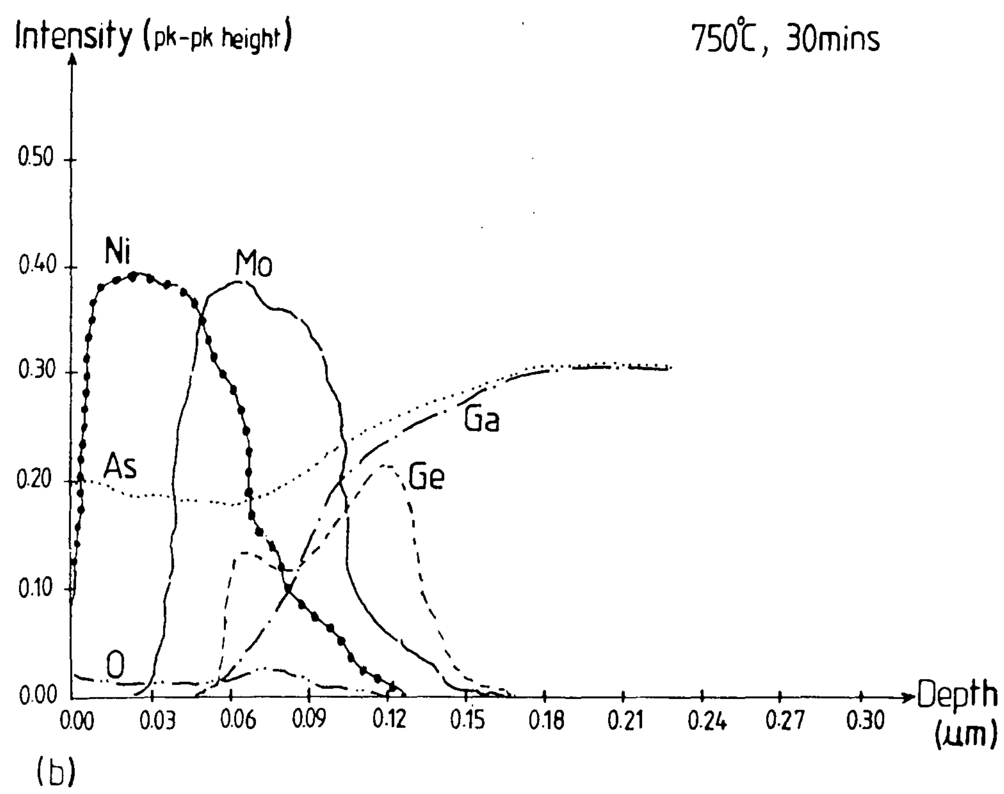


FIGURE 3.2.2 :Auger Electron Spectroscopy profiles

content was reduced to a minimum for the substrates that were cleaned by sputtering prior to deposition. Since the deposition of the refractory metals is done under very high vacuum (1 x 10^{-6}T) and Argon is used as sputtering gas, it is very unlikely that the oxygen will have originated from gases present inside the chamber at the time of sputtering. Since a small amount of Carbon is also present on the surface of the substrates without 'sputter cleaning', it is suspected that both the oxygen and Carbon are remnants of the organic solvent cleaning of the semiconductor surface prior to loading inside the chamber. Consequently, it is now common practice to 'sputter clean' target and substrate prior to any deposition.

3.2.4: Definition of Transmission line model on refractory metallisation for assessment of contact resistance.

Using the optimum sputtering conditions obtained previously, various metallisation systems consisting of Ge/Mo/W, Ge/Mo/Au and Ge/Mo/Ni were deposited on to n type GaAs with doping profile similar to the emitter of the HBTs. Photolithography, followed by ion beam milling, were then used to define the TLMs for measurement of contact resistance. Since the photolithography is performed after deposition of the metals, a negative of the pattern used for previous TLM definition is required. This is achieved by using resist reversal techniques to define the TLM pattern on the metal layers. It must be noted that deposition of the metals is not achieved through a photoresist pattern because during sputtering, the surface of the resist is also under bombardment and resist molecules are sputtered off and

[SELF-ALIGNED PROCESS]

TABLE 3.30 : Ohmic contacts for refractory metallisations

CONTACT STRUCTURE Metals/Thickness (Å)	HEAT TREATMENT Temp/Time/Ambient gas/Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\,cm^2$)
W : 2000 Mo : 1000 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	Best values $2.4 - 2.5 \times 10^{-4}$ (30mins)
W : 2000 Mo : 1200 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$2.2 - 2.3 \times 10^{-4}$ (30mins)
W : 2000 Mo : 1400 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$4.4 - 4.6 \times 10^{-5}$ (30mins)
W : 2000 Mo : 1600 Ge : 400 GaAs substrate	FA 750° for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$1.2 - 1.4 \times 10^{-5}$ (30mins)

TABLE 3.30 :Ohmic contacts for refractory metallisations

CONTACT STRUCTURE Metals/Thickness (Å)	HEAT TREATMENT Temp/Time/Ambient gas/Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE (Ω cm^2)
W : 2000 Mo : 1800 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	Best values $1.2 - 1.3 \times 10^{-5}$ (30mins)
W : 2000 Mo : 2000 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$1.2 - 1.25 \times 10^{-5}$ (30mins)
Ni : 2000 Mo : 1000 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$9.7 - 9.8 \times 10^{-6}$ (30mins)
Ni : 2000 Mo : 1200 Ge : 400 GaAs substrate	FA 750° for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$9.5 - 9.8 \times 10^{-6}$ (30mins)

TABLE 3.3.0 : Ohmic contacts for refractory metallisations

CONTACT STRUCTURE Metals/Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\,cm^2$)
Ni : 2000 Mo : 1400 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	Best values $4.6 - 4.8 \times 10^{-6}$ (30mins)
Ni : 2000 Mo : 1600 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$2.9 - 3.75 \times 10^{-6}$ (30mins)
Ni : 2000 Mo : 1800 Ge : 400 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$2.3 - 3.0 \times 10^{-6}$ (30mins)
Ni : 2000 Mo : 2000 Ge : 400 GaAs substrate	FA 750°for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$	$1.9 - 2.0 \times 10^{-6}$ (30mins)

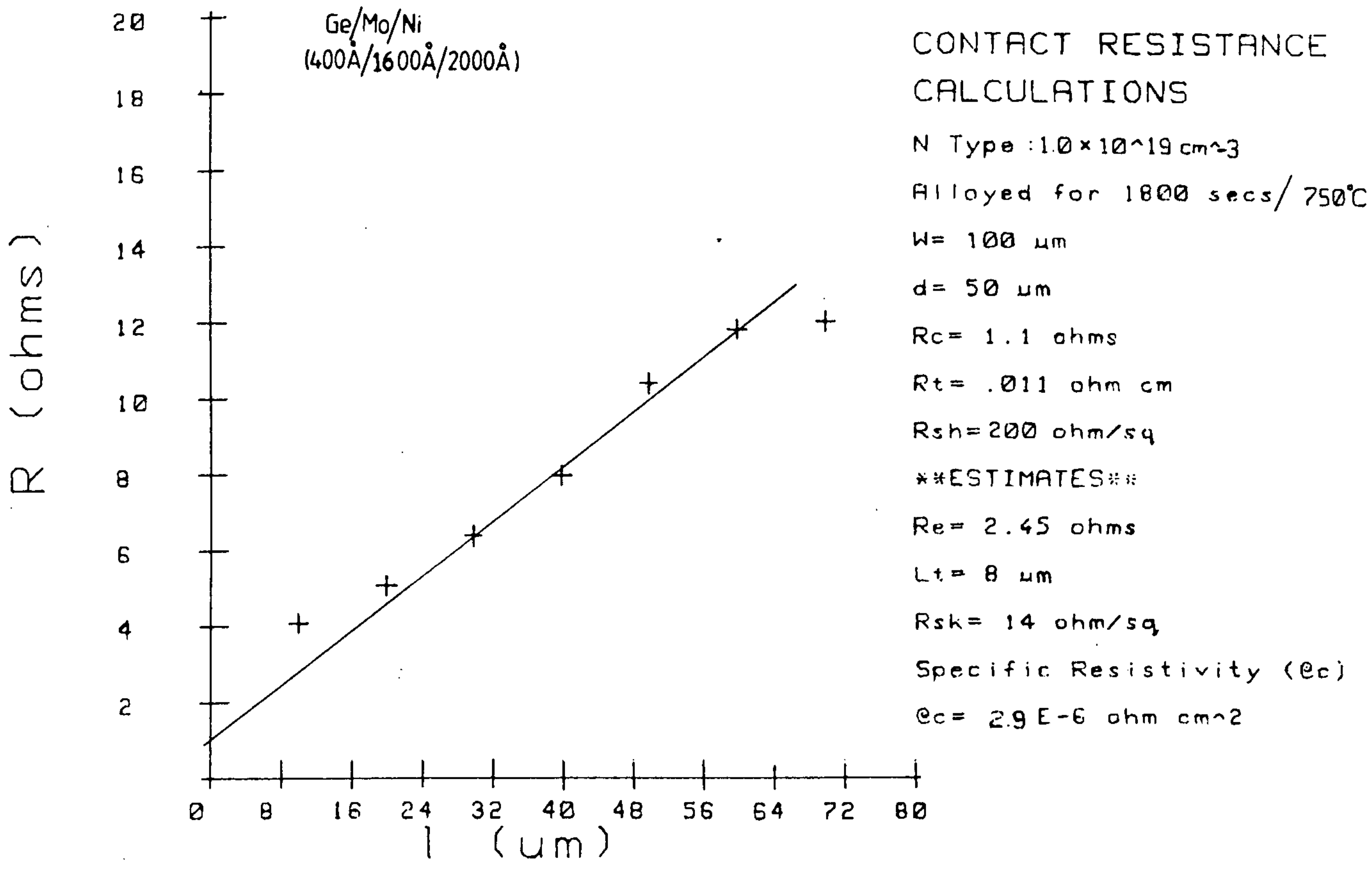


FIGURE 3.2.3:Plot of TLM results for assessment of contact resistance.

redeposited in unwanted regions on the wafer. This problem is eliminated by depositing the metals first and then patterning them into contact pads. As for the conventional process, different annealing conditions were applied to the substrates and contact resistance values were measured for each condition.

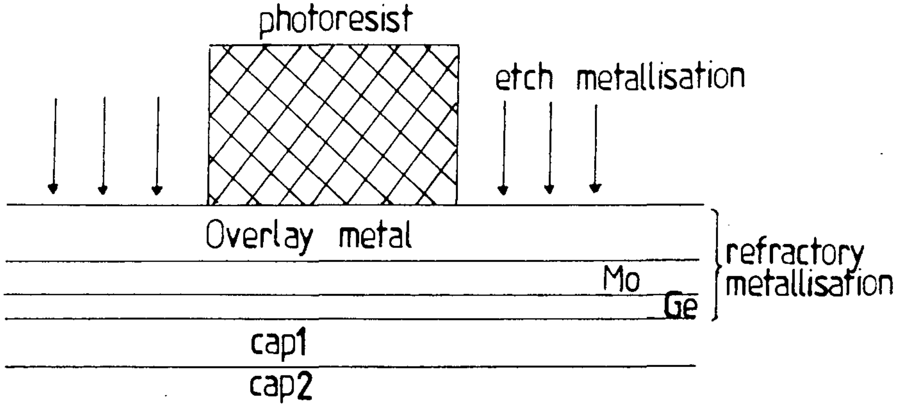
3.3.0: Definition of T-shaped emitter contact

3.3.1: Using dry etching

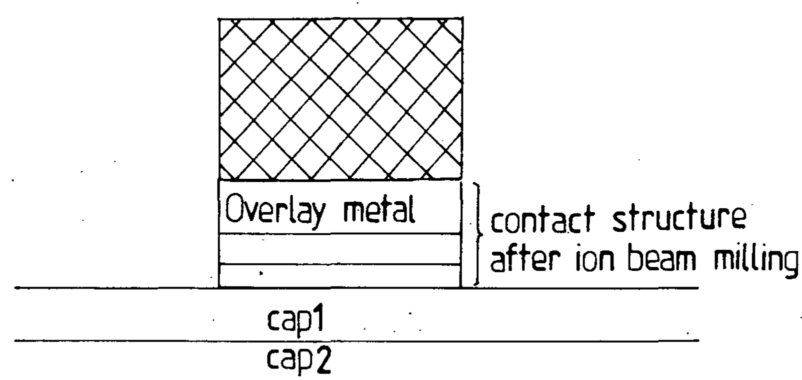
Once the metals have been deposited by sputtering on to the samples, it is necessary to pattern the emitter in the top region of the metal. The process involves patterning the overlay metal surface with a suitable resist pattern, then using a dry etching technique (ion beam milling, reactive ion beam etching and/or reactive ion etching) to etch off the metals outside the resist (figure 3.3.0).

Ion beam milling can be used to etch only the overlay metal because of its directional nature. It cannot be used to undercut the underlay metal layers as it would thus defeat the purpose of trying to achieve a T-shaped contact structure (figure 3.3.0 (a) & (b)).

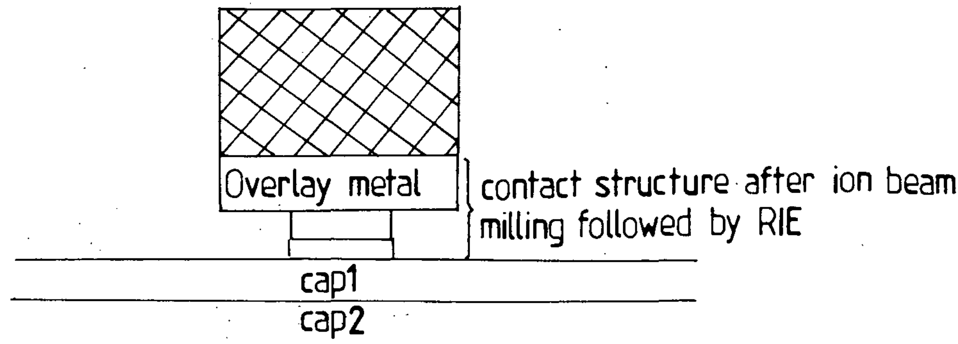
Reactive ion etching (RIE) provided the means of etching the underlay metal layers while leaving the overlay metal intact, thus undercutting the latter and forming a T-shape. The two combinations of gases used, $SF_6:N_2$ and $CF_4:O_2$, successfully etched the Ge/Mo/W and Ge/Mo/Au layers into a T-structure but failed to etch nickel in the metallisation system Ge/Mo/Ni. A T-structure was thus achieved in the latter system by first etching the Ni by ion beam milling or wet chemical etching (see later).



(a) Define emitter contact pattern by photolithography.



(b) Define emitter contact by etching metals using ion beam milling.



(c) Define emitter contact by etching metals using ion beam milling for the overlay metal and reactive ion etching for the remaining layers of the metallisation.

FIGURE 3.3.0 : Various etching techniques are used to form the T shaped contact structure.

With the isotropic nature of the RIE, different extents of undercutting the underlay metal layers were achieved by altering the various parameters that alter etching behaviour, namely:

(i) Etch time;

(ii) Ratios of gases admitted (eg: $CF_4:O_2$ and $SF_6:N_2$);

(iii) Gas flow rate into the chamber;

(iv) Pressure inside the system;

(v) Power density inside the chamber.

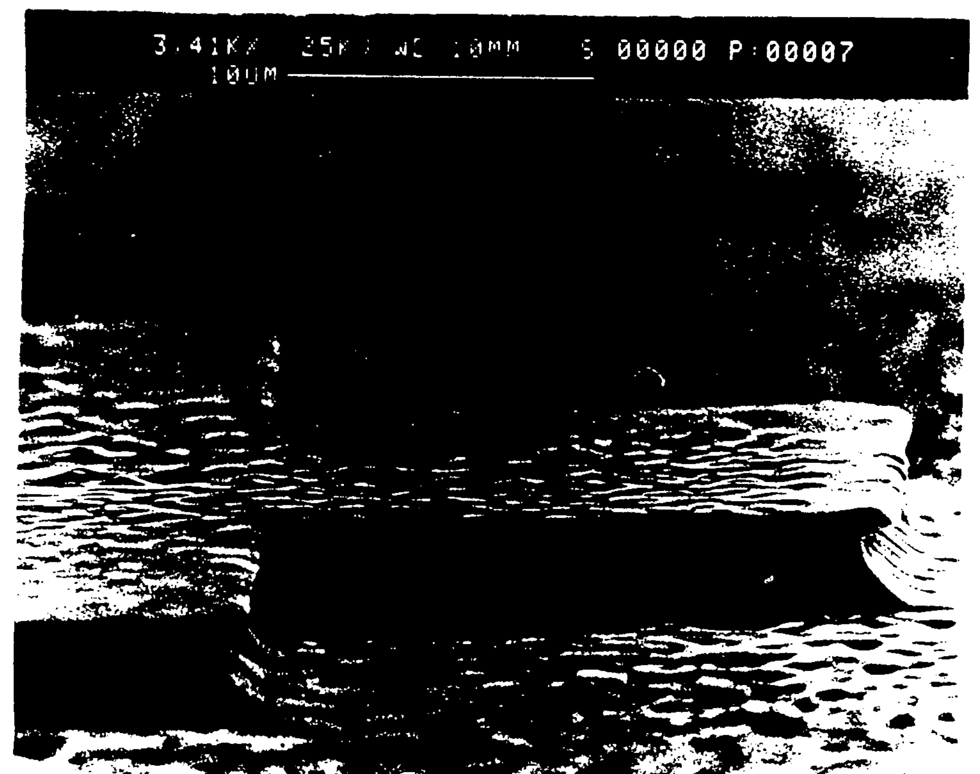
The effects on the etch profile were observed using scanning electron microscopy (SEM) and are shown in figures 3.3.1 (a) to (j).

3.3.2: Using wet chemical etching for the overlay metal

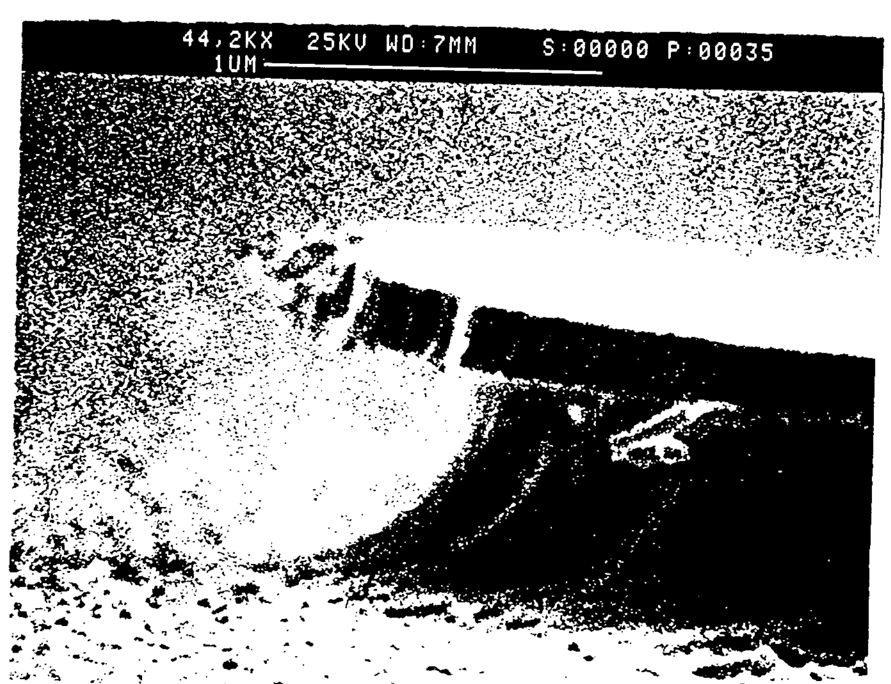
Wet chemical etching can be used to etch the overlay metal, while the other metallic layers are etched using reactive ion etching. Wet etching has the advantage of providing a means of reducing the dimensions of the the overlay metal and consequently, obtaining devices with much smaller active regions with no additional difficulties to the photolith definition. One disadvantage, however, is that the etchant used must be chosen carefully so that it does not react with the metal directly under the overlayer and this is a very important factor in the choice of overlay metal.

(a) Gold etch:-

Due to its unreactive nature, gold is by far the most difficult metal to etch and therefore, the conditions required for the etchant are particularly critical. The strongest factor influencing the ratio of constituents for the gold etchant can be seen from the graph shown in figure A7 which illustrates the



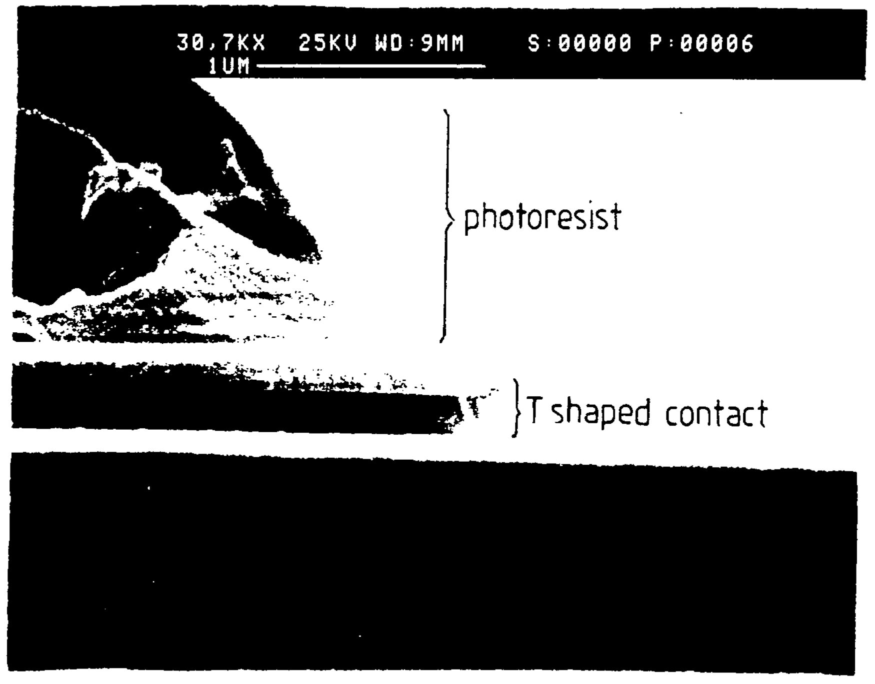
(a) Ge(400Å)/Mo(2000Å)/Au(2000Å) etched in SF_6:N_2 (160:40 sccm) at 150 mT and 50 W for 2 mins.



(b) Ge(400Å)/Mo(2000Å)/Au(2000Å) etched in SF_6:N_2 (160:80 sccm) at 150 mT and 50 W for 6 mins.

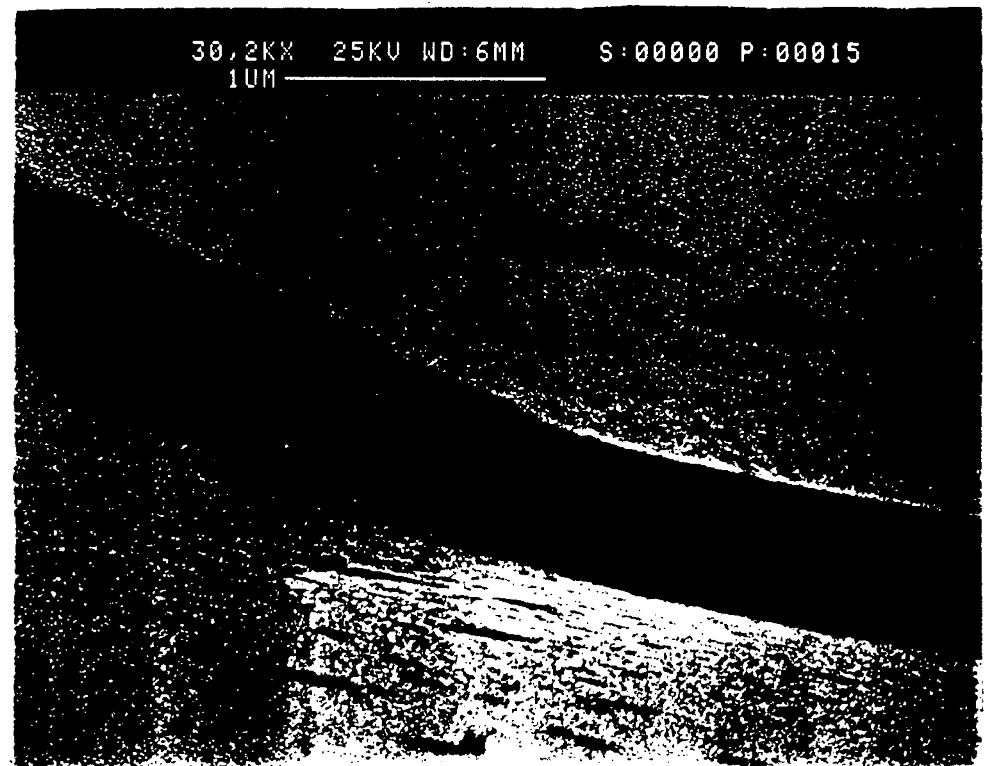
FIGURE 3.3.1 : SEM micrographs of T-shaped contact structures.

(c) Ge(400Å)/Mo(2000Å)/Au(2000Å) etched in $CF_4:O_2$ (80:10 sccm) at 150 mT and 50 W for 3mins. Alloyed at 750°C for 30mins.

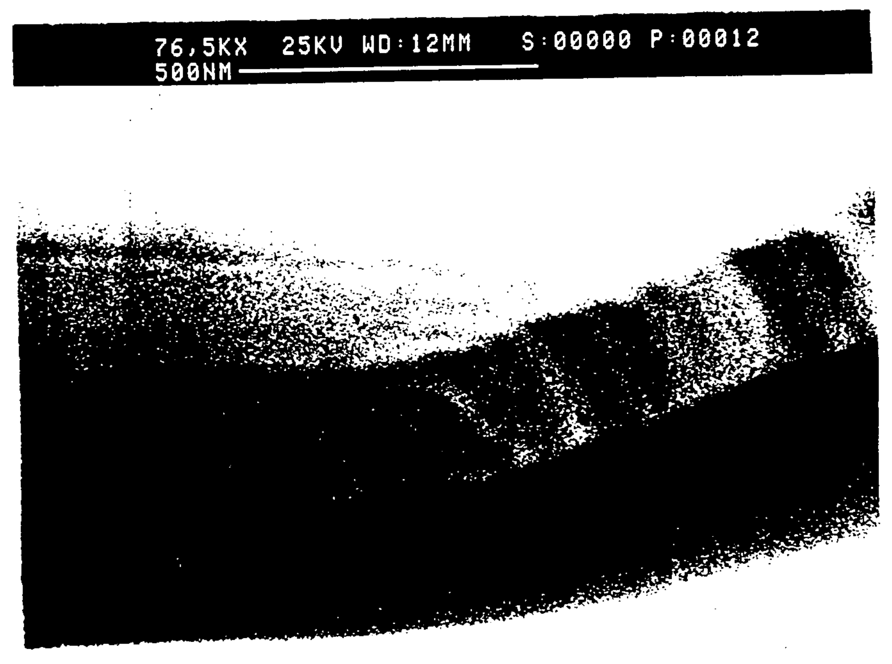


(d) Ge(400Å)/Mo(2000Å)/W(2000Å) etched in $SF_6:N_2$ (30:10 sccm) at 150 mT and 100W for 3mins.

FIGURE 3.3.1 : SEM micrographs of T-shaped contact structures.

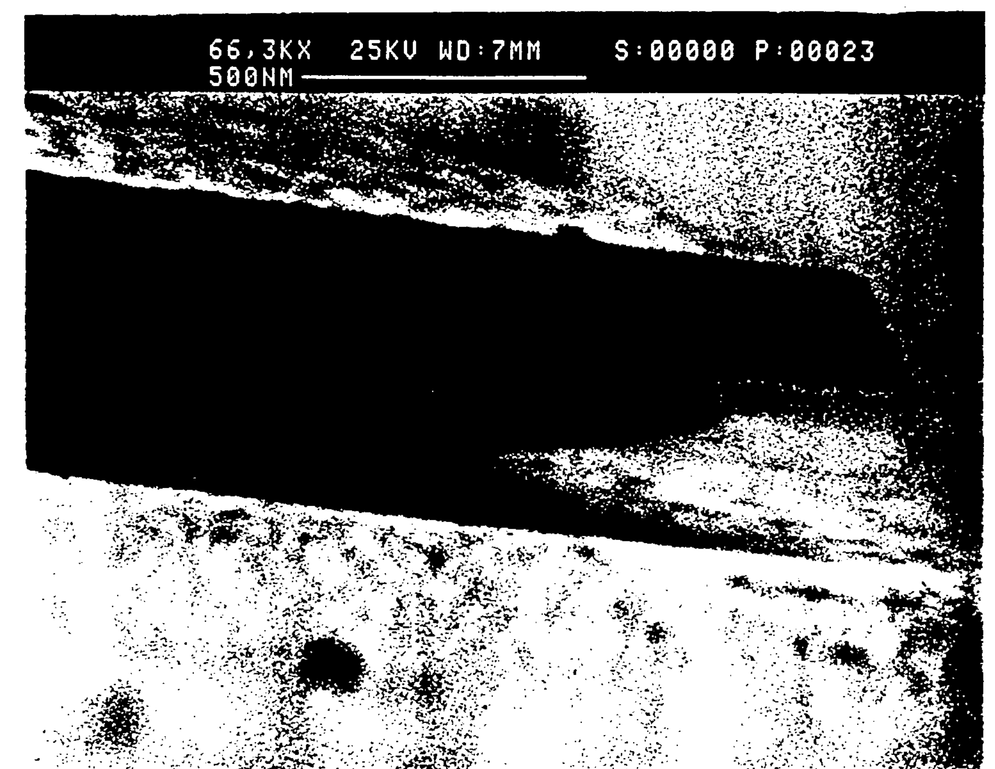


(e) Ge(400Å)/Mo(2000Å)/Ni(2000Å) etched by ion beam milling (for Ni) followed by $SF_6:N_2$ (160:20sccm) at 150mT and 50W for 3mins.

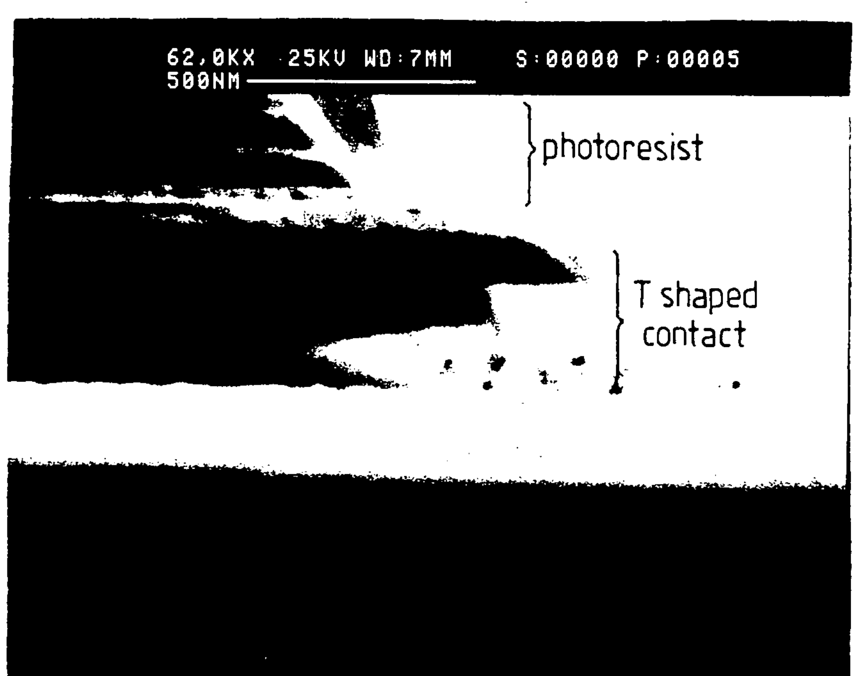


(f) Ge(400Å)/Mo(2000Å)/Ni(2000Å) etched by ion beam milling (for Ni) followed by $CF_4:O_2$ (160:20 sccm) at 150mT and 50W for 3mins.

FIGURE 3.3.1 : SEM micrographs of T-shaped contact structures.

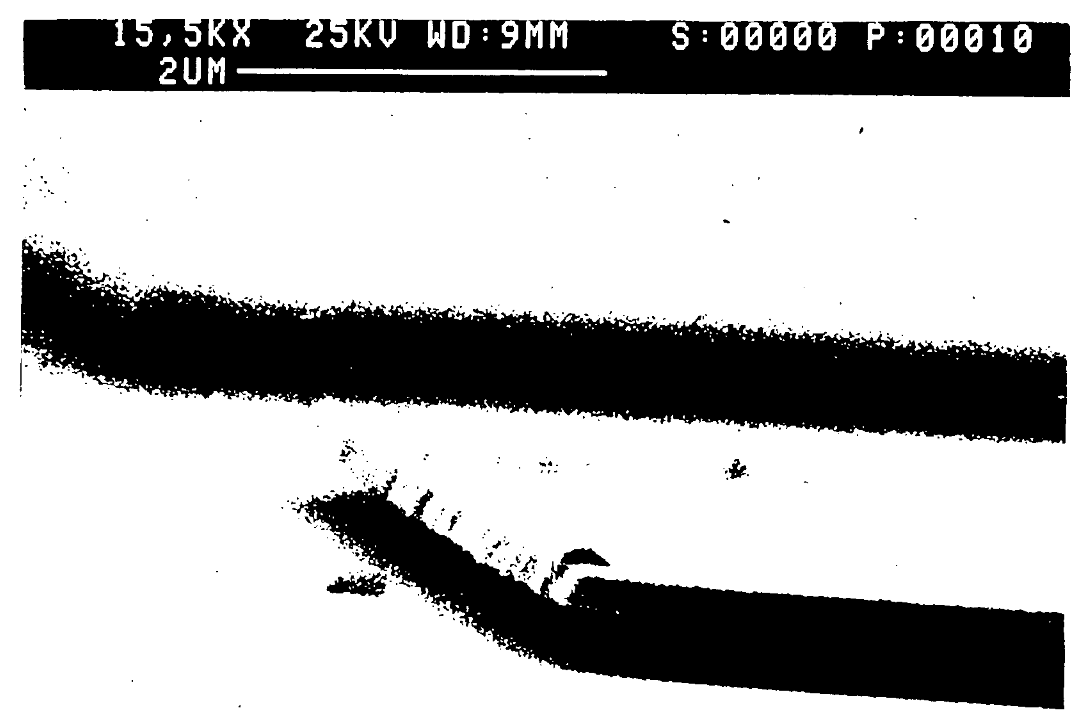


(g) Ge(400Å)/Mo(2000Å)/Ni(2000Å) etched by (i) wet etching, followed by (ii) RIE, $SF_6:N_2$ (30:10 sccm) at 300 mT and 100W for 2mins.



(h) Ge(400Å)/Mo(2000Å)/Ni(2000Å) etched using the optimum conditions given in (g) above.

FIGURE 3.3.1 : SEM micrographs of T-shaped contact structures.



(i) Overall view of T shaped contacts defined using optimum conditions given in (g).

(j) Overall view of T shaped contacts defined as in (g).

FIGURE 3.3.1 : SEM micrographs of T-shaped contact structures.

TABLE 3.2.0 Characterisation of Nickel etch

{ ACETIC ACID 1250 ml; ORTHOPHOSPHORIC ACID 250 ml; NITRIC ACID 750 ml; SULPHURIC ACID 250 ml }

Conc. of etchant (etchant/DI water)	Etch time (s)	Etched depth (Å)	Etch rate = Etch depth (Å) / Etch time (s)	COMMENTS
250ml pure etchant	5	–	–	Pattern destroyed
250ml/125ml	5	–	–	As above
250ml/250ml	5	4000 Å	800 Å/s	Photoresist pattern slightly etched & etch rate too fast;
250ml/500ml	5	800 Å	40 Å/s	Etch rate still too fast for controllable etching;
250ml/750ml	5	50 Å	10 Å/s	Pattern unaffected. Good etch rate needs to be verified;
250ml/750ml	10	105 Å	10 Å/s	For etchant/DI water (1:3), etch rate of Ni is 10 Å/s;
250ml/750ml	50	496 Å	10 Å/s	As above
250ml/1000ml	5	32 Å	6 Å/s	Very good etch rate makes etching very controllable;
250ml/1000ml	50	304 Å	6 Å/s	As above
250ml/1000ml	300	1797 Å	6 Å/s	As above.

selective etching behaviour of the system iodine/potassium iodide (I_2/KI) for GaAs, AlGaAs (with 30% Al) and non-selective etching. The region of non-selective etching is desirable as it is gold which is required to be etched and not GaAs or AlGaAs. The choice of the concentration of the etchant was also based on previous experimental results [100].

(b) Nickel etch:-

Nickel proved to react adequately with relatively dilute solutions of sulphuric acid (less than 10%). The problem in this case is that the sulphuric acid also attacks the molybdenum layer under the nickel, which makes it difficult to control the etching stopping point.

As an alternative to sulphuric acid, a homogeneous mixture of the constituents listed below was used as etchant:

Acetic acid :	1250 $\pm$ 20 ml
Orthophosphoric acid :	250 $\pm$ 10 ml
Nitric acid :	750 $\pm$ 5 ml
Sulphuric acid :	250 $\pm$ 10 ml

The etchant was mixed with de-ionised water in order to vary its concentration and Nickel layers deposited on dummy wafers were patterned and etched using different concentrations of etchant. Results are given in Table 3.3.0 .

3.4.0: Wet chemical etching of Capl

The cap layer is heavily doped n type in order to provide good ohmic contact resistance to the emitter. Etching the cap serves the purpose of removing that heavily doped region where ion implantation to the base will take place, since it is more

FIGURE 3.4.0

photoresist

refractory metallisation

C1 — cap1 n^+-GaAs

C2 — cap2 n-GaAs

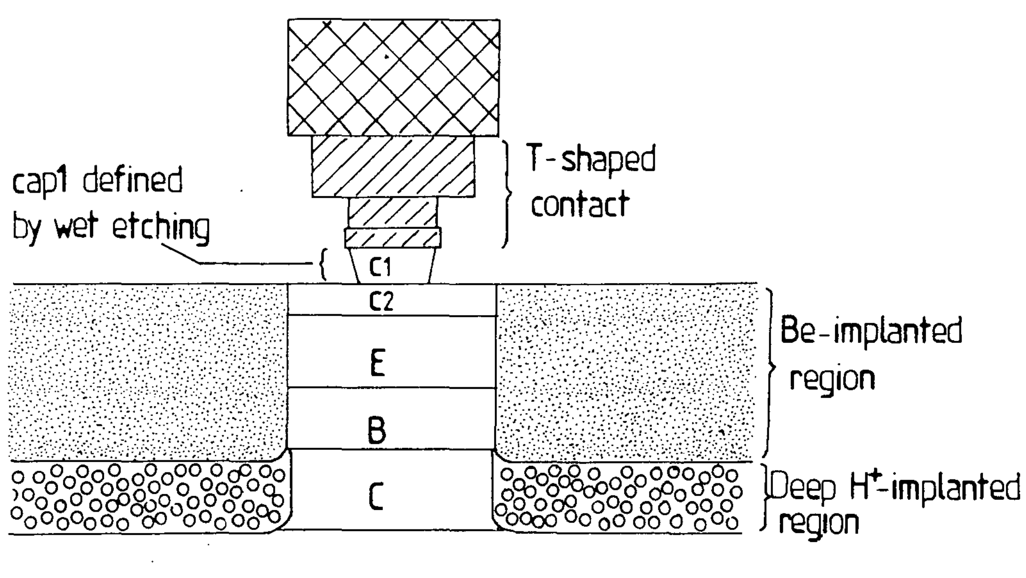
E — emitter n-$Al_xGa_{1-x}As$

B — base p^+-GaAs

C — collector n^--GaAs

collector buffer n^+-GaAs

a)(i)Clean GaAs surface; (ii)Deposit refractory metallisation;(iii)Define emitter contact pattern by photolithography.



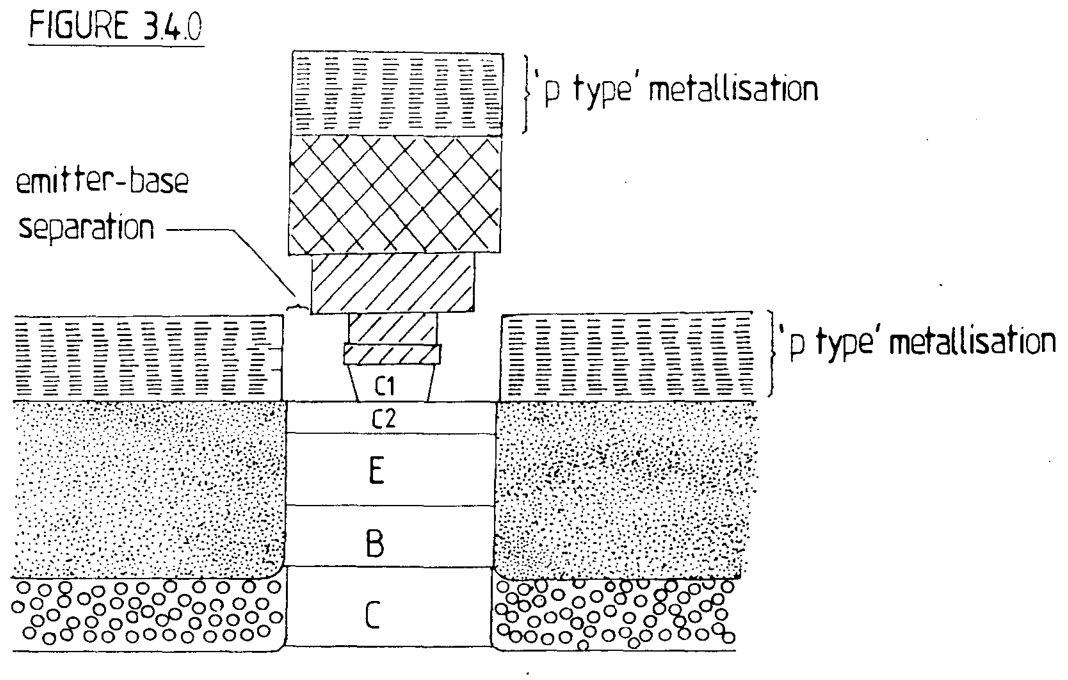
b)(i)Define T-shaped contact by etching;(ii)Wet etch cap1;(iii)Implant protons in the extrinsic collector region;(iv)Implant beryllium to form the base contact regions.

difficult to change a heavily doped n type region into a heavily doped p type region than it is to change a lightly doped n type region such as the emitter (figure 3.4.0(a) and (b)). A second advantage of etching the cap layer off in the areas selected for ion implantation is that it provides alignment marks for subsequent photolithographic levels. It must be noted that wet etching of the cap layer is achieved while the photoresist pattern for the emitter contact is still there (figure 3.4.0(b)). The reason for not removing the photoresist is that it will be used as the masking pattern for the implantation to the base. The T-shaped contact itself could be used as a mask [38] to the implantation but in doing so, the separation required between the emitter contact and the base contact in order to destroy the lateral diode caused by implantation will not be available (figure 3.4.0(c)). It is also worthwhile at this stage to remember that the etchant must be carefully chosen in order to provide the required edge profiles after etching.

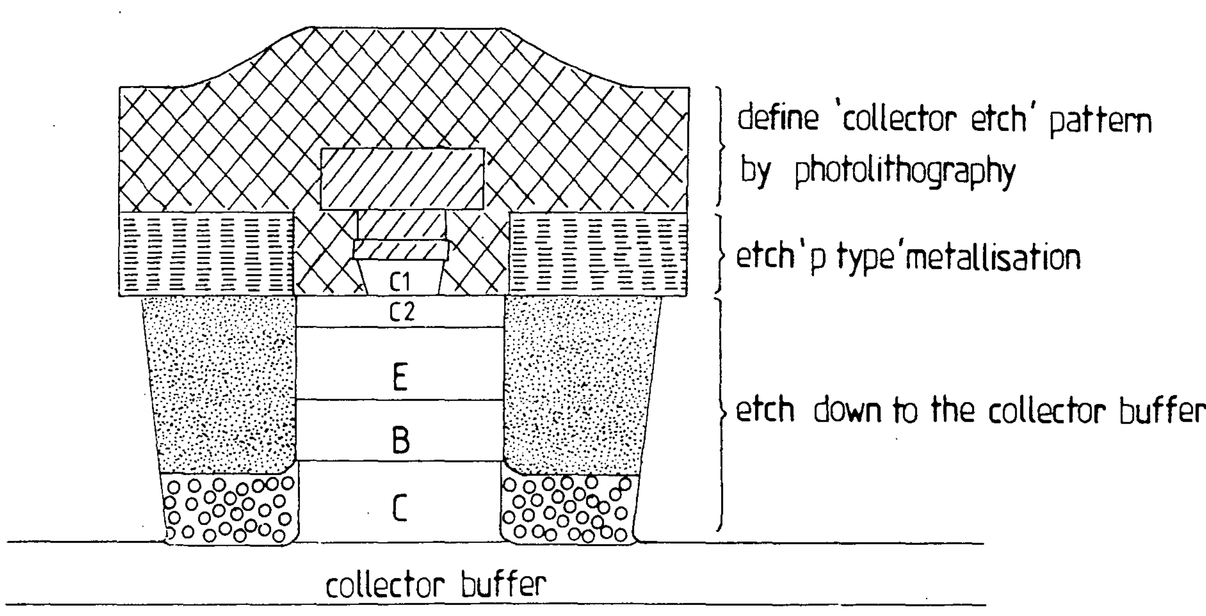
3.5.0: Proton (H^+) implanation in the extrinsic collector

The extrinsic base-collector capacitance (originating from the junction of the p^+ base implant and the collector epilayer) can have a significant effect in slowing the device performance. To overcome the problem, protons (H^+) are introduced by implantation from the surface into the low doped collector region below the extrinsic base. Proton-implanted GaAs remains compensated even after high temperature anneal. The proton implant creates semi-insulating regions which, if sufficiently wide, decrease the base-collector capacitance dramatically. The same photoresist pattern used to define the emitter T-shaped

FIGURE 3.4.0



c)(i)Metallise the base contact regions;(ii)Remove photoresist.



d)(i)Define 'collector etch' pattern by photolithography;(ii)Etch 'p type' metal to to define the base contact pads;(iii)Etch down to the collector buffer.

contact structures is used as a mask to the proton implantation, the Be implantation and the base metallisation.

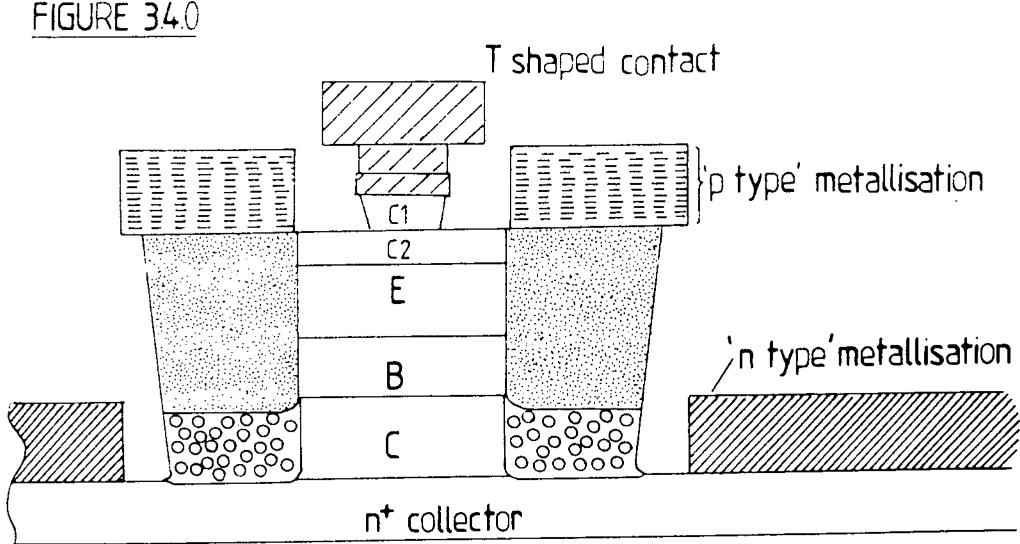
3.6.0: Beryllium implantation to the base layer

Beryllium ions are implanted to the bottom of the base layer so as to provide a deep region of heavily doped p type material underneath the base contact (figures 3.4.0 (b), (c) and (d)) thus increase the chances of good ohmic contact to the base layer. This is readily seen from equation A4.6 which shows that minimum values of contact resistance are strongly dependent on low value of sheet resistance of semiconductor layer under the contact pad.

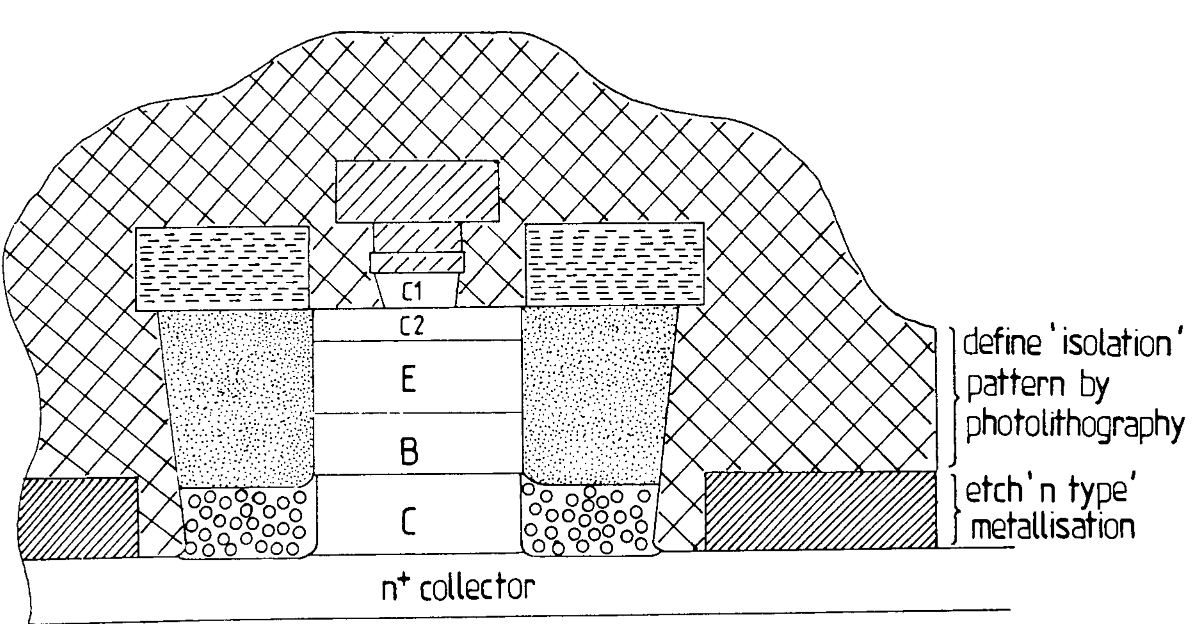
$$R_C = \frac{R_{Sk} L_T}{W} \coth (d/L_T) \qquad \text{Eqn 4.6.0}$$

As Be is the lightest p type dopant in GaAs [101], the lattice disorder produced by implantation is significantly less than for heavier ions. Consequently, the electrical activation of implanted Be can be obtained with anneal temperatures as low as 500°C [101,102] although post implantation annealing has generally been carried out using a conventional furnace anneal between 700°C and 900°C. The implantation of Be down to the base layer is achieved using the same conditions as for the conventional process. With a view to minimising the number of process steps in the fabrication of self-aligned devices, efforts concentrated on post-implantation annealing of Be at 750°C since that temperature was chosen for heat treating the refractory metals. The doping concentration achieved in the base contact regions was 1×10^{19} cm^{-3} .

FIGURE 3.4.0



e)(i)Metallise the collector;(ii)Remove photoresist.



f)(i) Define 'isolation' pattern by photolithography;(ii)Etch 'n type' metallisation to define collector contact pads.

3.7.0: Metallisation to the p type base

The contact metallisation to the base was deposited on the heavily doped Be-implanted regions (figure 3.4.0(c)). The same metallisation system of Au(200Å)/Zn(600Å)/Au(2000Å) used for the conventional process was selected for the self-aligned process since the value of specific contact resistance produced by alloying at 750°C for 30 mins (Table 3.3.1) was close to the previous value obtained using RTA. It is important to note that the metals cannot be deposited by sputtering in this case because directional deposition is required. Thermal evaporation was used.

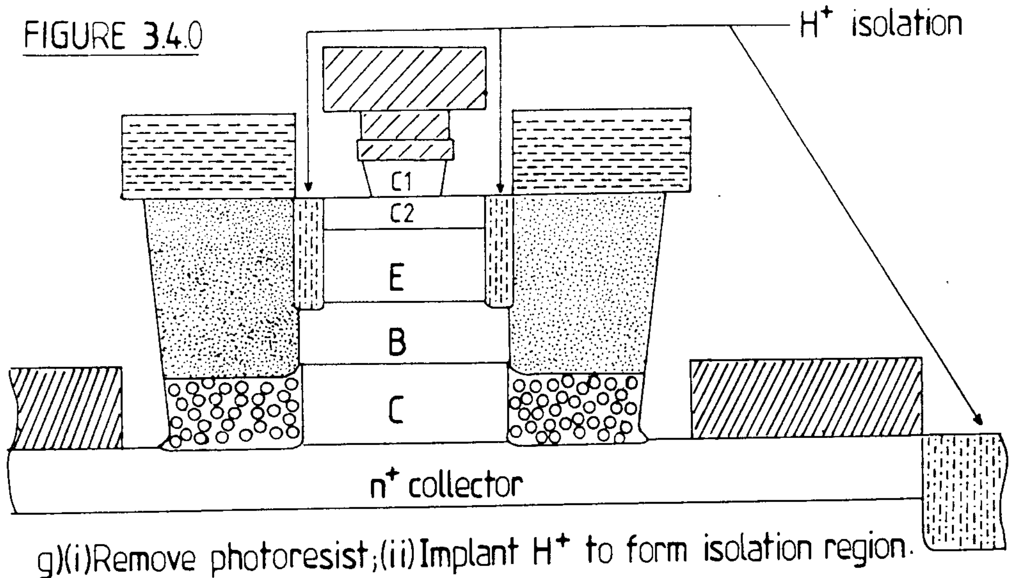
3.8.0: Ion beam milling to define the p type contact pad

After metallisation of the heavily doped Be-implanted regions, the photoresist mask was removed and the samples thoroughly cleaned. The contact pads to the base were then defined by photolithography (figure 3.4.0(d)), followed by ion beam milling of the metals until the semiconductor was reached.

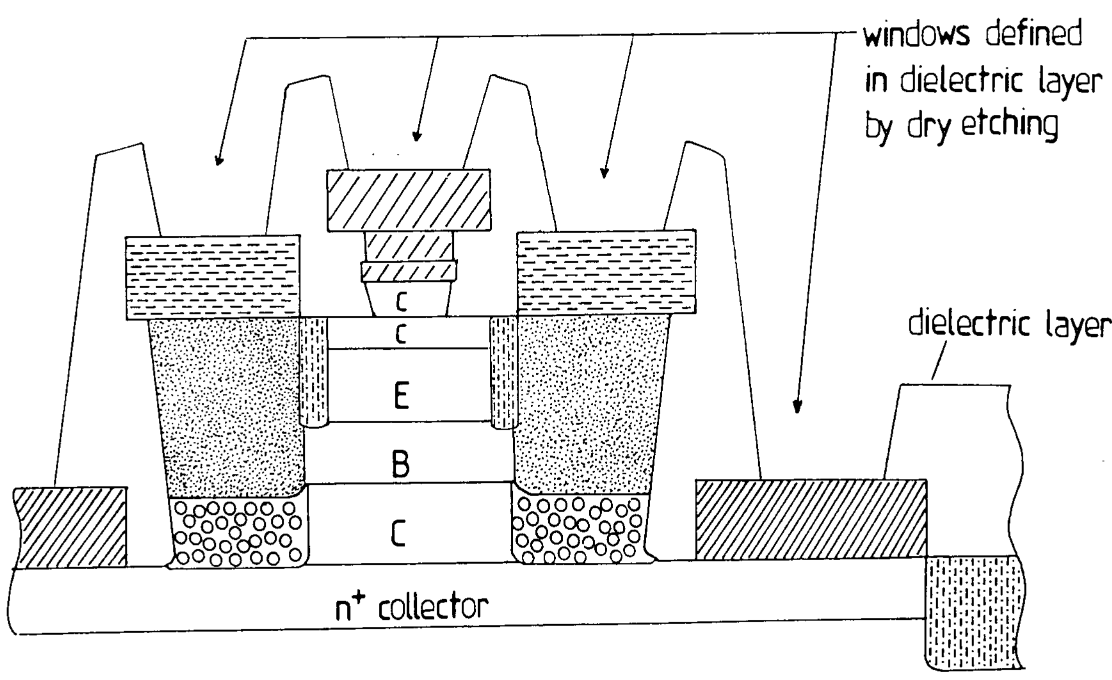
3.9.0: Wet chemical etching to the collector

Using the same photoresist mask as for the definition of the base contact pads, wet etching was performed down to the collector contact layer (also known as collector buffer). It was important to use the photoresist as a mask since it prevented etching from occuring in the small separation between p and n type metallisations (figure 3.4.0 (c)). As was the case with the etching of cap 1, the etchant must be chosen with the aim to provide the required slopes of the semiconductor to accommodate subsequent processing.

FIGURE 3.4.0



g)(i)Remove photoresist;(ii)Implant H^+ to form isolation region.



h)(i)Deposit dielectric layer;(ii)Define dielectric windows by photolithography followed by dry etching.

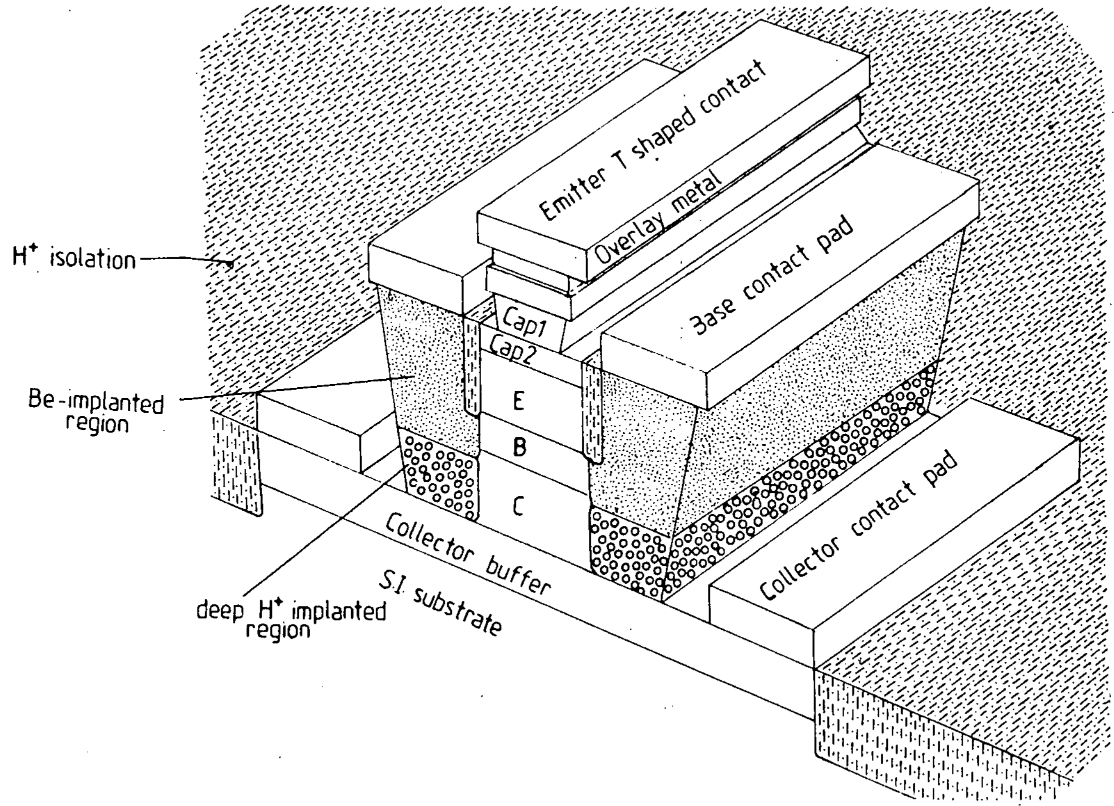


FIGURE 3.4.0(i): 3 dimensional view of SAHBT with T shaped emitter contact.

3.10.0: Metallisation to the n type collector

For the collector, metallisation schemes were as used in the fabrication of conventional devices. The metals were deposited by e-beam evaporation (figure 3.4.0 (d) & (e)).

3.11.0: Definition of collector contact pads

After metallisation of the collector, the masking layer of photoresist is lifted off and the sample is thoroughly cleaned. The collector contact pads are then defined by photolithography followed by ion beam milling of the metal layers (figure 3.4.0 (f)).

3.12.0: Heat treatment for optimum contact resistance

After the definition of the collector contact pads, the metallisation systems to the emitter, base and collector (and the implantation region for the extrinsic base) are subjected to a furnace anneal (750°C for 30 mins in a nitrogen atmosphere) in order to obtain best possible values of contact resistances. The above mentioned conditions were chosen because they provided the best results for the refractory metals (1.9×10^{-6} ohm-cm^2) used for the emitter, while the values of specific contact resistance for the base (1.2×10^{-6} ohm-cm^2) and collector (8.6×10^{-6} ohm-cm^2) only deteriorated very slightly in comparison to their optimum values previously obtained with RTA at 450°C for 40s. The alloyed metal contacts to the emitter, base and collector were then analysed by AES and the results are shown in figures 3.5.0 (a) and (b) for the base contacts and figures 3.5.0 (e) and (f) for the collector contacts. A typical plot of transmission line model results for assessment of contact resistance is shown

[SELF ALIGNED PROCESS]

TABLE 3.3.1 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Ti : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	Best values $9.8 - 9.9 \times 10^{-3}$ (40mins)
Au : 2000 Zn : 700 Ti : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$9.5 - 9.75 \times 10^{-3}$ (40mins)
Au : 2000 Zn : 600 Ti : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$9.4 - 9.7 \times 10^{-3}$ (40mins)
Au : 2000 Zn : 500 Ti : 200 GaAs substrate	FA 650° for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$9.4 - 9.5 \times 10^{-3}$ (40mins)

TABLE 3.3.1 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Ti : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	Best values $5.8 - 6.1 \times 10^{-4}$ (40mins)
Au : 2000 Zn : 700 Ti : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$5.5 - 5.9 \times 10^{-4}$ (40mins)
Au : 2000 Zn : 600 Ti : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$5.6 - 5.7 \times 10^{-4}$ (40mins)
Au : 2000 Zn : 500 Ti : 200 GaAs substrate	FA 750° for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$5.2 - 5.7 \times 10^{-4}$ (40mins)

TABLE 3.3.1 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Cr : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	Best values $6.45 - 6.9 \times 10^{-4}$ (40mins)
Au : 2000 Zn : 700 Cr : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$4.8 - 5.5 \times 10^{-4}$ (40mins)
Au : 2000 Zn : 600 Cr : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$4.8 - 5.1 \times 10^{-4}$ (40mins)
Au : 2000 Zn : 500 Cr : 200 GaAs substrate	FA 650° for 10 / 20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$4.1 - 4.3 \times 10^{-4}$ (40mins)

TABLE 3.3.1 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Cr : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	Best values $8.7 - 9.1 \times 10^{-5}$ (40 mins)
Au : 2000 Zn : 700 Cr : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$8.7 - 9.25 \times 10^{-5}$ (40 mins)
Au : 2000 Zn : 600 Cr : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$8.6 - 9.1 \times 10^{-5}$ (40 mins)
Au : 2000 Zn : 500 Cr : 200 GaAs substrate	FA 750° for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$8.1 - 8.8 \times 10^{-5}$ (40 mins)

TABLE 3.3.1 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals/Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE (Ω cm^2)
Au : 2000 Zn : 800 Au : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	p = 3×10^{18}	Best values 1.5 - 1.75 x 10^{-5} (40mins)
Au : 2000 Zn : 700 Au : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	p = 3×10^{18}	1.5 - 1.8 x 10^{-5} (40mins)
Au : 2000 Zn : 600 Au : 200 GaAs substrate	FA 650°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	p = 3×10^{18}	1.5 - 2.3 x 10^{-5} (40mins)
Au : 2000 Zn : 500 Au : 200 GaAs substrate	FA 650° for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	p = 3×10^{18}	1.4 - 1.6 x 10^{-5} (40mins)

TABLE 3.3.1 :Contact resistance results for p-type GaAs

CONTACT STRUCTURE Metals / Thickness (Å)	HEAT TREATMENT Temp. / Time / Ambient gas / Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\ cm^2$)
Au : 2000 Zn : 800 Au : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	Best values $1.2 - 1.5 \times 10^{-6}$ (40mins)
Au : 2000 Zn : 700 Au : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$1.2 - 1.5 \times 10^{-6}$ (40mins)
Au : 2000 Zn : 600 Au : 200 GaAs substrate	FA 750°C for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$1.2 - 1.5 \times 10^{-6}$ (30mins)
Au : 2000 Zn : 500 Au : 200 GaAs substrate	FA 750° for 10 /20 /30 /40 mins in a N_2 atmosphere (High temperature process furnace)	$p = 3 \times 10^{18}$	$1.2 - 1.4 \times 10^{-6}$ (40mins)

TABLE 3.3.1 : Contact resistance results to n-type GaAs

CONTACT STRUCTURE Metals/ Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE ($\Omega\,cm^2$) Best values
Au : 2000 Ni : 400 AuGe : 600 Ni : 50 GaAs substrate	FA 650°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature.process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$3.7 - 3.9 \times 10^{-4}$ (40mins) $6.1 - 7.3 \times 10^{-4}$ (40mins)
Au : 2000 Ni : 300 AuGe : 600 Ni : 50 GaAs substrate	FA 650°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$7.4 - 8.5 \times 10^{-5}$ (40mins) $9.0 - 9.7 \times 10^{-5}$ (40mins)
Au : 2000 Ni : 200 AuGe : 600 Ni : 50 GaAs substrate	FA 650°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$6.0 - 7.2 \times 10^{-5}$ (40mins) $6.6 - 7.1 \times 10^{-5}$ (40mins)
Au : 2000 Ni : 100 AuGe : 600 Ni : 50 GaAs substrate	FA 650°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	non-ohmic non-ohmic

TABLE 3.3.1 : Contact resistance results to n-type GaAs

CONTACT STRUCTURE Metals/ Thickness (Å)	HEAT TREATMENT Temp./Time/Ambient gas/ Furnace type	Semiconductor doping (cm^{-3})	SPECIFIC CONTACT RESISTANCE (Ωcm^2) Best values
Au : 2000 Ni : 400 AuGe : 600 Ni : 50 GaAs substrate	FA 750°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$1.25 - 3.4 \times 10^{-5}$ (30mins) $8.6 - 9.3 \times 10^{-5}$ (30mins)
Au : 2000 Ni : 300 AuGe : 600 Ni : 50 GaAs substrate	FA 750°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$5.75 - 8.2 \times 10^{-6}$ (30mins) $2.5 - 6.7 \times 10^{-5}$ (30mins)
Au : 2000 Ni : 200 AuGe : 600 Ni : 50 GaAs substrate	FA 750°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	$2.1 - 2.4 \times 10^{-6}$ (30mins) $8.6 - 8.8 \times 10^{-6}$ (30mins)
Au : 2000 Ni : 100 AuGe : 600 Ni : 50	FA 750°C for 10/20/30/40 mins in a N_2 atmosphere (High temperature process furnace)	$n = 2 \times 10^{18}$ $n = 1 \times 10^{18}$	non-ohmic non-ohmic

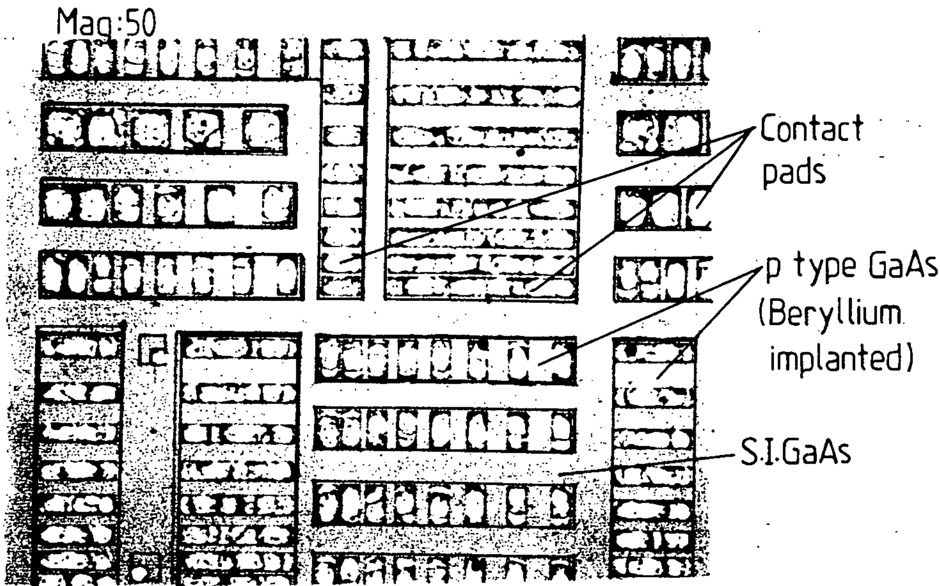


FIGURE 3.5.0(a): Top view of TLMs for assessment of contact resistance. Contact pads consist of Au(2000Å)/Zn(600Å)/Au(200Å)/GaAs alloyed at 750°C for 30 mins.

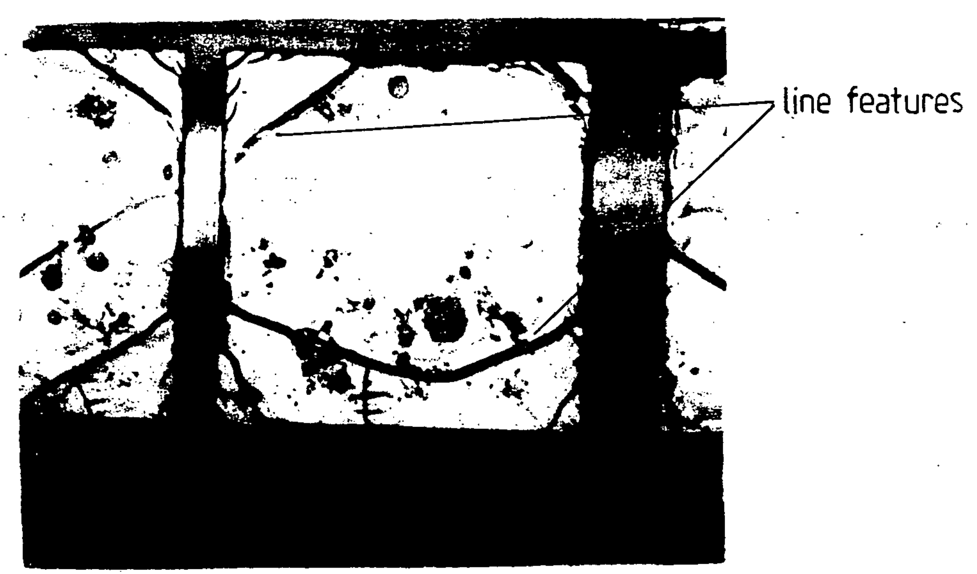
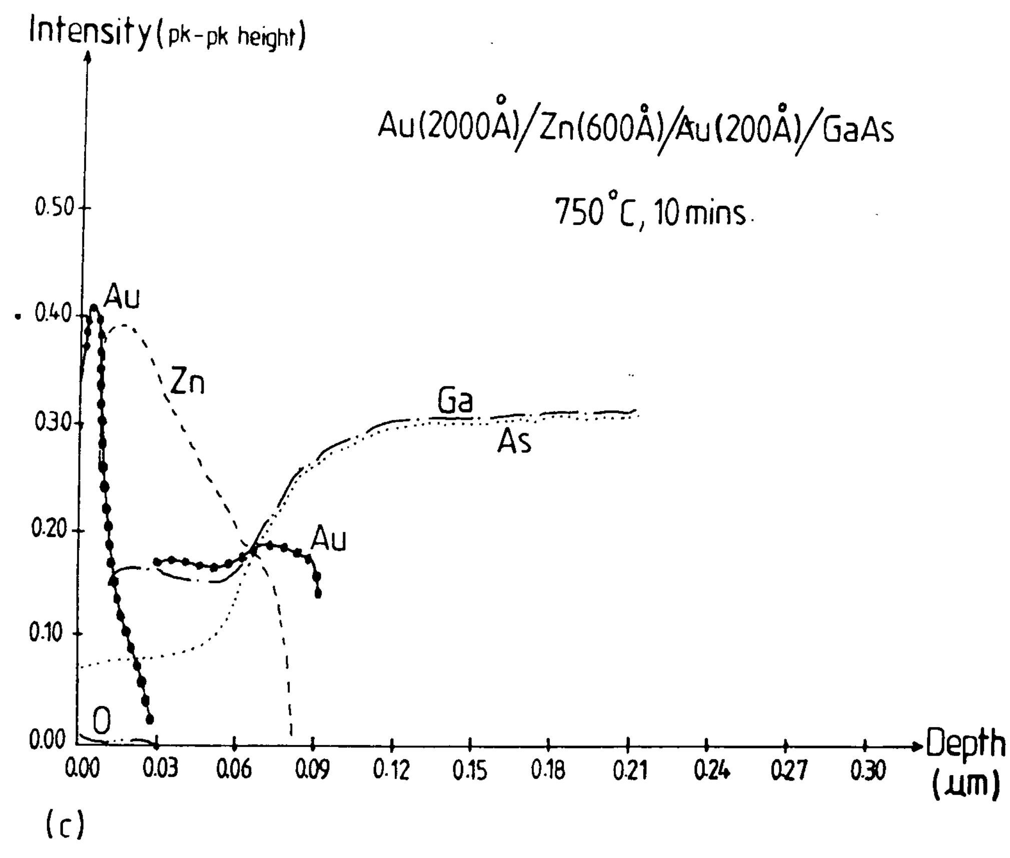


FIGURE 3.5.0(b): Close up on TLMs pictured in (a) above shows dark line features on the contact pads.



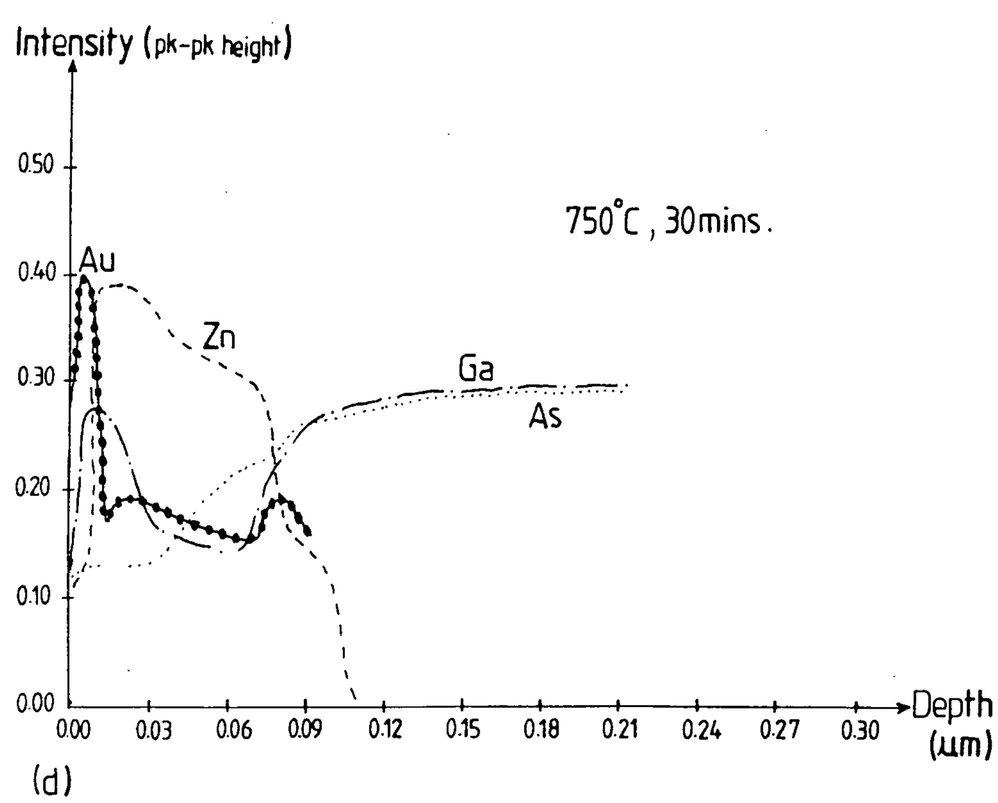


FIGURE 3.5.0 :Auger Electron Spectroscopy profiles

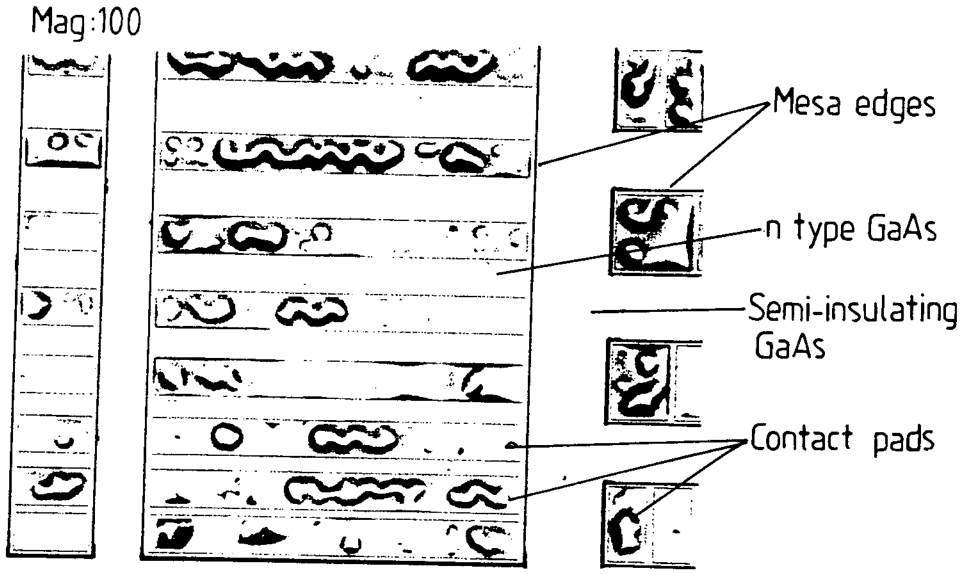


FIGURE 3.5.0(e): Top view of TLMs for assessment of contact resistance. Contact pads consist of Au(2000Å)/Ni(200Å)/AuGe(600Å)/Ni(50Å)/GaAs alloyed at 750°C for 30mins using FA.

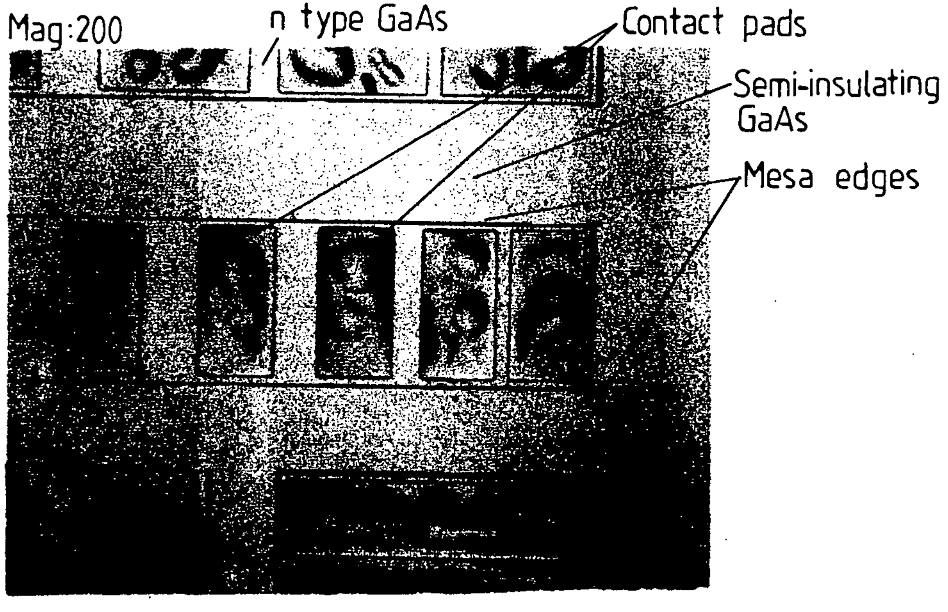
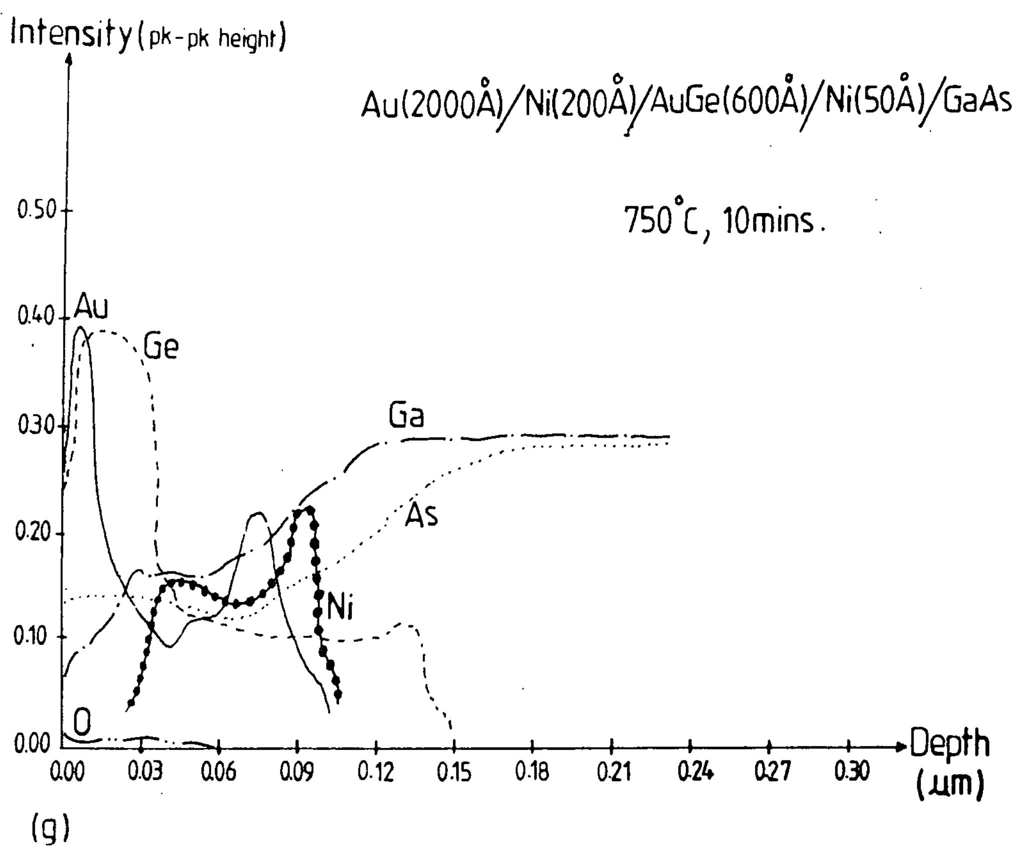


FIGURE 3.5.0(f): Close up on TLMs pictured in (e) above shows uneven surface of alloyed contacts.



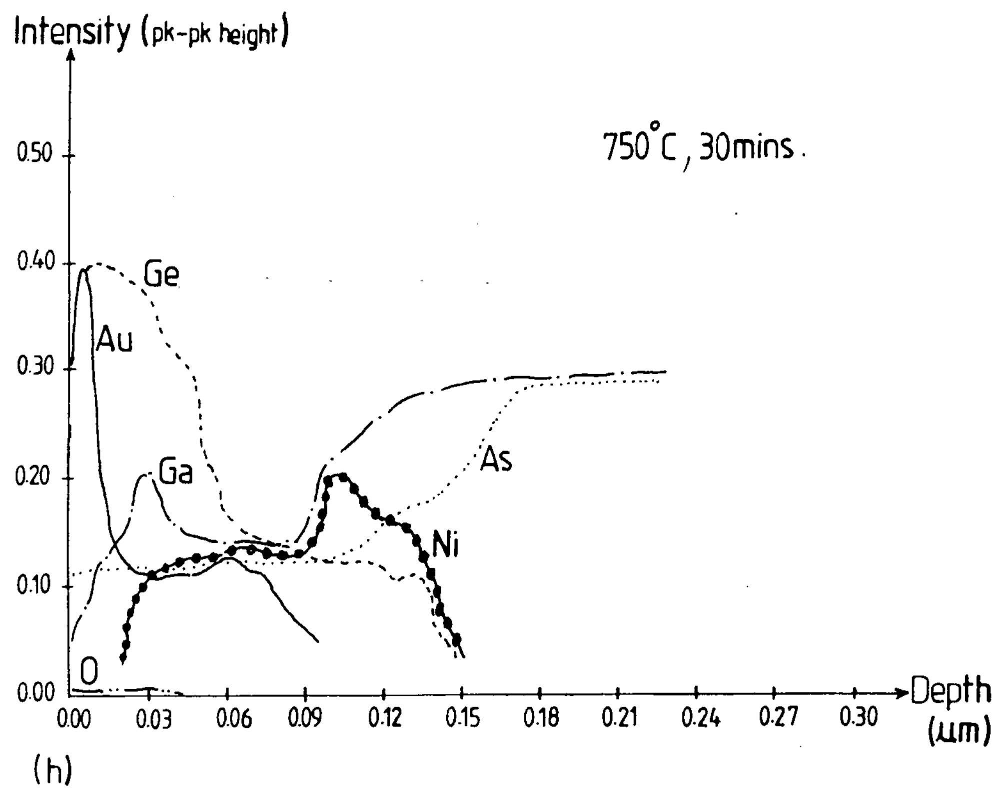


FIGURE 3.5.0 :Auger Electron Spectroscopy profiles

in figure 3.2.3 . Values of contact resistance R_C and transfer length L_T can be obtained directly from the plot while the specific contact resistance ρ_C can be calculated from values obtained with the plot. A full description of the TLM method is given in appendix A4.

3.13.0: Proton bombardment for isolation

In previous fabrication techniques, isolation was achieved by etching the material around the devices down to semi-insulating substrate. Because of the possible non-uniformity usually associated with wet etching, proton (H^+) bombardment was used to electrically isolate the devices. The emitter and base contact pads acted as a mask and thus enabled the lateral diode created during Be implantation to be destroyed (figure 3.4.0 (g)).

3.14.0: Performance of self-aligned 8µm HBT

The frequency response of an 8µm self-aligned HBT is shown in figure 3.7.0. Best value obtained for the transition frequency f_t was 10.7GHz and for the maximum oscillation frequency f_{max} was 9.8 GHz, thus demonstrating a net improvement over the performance of conventional devices.

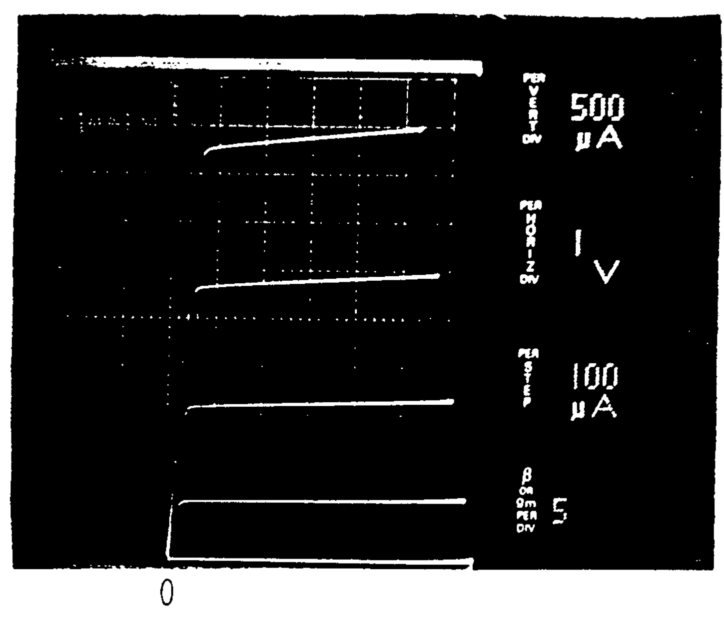
3.15.0: Other processing considerations

3.15.1: Zinc diffusion for base contacts

As an alternative to Be-implantation to create a heavily doped p type region to host the metallisation of the base, zinc diffusion by the `sealed tube method´ (appendix A11) was considered. The latter could be incorporated as part of the

Emitter design dimensions : $8\,\mu m \times 16\,\mu m$.

Emitter effective dimensions : $\sim 6.8\,\mu m \times 15\,\mu m$.



$\beta = 10 - 15$

$V_t = 0.2V$

$V_{br} = 8.0V$

$J_c = 1.6 \times 10^{-4}\ A/cm^2$

FIGURE 3.6.0 : Measured I-V characteristics for an 8 µm SAHBT.

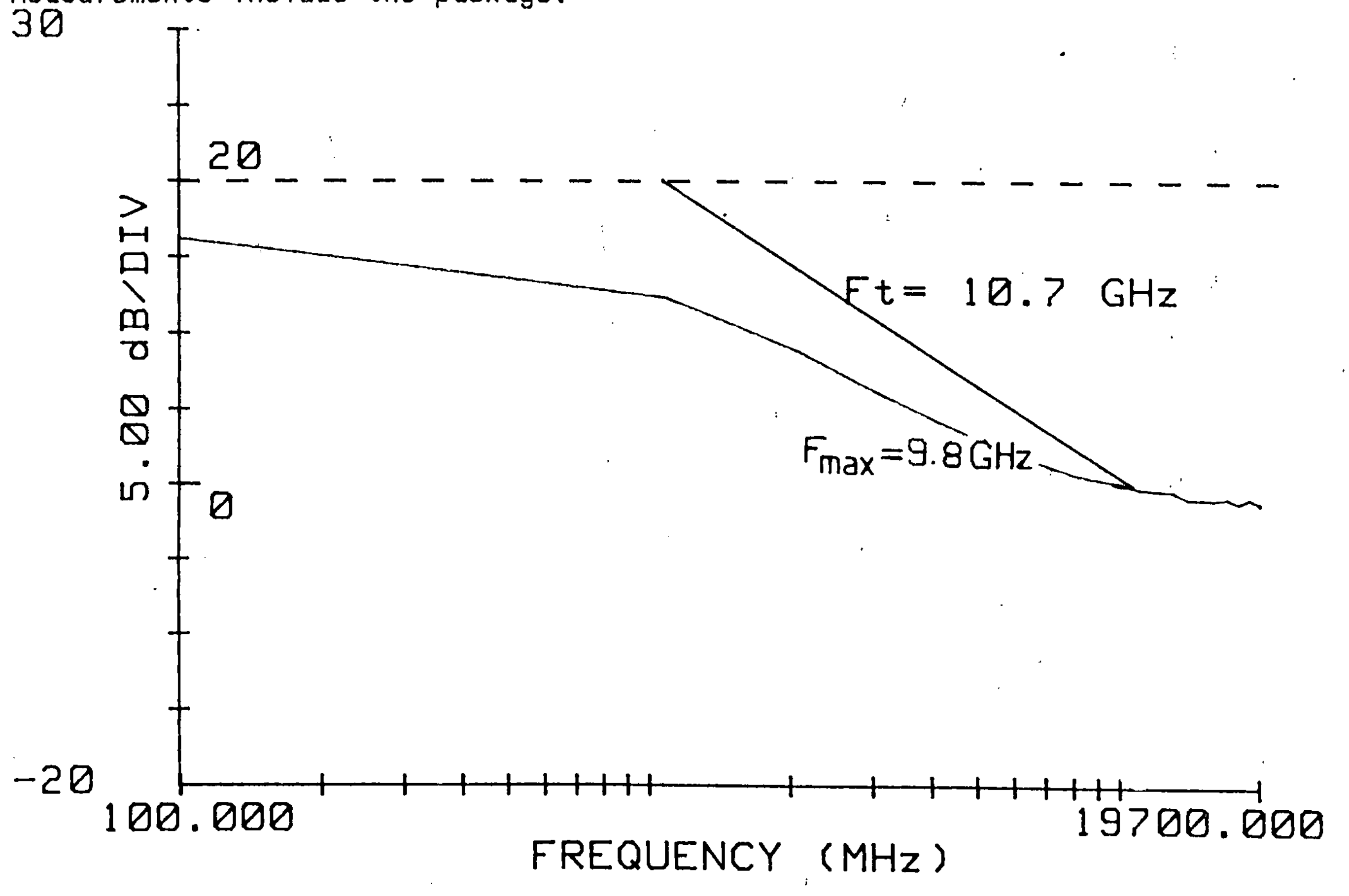


FIGURE 3.7.0: Current gain v/s frequency for a packaged 8 um SAHBT.

fabrication process for HBTs via the suggested process route described by figures 3.10.0 - 3.12.0 . A surface concentration of 1×10^{20} cm^{-3} was achieved using this technique. Hall and Stripe measurements performed on semi-insulating GaAs with zinc diffusion carried out at 750°C for 30 mins under arsenic overpressure gave the results shown in figures 3.8.0 and 3.9.0. Metallisation systems used for Be-implantation were deposited on zinc-diffused GaAs substrates amd TLMs were defined and contact resistance was assessed as before. For the same metallisation scheme of Au(2000A)/Zn(600A)/Au(200A)/GaAs, alloying at 450°C for 40s gave a specific contact resistance of 1.1×10^{-6} ohm-cm^2 while alloying at 750°C for 30 mins gave a specific contact resistance of 8.1×10^{-7} ohm-cm^2 . Although zinc diffusion is a very attractive technique for contacting the base layer because of the high doping concentration possible, it cannot be used as a self-aligned process because it is isotropic.

3.15.2: Air bridges for interconnecting devices or for bonding pads.

One of the main problems associated with interconnects between devices in the conventional process is that of the high capacitance due to the dielectric material (polyimide or silicon nitride) used to isolate one metal layer from the other.

Air-bridge structures use air as a dielectric and thus enable the parasitic capacitances to be reduced to a minimum. Experimental work concentrated on fabrication of such structures on dummy samples with mesa structures similar to the transistor structures already defined on the surface. Figures 3.14.0 (a) to

(f) show how such structures can be used in the fabrication of SAHBTs. The complexity of circuits will determine whether these should be used for bonding pads or for interconnects or for both. One disadvantage of the air-bridge structure is the relatively large number of process steps used in its fabrication.

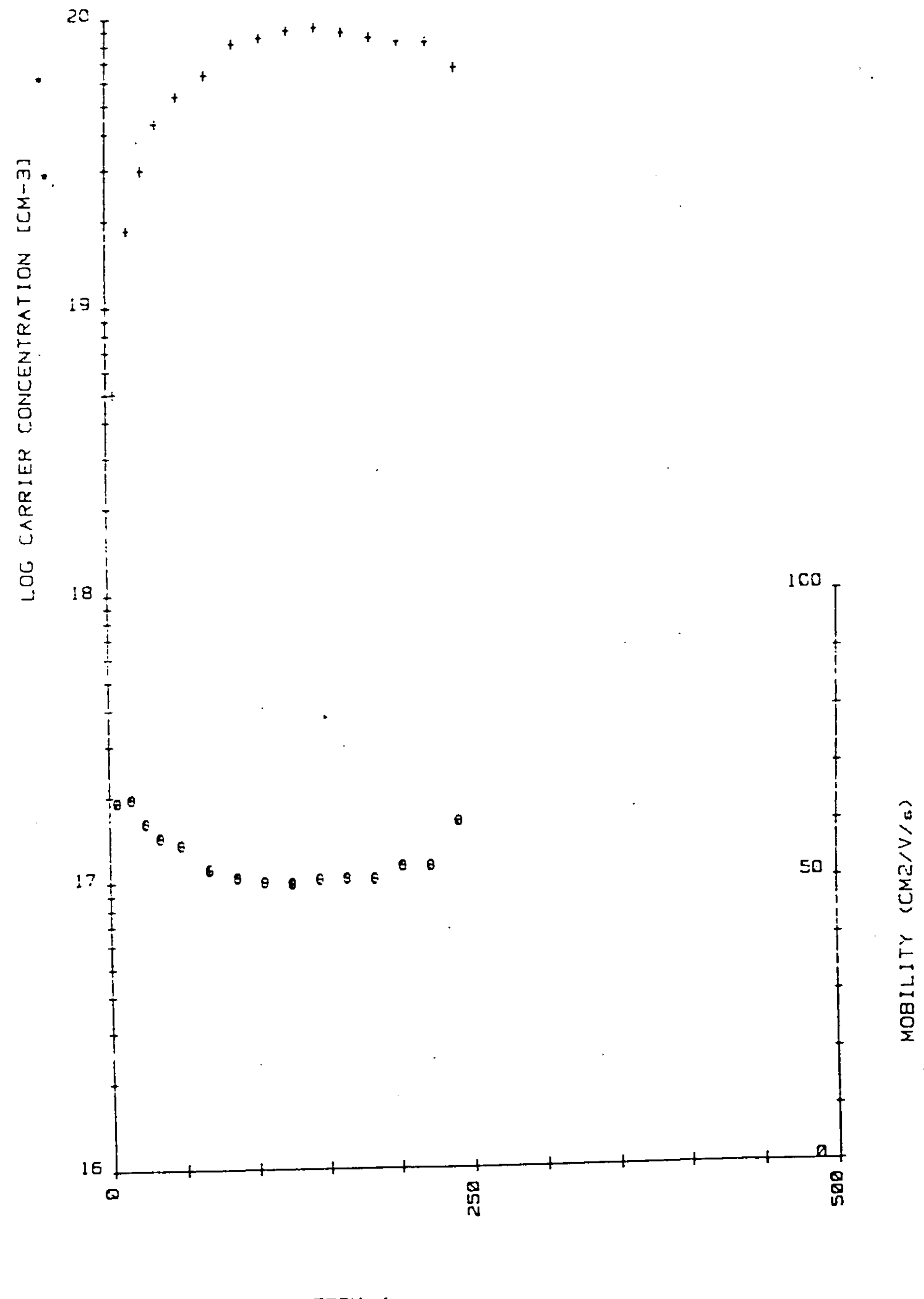


FIGURE 3.8.0: Hall measurements of log carrier concentration v/s depth for semi-insulating GaAs with zinc diffusion performed at 750°C for 30 mins under arsenic overpressurre.

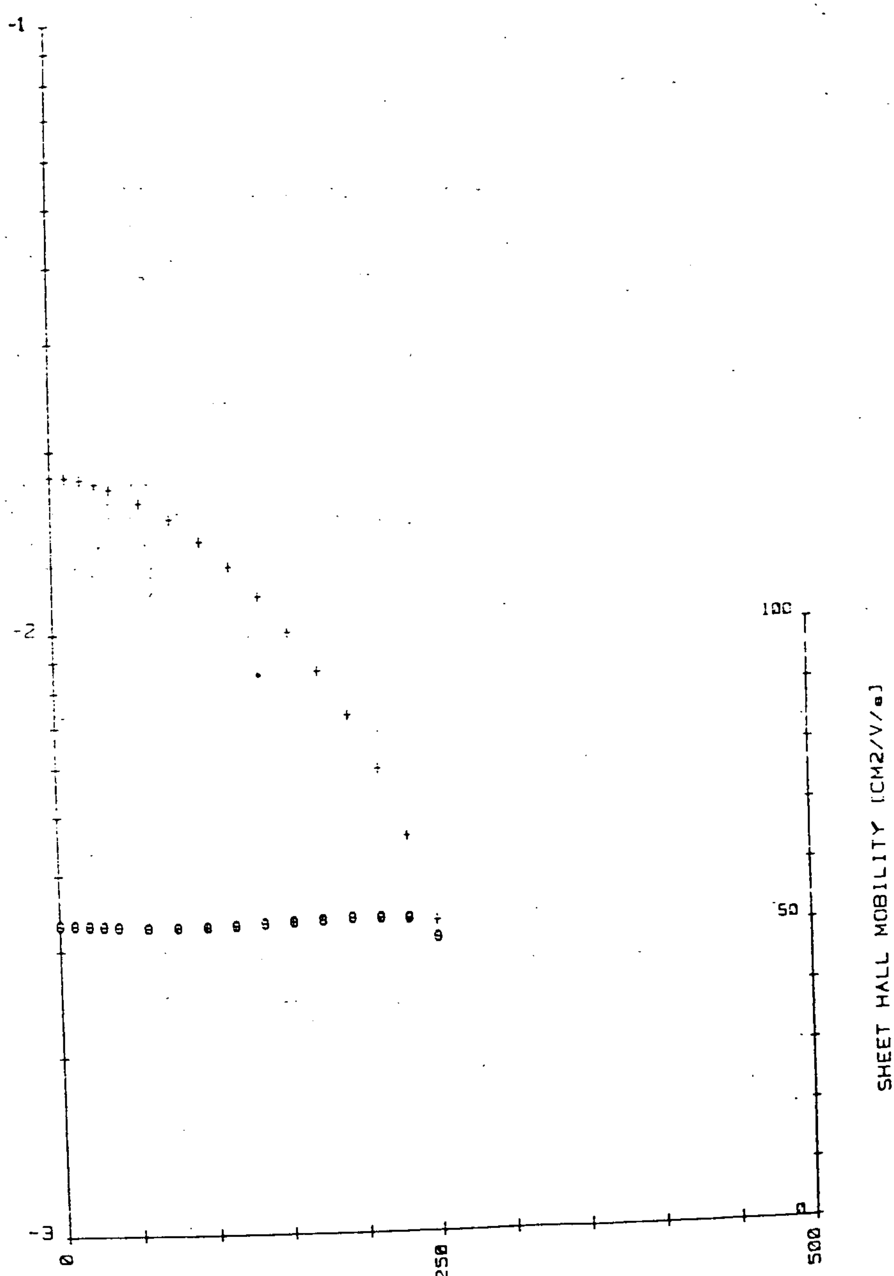


FIGURE 3.9.0 : Hall measurements of conductivity and sheet mobility v/s depth for semi-insulating GaAs with zinc diffusion performed at 750°C for 30 mins under arsenic overpressure.

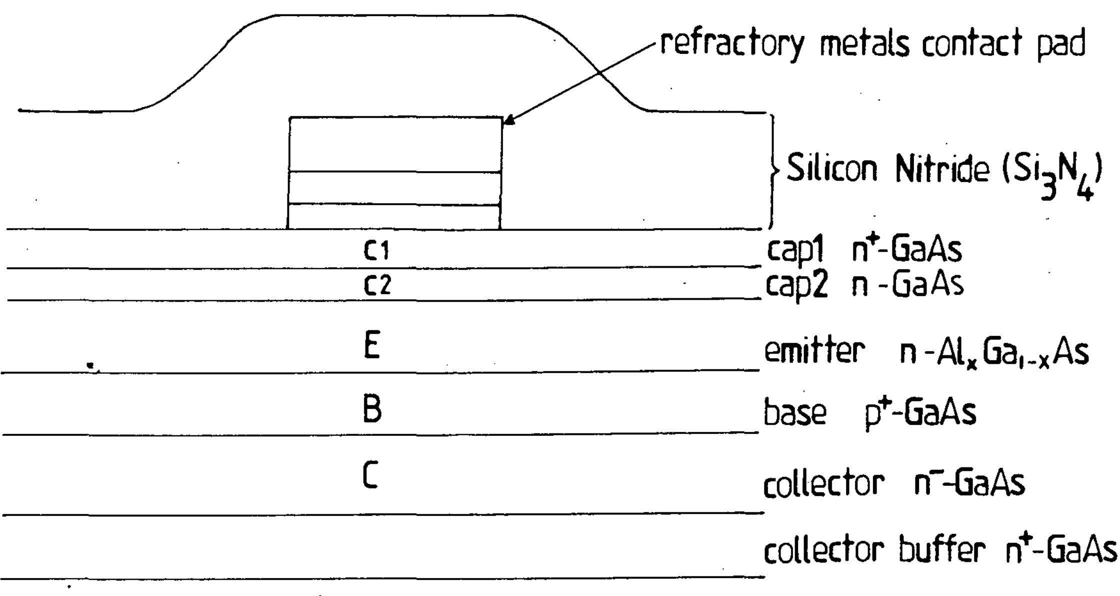


FIGURE 3.10.0 :(i)Deposit refractory metals; (ii)Define contact pad; (iii)Deposit silicon nitride.

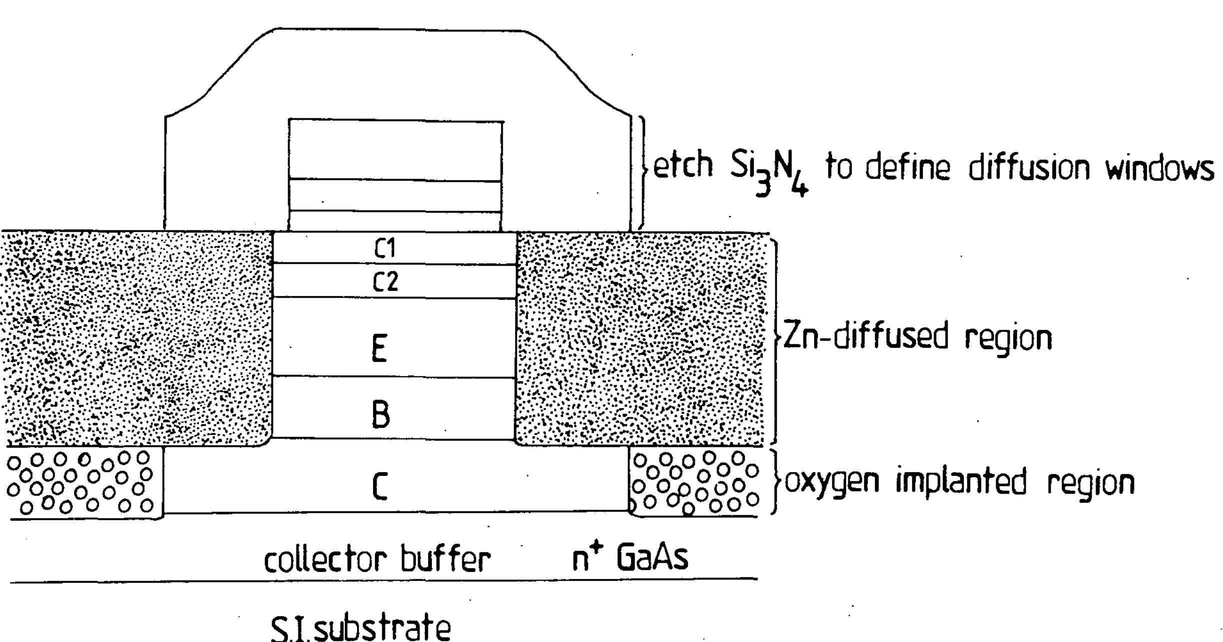


FIGURE 3.11.0 :(i)Define diffusion windows; (ii)Implant oxygen in the extrinsic collector region; (iii)Diffuse zinc to the base-collector interface.

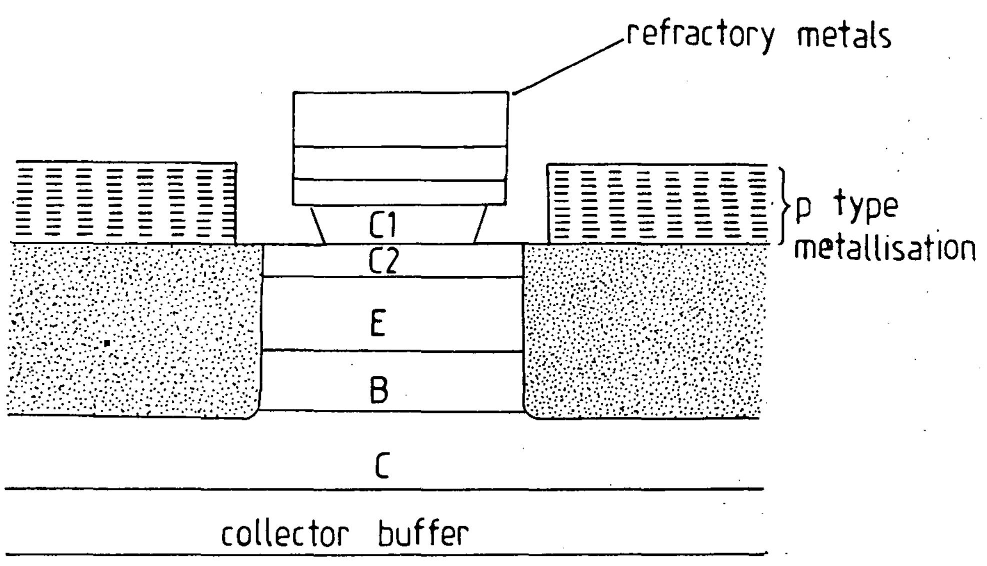


FIGURE 3.12.0 : (i)Remove Si_3N_4 ; (ii)Define pattern for base metal after etching Cap1 ; (iii)Metallise the base.

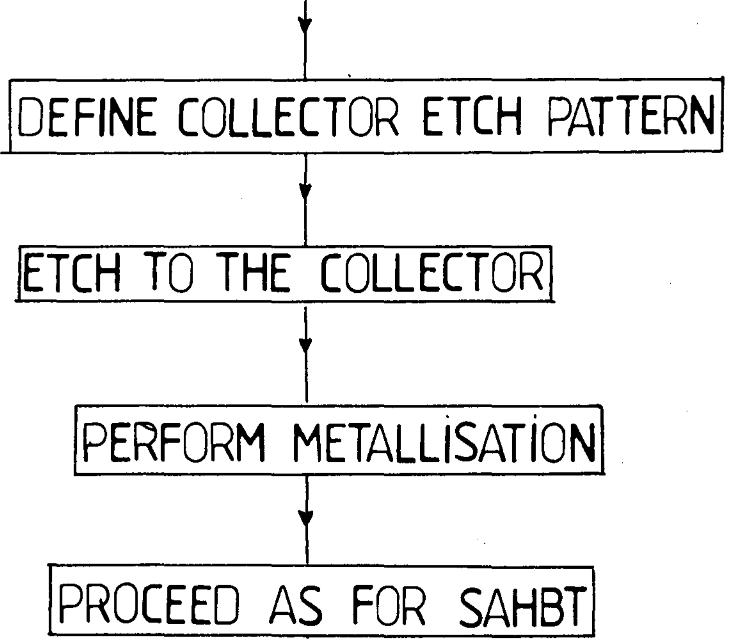


FIGURE 3.14.0: Fabrication of an 'air-bridge' structure for 'interconnecting' devices or for 'bonding pads'.

(a) CROSS SECTIONAL SCHEMATIC DRAWING.

- n-type refractory metallisation
- p-type metallisation
- p-type implantation
- H^+ isolation
- n type metallisation
- interconnect metallisation
- dielectric layer

Clean wafer surface

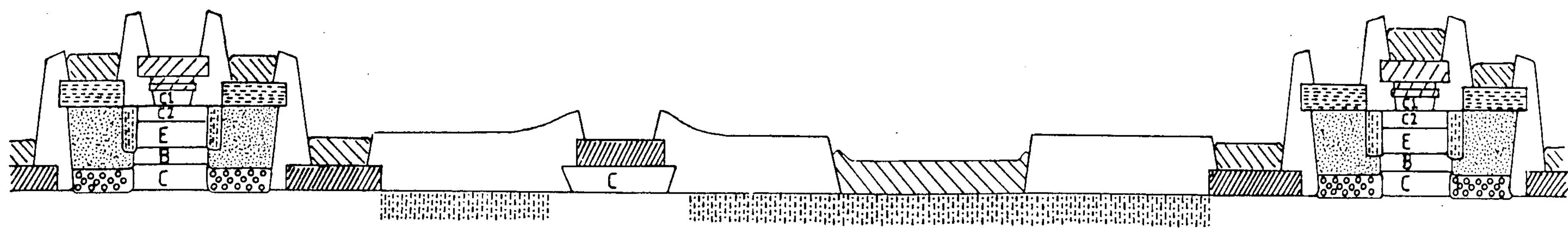


FIGURE 3.14.0: Fabrication of an 'air-bridge' structure for 'interconnecting' devices or for 'bonding pads'.

(i) DEFINE "AIR BRIDGE PROTECT WINDOWS" BY PHOTOLITHOGRAPHY;
(ii) METALLISE WITH TITANIUM/GOLD/TITANIUM;

(b)

- n-type refractory metallisation
- p-type metallisation
- p-type implantation
- H^+ isolation
- n type metallisation
- interconnect metallisation
- dielectric layer
- deep H^+ implantation

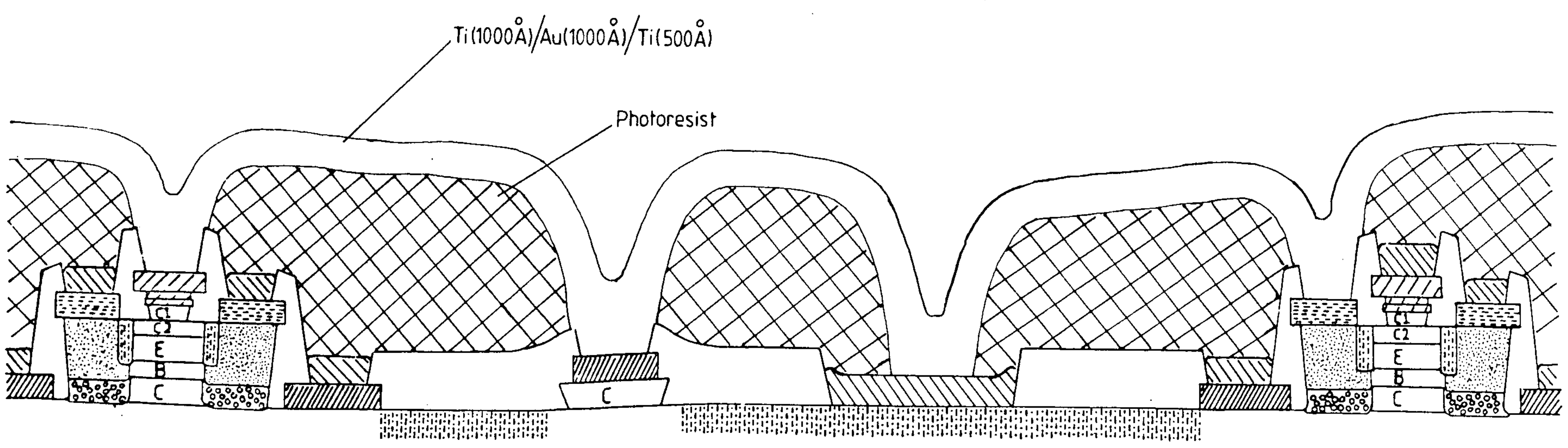


FIGURE 3.14.0: Fabrication of an 'air-bridge' structure for 'interconnecting' devices or for 'bonding pads'.

(iii) DEFINE "PLATING WINDOWS" BY PHOTOLITHOGRAPHY;

(iv) ETCH TITANIUM IN 10% HF;

(v) PLATE TO APPROXIMATELY 5 µm;

(c)

- n-type refractory metallisation
- p-type metallisation
- p-type implantation
- H^+ isolation
- n type metallisation
- interconnect metallisation
- dielectric layer

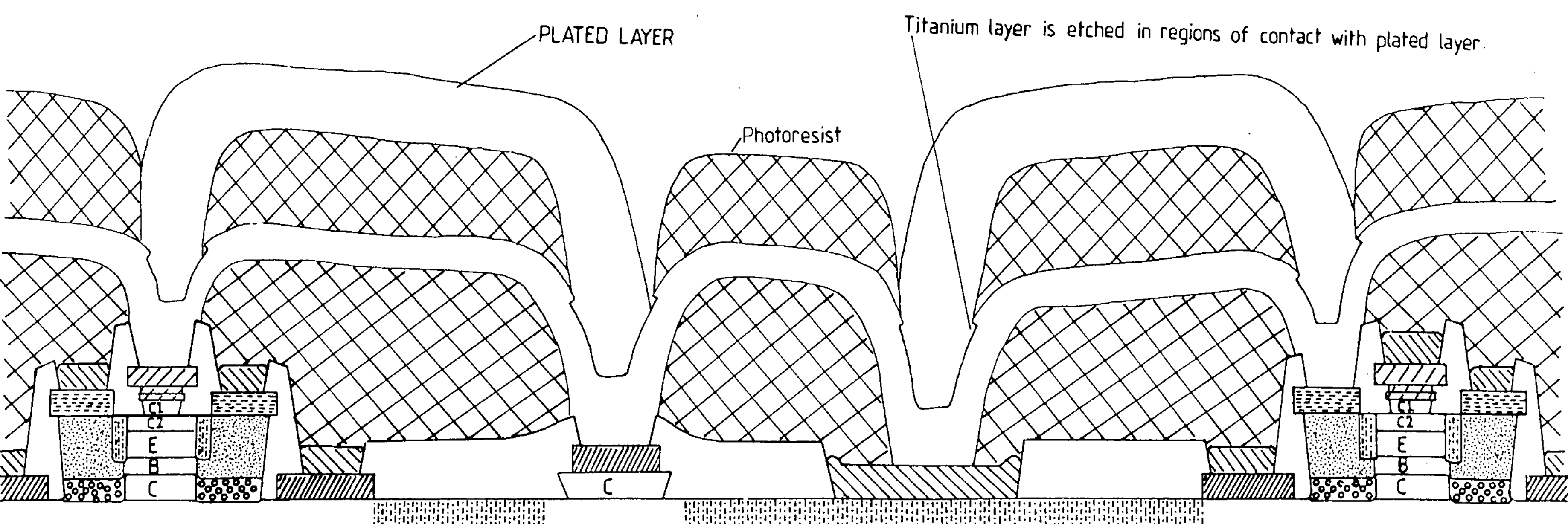


FIGURE 3.14.0: Fabrication of an 'air-bridge' structure for 'interconnecting' devices or for 'bonding pads'.

(vii) ETCH TITANIUM IN 10% HF, GOLD IN OROSTRIP, AND TITANIUM IN 10% HF.

(e)

- n-type refractory metallisation
- p-type metallisation
- p-type implantation
- H^+ isolation
- n type metallisation
- interconnect metallisation
- dielectric layer
- deep H^+ implantation

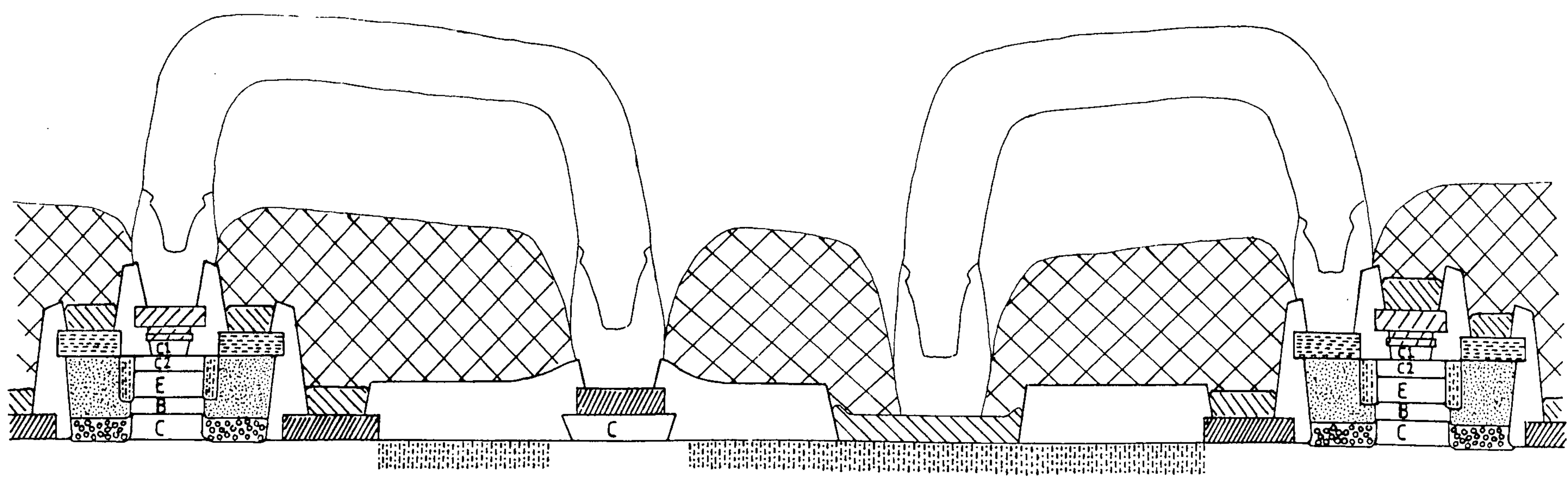


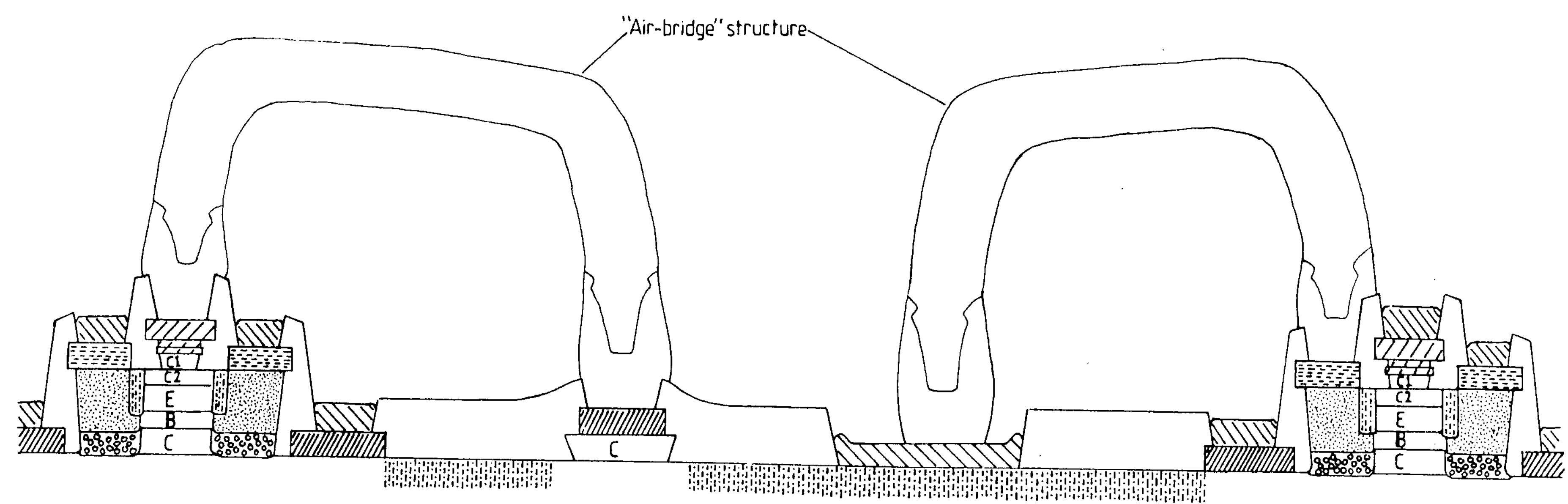
FIGURE 3.14.0: Fabrication of an 'air-bridge' structure for 'interconnecting' devices or for 'bonding pads'.

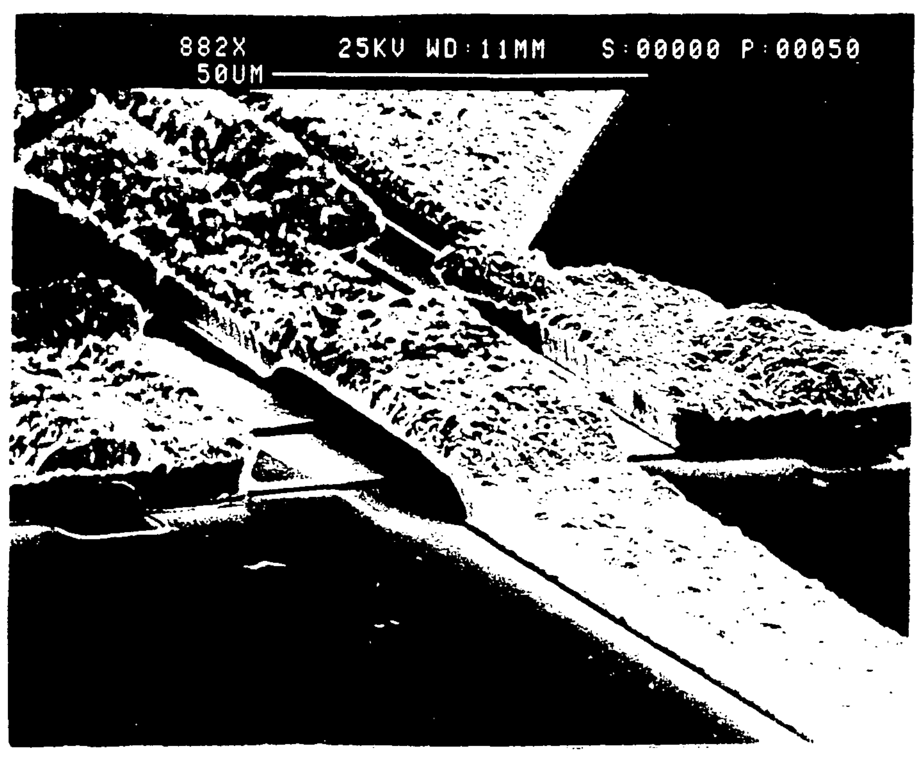
(viii) FLOOD EXPOSE AND DEVELOP;

(ix) SOLVENT CLEAN.

(f)

- n-type refractory metallisation
- p-type metallisation
- p-type implantation
- H^+ isolation
- n type metallisation
- interconnect metallisation
- dielectric layer
- H^+ implantation





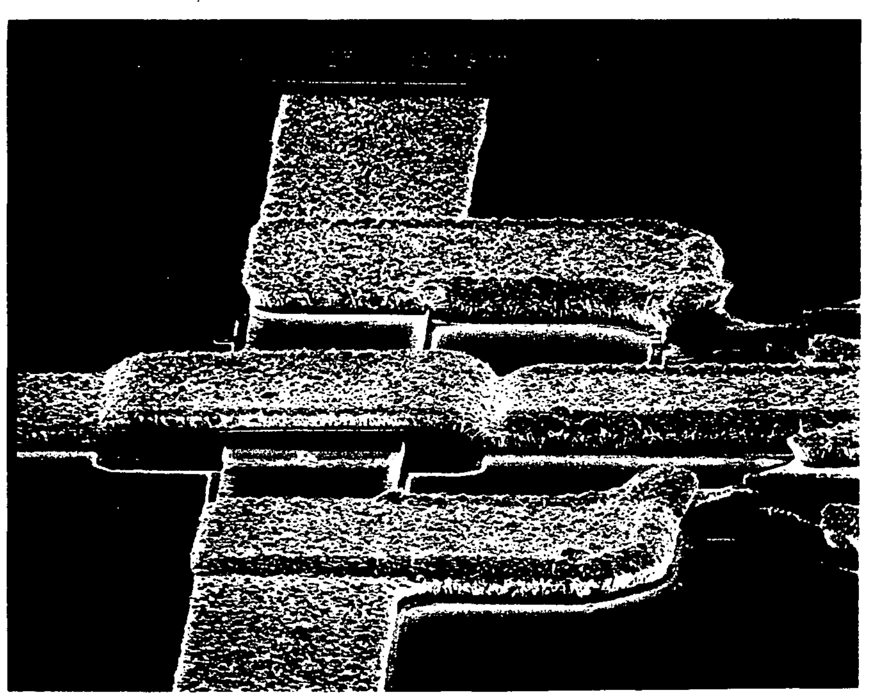


FIGURE 3.15.0: SEM micrographs of air-bridge structures.

CHAPTER 4: DISCUSSION

4.1.0: T-shaped contact structure to the emitter

Experimental results reported in this thesis have demonstrated the fabrication of a T-shaped contact structure for the emitter of AlGaAs/GaAs SAHBTs. Metallisations used consisted of sequentially deposited germanium, molybdenum and an overlay metal, where the overlay metal could be tungsten, gold or nickel. The latter three metals were chosen as possible overlayers because they satisfy the basic requirements of the overlayer which are good electrical conductivity and good adhesion to the bonding metal. The ohmic contact formation occurs by direct synthesis of molybdenum germanide as a contacting metallurgy and a shallow n^+ region formed near the surface of the GaAs by germanium diffusion.

The choice of overlay metal becomes limited when annealing at high temperature (750°C) is required. As shown in figure 3.3.1(c), when gold is used as an overlayer in the contact pad, the T-shaped contact is distorted (upward bending occurs at the edges of the Au). It is believed at present that the distortion is caused by the difference in coefficients of linear expansion for the layers in the contact pad and the host lattice, resulting in a stress at the interfaces of the metal layers. Gold was thus discarded as a possible overlayer for the T-shaped contact.

Tungsten, on the other hand, withstands the annealing but the value obtained for specific contact resistance (1.2 x 10^{-6} ohm-cm^2) is not promising when compared to the value obtained with the conventional Ni/AuGe/Ni/Au contacts (1.0 x 10^{-6} ohm-cm^2).

Moreover, because tungsten has an etch rate very close to that of molybdenum for the gases used during the RIE, the tungsten is only very slightly undercut during the fabrication of the T-shaped contact.

Experimental results have shown that nickel is the best metal as an overlayer. In addition to providing very good ohmic contact, Ni can be etched either by ion beam milling or by the wet etchant described in Section 3.3.2(b). This latter process should be used as standard process because during etching, the Ni layer undercuts the photoresist, thus providing a small separation between the emitter contact and the subsequent base contacts. The etching must however be monitored very carefully to ensure that etching stops as soon as the top of the Mo layer is reached. Although it has been demonstrated that the etchant does not etch Mo, etching must be stopped so as to prevent more undercutting of the photoresist, which would result in an emitter contact very much smaller than the design pattern, consequently affecting the performance of the device. Also, when RIE is afterwards used to undercut the overlayer, Ni provides a nice hard mask which is unaffected by the dry etching. Best contact performance (1.9×10^{-6} ohm-cm^2) was obtained with contact metallisation consisting of Ge(400Å)/Mo(2000Å)/Ni(2000Å).

4.2.0: Annealing and alloying method

The key issue in the annealing of ion-implanted GaAs is the preservation of surface stoichiometry [101] by prevention of arsenic loss from the wafer, while providing high activation of the implanted dopants. Since GaAs dissociates at temperatures

around 640°C and since the annealing temperature was chosen as 750°C, the top and bottom surfaces of the wafer were encapsulated with a thin layer (400Å) of silicon nitride to prevent arsenic loss during the annealing.

As indicated by the results listed in tables 3.1.0 and 3.3.1, by performing only one alloying step for the three metallisation systems (emitter, base and collector), it is possible to obtain good values of ρ_c for all three systems. A study of the Auger profiles for the alloyed contacts to the emitter and collector in the conventional process shows that ohmic behaviour of the contact results from germanium forming an n^+ layer, sufficiently doped to produce a linear current-voltage characteristic as a result of field emission at the contact/GaAs interface. The first nickel layer provides good adhesion to the semiconductor while the second nickel layer provided a cover to hold the liquid AuGe in uniform contact during alloying. For similar contacts alloyed at 750°C for 30 minutes, the mechanism by which ohmic behaviour results appears to be of a different nature to alloying just above the AuGe eutectic as for the conventional process. Figures 3.5.0 (h) shows that there is a much deeper penetration of both germanium and nickel into the GaAs. A high Ga surface concentration is also observed, indicating a certain level of Ga out-diffusion which seems to only be stopped by the overlayer of gold. It is believed at this stage that ohmic behaviour is due to the presence of an n^+ layer at the contact/GaAs interface together with a strong concentration of a Ga-Ni compound in the region under the contact. It must also be noted that the oxygen contamination is

greatly reduced when alloying at 750°C. However, the plot of figure 3.5.0 (h) cannot be correctly interpreted as a depth-composition profile because the alloyed contacts had non-uniform surfaces (figures 3.5.0 (e) & (f)). The Ni/AuGe film balled up on the GaAs surface during alloying, and thus the ion-milling process required for AES did not remove material in a uniform planar manner. The sudden non-ohmic behaviour of the contacts when alloying at 750°C is performed for more than 30 minutes is believed to be due to excessive Gallium out-diffusion resulting in a Ni-As phase underneath the contact. The above results should thus provide the basis for further studies of high temperature alloying of Ni/AuGe films.

Figures 3.5.0 (a) & (b) shows the surface of the Au/Zn/Au contacts to the base after alloying at 750°C for 30 mins and the AES profiles are shown in figures 3.5.0 (c) & (d). Definite cracks that appear on the contact surface are believed to be the result of different expansions of the zinc and the gold, together with an enhanced out-diffusion of Ga at the interface of the gold overlayer and the zinc layer. Ohmic behaviour is believed to be the result of a p^+ layer formed at the contact/GaAs interface by the diffusion of zinc into the GaAs together with a Ga-Au compound in the region underneath the contact. This mechanism is different to alloying at 450°C for 40s whereby ohmic behaviour is the result of a p^+ region formed at the contact/GaAs interface due to the diffusion of zinc into the GaAs. No traces of oxygen were obtained after alloying at 750°C. It is also important to note that the value of specific contact resistance saturates as the alloying time is increased beyond thirty minutes.

4.3.0: Proton implantation

The extrinsic collector capacitance was significantly reduced with the deep implantation of protons (H^+) into the extrinsic collector region underneath the base implant. The effect of reducing that capacitance together with the reduced base series resistance is a key factor in improving the performance of the device. It also prevents the implanted species in the base from diffusing further into the active region of the device during annealing. Proton-implanted GaAs remains compensated even after high temperature anneal.

4.4.0: Performance of self-aligned 8µm HBT

The increase in f_t is associated with the reduction in collector capacitance as a result of the implantation of protons in the extrinsic collector region, thus minimising the collector resistance-capacitance charging time τ_{ec} (see Appendix A2), and also a reduction in parasitic capacitances associated with the emitter as a result of the smaller emitter dimensions due to the proton-implanted region around the emitter contact. Also, the emitter contact itself is smaller because of the undercutting of the overlayer during dry etching. The increase in f_{max} is caused by an increase in f_t and also by a reduction in the base series resistance $r_{bb'}$ and the collector capacitance (see Appendix A2). It must however be noted that improved performance of the above SAHBTs over conventional devices is only an indication of the possible superiority of the self-aligned process over the conventional technology. Further optimisation of the process is essential if the latter is aimed at production.

4.5.0: Zinc diffusion for HBTs

Because of the non-directional nature of the zinc diffusion process, a self-aligned technology such as the one involving the fabrication of a T-shaped contact structure is not suitable. The extent of the lateral diffusion of zinc into the semiconductor would cause the whole of the active region of the device to be doped p type for devices with geometries (1 - 4 µm) comparable to the depth of the diffused zinc (≃ 1µm). It is therefore essential to ensure that the lateral diffusion of the zinc stops before or at the edge of the active region. This is achieved by the use of the capping layer which protects the emitter contact and allows for the lateral diffusion to occur under the dielectric. The capping layer, together with an arsenic overpressure also prevent the loss of arsenic from the crystal during the diffusion.

4.6.0: Advantages of self-aligned process compared to conventional process

The self-aligned process described in this report thus provides us with the following advantages over the conventional method of fabricating HBTs:

(i) Using a single photoresist pattern, the T-shaped contact to the emitter, the implantation of the collector and base extrinsic regions and the base metallisation were performed.

(ii) The separation between base metal and active emitter is controlled by the degree of undercut of the photoresist during the fabrication of the T-shaped contact structure.

(iii) The process allows different metal combinations to be used for the contacts to emitter and base and a single annealing

process provides better uniformity in the performance of the contacts and consequently of the devices.

(iv) Isolation was achieved by proton bombardment of the surface outside the active transistor areas, also providing the destruction of the lateral emitter-base n-p diode at the same time. The isolation also serves the purpose of reducing the base-collector extrinsic capacitance and preventing excessive diffusion of the extrinsic base implant during annealing.

CHAPTER 5: CONCLUSION

Heterojunction bipolar transistors have been fabricated on MBE wafers using (i) the conventional fabrication process, and (ii) the new self-aligned process developed during this project. The latter process involved the definition of a T-shaped contact structure for the emitter by wet and dry etching techniques. Refractory metals deposited by sputtering were used because of their ability to withstand subsequent high temperature process steps. For a metallisation system consisting of Ge(400Å)/Mo(2000Å)/Ni(2000Å) alloyed at 750°C for 30 minutes in a N_2 atmosphere, a low specific contact resistance of 2×10^{-6} ohm-cm^2 was measured by standard transmission line model technique.

Conventional metallisation schemes consisting of sequentially evaporated Ni(50Å)/AuGe(600Å)/Ni(200Å)/Au(2000Å) for the collector and Au(200Å)/Zn(600Å)/Au(2000Å) for the base were all alloyed simultaneously. Specific contact resistances of 8.6×10^{-6} ohm-cm^2 and 1.2×10^{-6} ohm-cm^2 were obtained for the collector and base contacts respectively. These contact resistance values are sufficiently low for the devices to exhibit good microwave performance. After alloying at 750°C for the self-aligned process, the mechanisms by which good contact resistance occurred were found to be of a different nature to the liquid alloying technique used for the conventional process. This self-aligned technique enabled the emitter contact, emitter active region, extrinsic base, base contact and isolation of the extrinsic collector to be performed with one mask.

The possibility of using zinc diffusion as an alternative to ion implantation for doping the base contact regions was

investigated and acceptor concentrations of 1 x 10^{20} cm^{-3} were measured by `Hall and Stripe´ technique. This method of doping the base contact regions allowed for very low ohmic contact resistance to be achieved.

Air-bridge structures were investigated as a possible alternative to bonding pads and a process route is suggested whereby these structures could be incorporated as part of the self-aligned process.

For transistors with the same design dimensions (emitter dimensions: 8µm x 16µm) for both processes, the self-aligned process yielded HBT devices with better microwave performance (f_t= 10.7 GHz and f_{max}= 9.8 GHz) than the conventional technology (f_t= 8.0 GHz and f_{max}= 7.9 GHz). This improvement in performance is an indication of the possible superiority of the newly-developed self-aligned process but further optimisation of the latter is required to improve further on the performance of the HBT.

CHAPTER 6: PROPOSALS FOR FUTURE DEVELOPMENTS OF SAHBTs.

(a) Devices with emitter widths smaller than 8μm should be investigated and the process should now be extended to the fabrication of circuits.

(b) Fabrication of the T-shaped contacts using only dry etching should be investigated by involving other gases for the etching process and possibly other combinations of refractory metals.

(c) Air-bridge structures should be incorporated as an integral part of the fabrication process.

(d) The fabrication of SAHBTs should be investigated on MBE wafers with varying epitaxial structures.

(e) Zinc diffusion should be incorporated as an integral part of the conventional process in the place of ion-implantation. Higher doping concentration of the base contact region and lower values of specific contact resistance can then be achieved and the zinc diffusion process also offers a cheap and reliable way of doping the base contact regions.

(f) A more detailed study of the mechanisms by which ohmic behaviour results after high temperature annealing should be carried out for the metallisation schemes used in the self-aligned process and the study should also be extended to other metallisation schemes.

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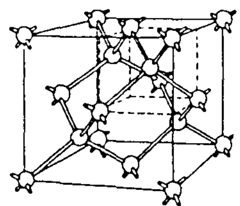
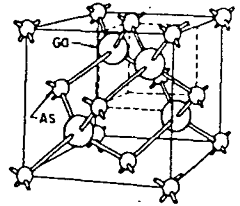
APPENDIX A1

Properties of GaAs at 300K





DIAMOND
(C, Ge, Si, etc)

ZINCBLENDE
(GaAs, GaP, etc)

Figure A1.0 : Lattice structures of Silicon and Gallium Arsenide.

TableA1: Comparison of carrier mobilities between GaAs and Si		
	GaAs	Si
Electron mobility μ_e	8500 cm /V - s	1500 cm /V - s
Hole mobility μ_p	400 cm /V - s	450 cm /V - s

TableA2: Energy gaps for GaAs and AlGaAs at 297 K		
	GaAs	$Al_xGa_{1-x}As$
Eg (direct)	1.424 eV	E_g (0<x< 0.45) = 1.424 + 1.247x eV
		E_g (0.45 < x < 1.0) = 1.424 + 1.247x + 1.147(x-0.45) eV

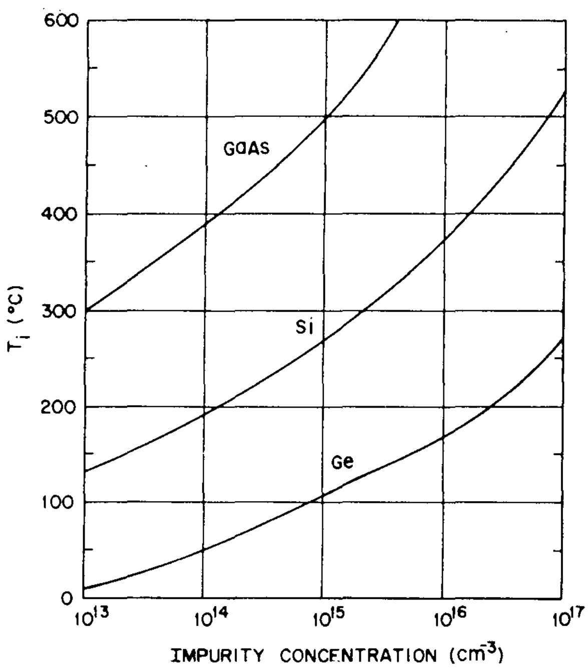


FIGURE A1.1 : Intrinsic temperature as a function of background concentration. (After Sze, Ref.[7])

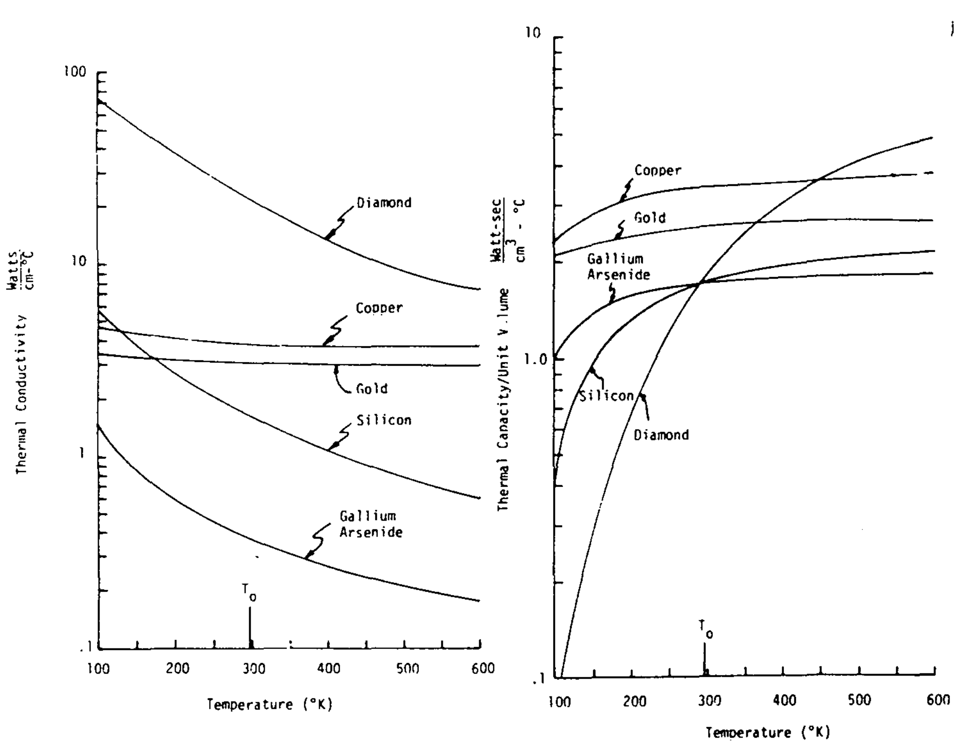


FIGURE A1.2 :Thermal conductivity and thermal capacity per unit volume v/s temperature for selected materials.

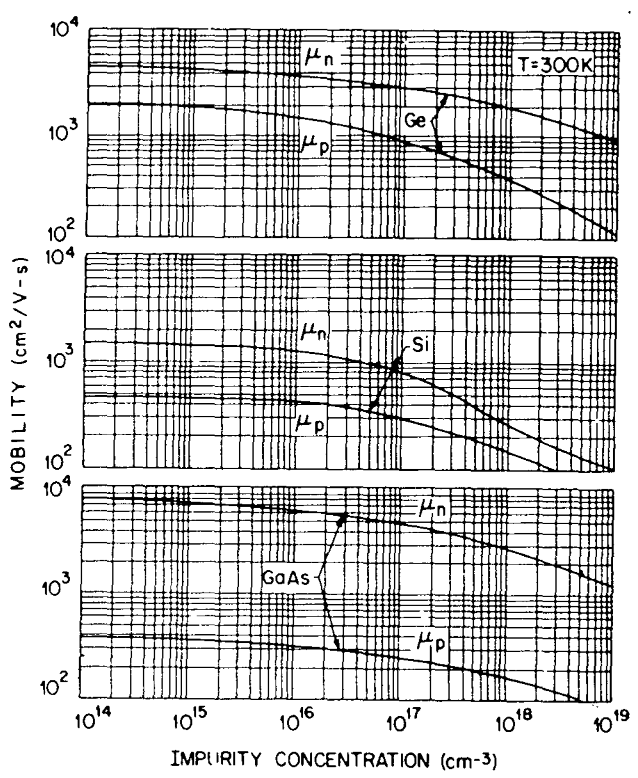


FIGURE A1.3 : Drift mobility of Ge, Si and GaAs at 300 K v/s impurity concentration. (After Casey and Panish, Ref. [7])

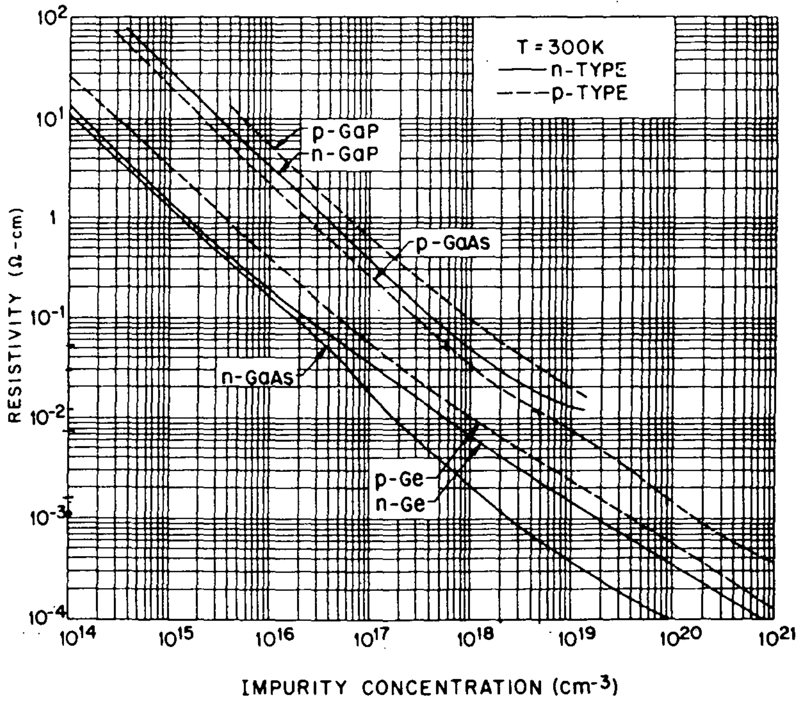


FIGURE A1.4 : Resistivity v/s impurity concentration for Ge, GaAs and GaP at 300 K. (After Sze and Irvin, Ref. [7])

PROPERTIES OF GALLIUM ARSENIDE AT 300K

Property	Value
Atoms/cm^3	4.42×10^{22}
Atomic weight	144.63
Crystal structure	Zincblende
Density (g/cm^3)	5.32
Dielectric constant	13.1
Effective density of states in conduction band, N_c (cm^{-3})	4.7×10^{17}
Effective density of states in valence band, N_v (cm^{-3})	7.0×10^{18}
Effective Mass, m^*/m_0	
Electrons	0.067
Holes	m^*_{lh} = 0.082 m^*_{hh} = 0.45
Electron affinity, χ (V)	4.07
Energy gap (eV)	1.424
Intrinsic carrier concentration (cm^{-3})	1.79×10^6
Intrinsic resistivity (Ω-cm)	10^8
Lattice constant (Å)	5.6533
Linear coefficient of thermal expansion $\Delta L/L\Delta T$ ($°C^{-1}$)	6.86×10^{-6}
Melting point (°C)	1238
Minority carrier lifetime (s)	10^{-8}
Mobility (Drift) (cm^2/V-s)	
Electron	8500
Hole	400
Optical phonon energy (eV)	0.035
Thermal conductivity (W/cm-°C)	0.46
Thermal diffusivity (cm^2/s)	0.24
Vapour pressure (Pa)	1 at 900°C 100 at 1050°C

APPENDIX A2

A/2.0.0: THEORY OF THE HETEROJUNCTION BIPOLAR TRANSISTOR

A/2.1.0: Homojunction

A homojunction is a junction in a single crystal in which both sides of the junction are made of the same material. By introducing impurities in the material, it is possible to have both p type and n type regions existing simultaneously in the semiconductor and form a p-n junction. By applying a voltage bias V across the junction, we change the electrostatic potential barrier and thus the electric field within the transition region. Consequently, we would expect changes in the various components of current at the junction (figure A2.0).

A/2.2.0: Heterojunction structure

A heterojunction is a junction in a single crystal between two dissimilar semiconductors (Gallium Arsenide and $Aluminium_x Gallium_{1-x}$ Arsenide in the case of our heterojunction bipolar transistor). When the two conductors have the same type of conductivity, the junction is called an isotype heterojunction and when the conductivity types differ, the junction is called an anisotype heterojunction.

A/2.2.1: Basic model

The energy-band model of an ideal abrupt heterojunction which neglects the effects of interface traps was proposed by Anderson (1962), who based his efforts on the previous work of Shockley. we consider this model next, since only slight modification of the model is needed to account for non-ideal

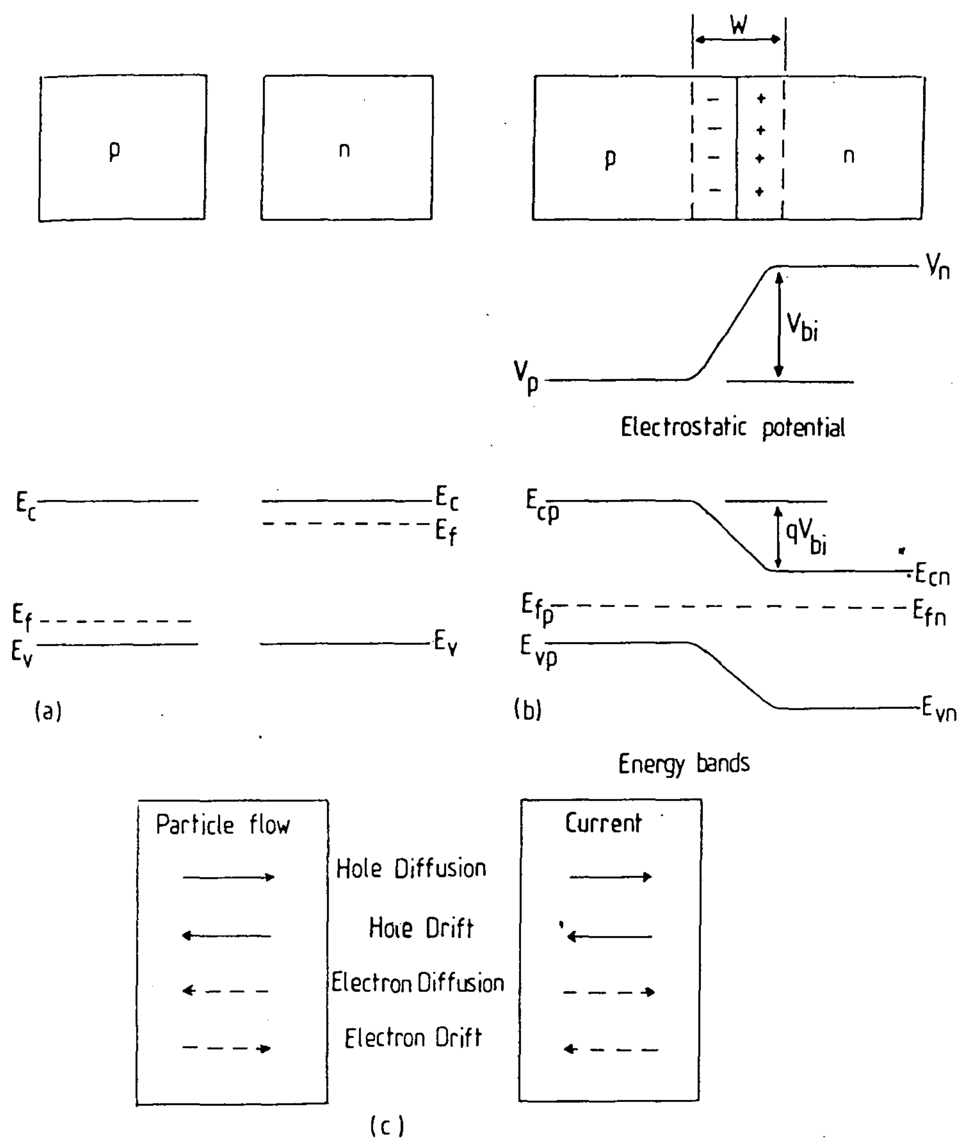


Figure A2.0 (i) : Properties of an equilibrium p-n junction (a) isolated regions (b) junction, showing space charge in the transition region W, the built in voltage and the energy bands (c) directions of the four components of particle flow within W, and the resulting current directions.

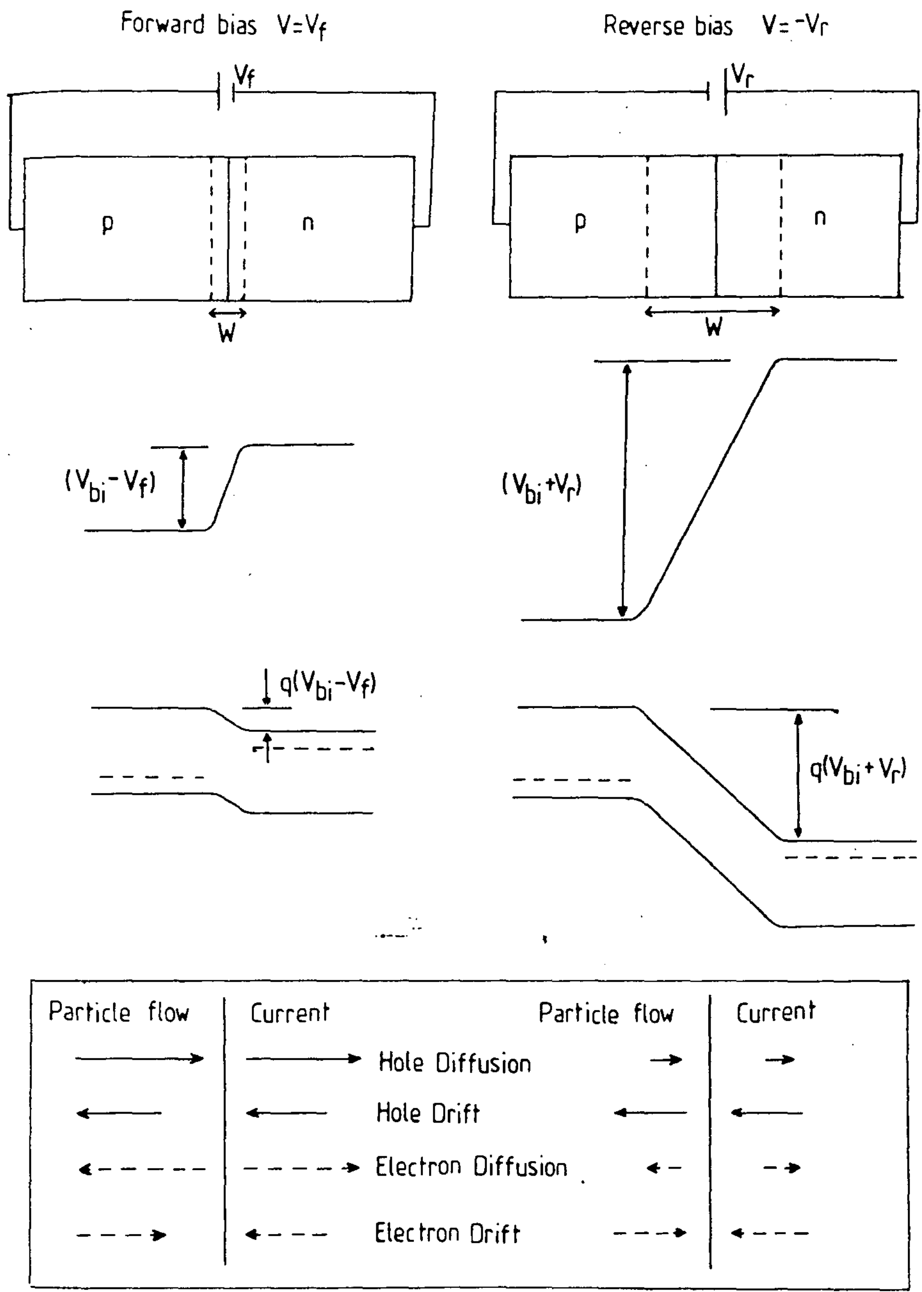


Figure A2.0: Effects of bias at a p n junction; depletion region (ii) width, electrostatic potential, energy band diagram, and particle flow and current directions within W.

cases such as interface traps. Figure A2.1 shows the energy-band diagram of two isolated n and p type semiconductors. The two semiconductors were assumed to have different bandgaps E_{g1} and E_{g2}, different work functions ϕ_1 and ϕ_2 , different electron affinities χ_1 and χ_2. The difference in energy of the conduction band edges in the two semiconductors is represented by ΔE_c and that in the valence band edges by ΔE_v. Figure A2.2 shows that the discontinuity in the conduction band edges is simply the difference in electron affinities of the two materials.

$$\Delta E_c = \chi_1 - \chi_2 \qquad \text{Eqn A2.0}$$

and $$E_{g2} = E_{g1} + \Delta E_c + \Delta E_v \qquad \text{Eqn A2.1}$$

or $$\Delta E_c + \Delta E_v = E_{g2} - E_{g1} = \Delta E_g \qquad \text{Eqn A2.2}$$

Equation A2.2 is an important relation because ΔE_c and ΔE_v are known for GaAs/$Al_x Ga_{1-x}$As, while the difference between the electron affinities is not well established.

When a junction is formed between these semiconductors, the energy-band profile at equilibrium is as shown in figure A2.2 for an n-p anisotype heterojunction. The Fermi level must coincide on both sides in equilibrium and the vacuum level is everywhere parallel to the band edges and is continuous. The total built-in potential V_{bi} is equal to the sum of the partial built-in voltages V_{b1} and V_{b2}, where V_{b1} and V_{b2} are the electrostatic potentials supported at equilibrium by semiconductors 1 and 2, respectively. The discontinuity in the conduction band edges ΔE_c creates a potential step or `spike´ barrier for electrons transversing to the `p´ type base (figures A2.3 and A2.4). Thus

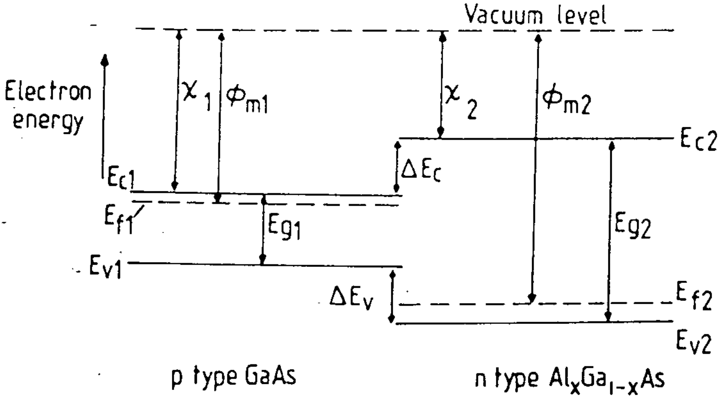


Figure A2.1: Energy-band diagram of isolated 'p' type Gallium Arsenide and 'n' type Aluminium Gallium Arsenide.

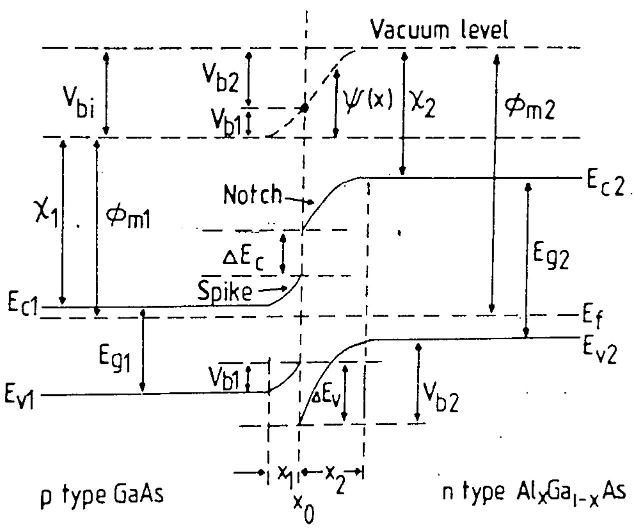


Figure A2.2: Energy-band diagram of an abrupt p-n heterojunction at thermal equilibrium.

there will be a potential drop in the interface of these two materials which can be used to accelerate electrons over the short interfacial distance to a kinetic energy close to, but lower than the difference of minima ($\leqslant$ 0.3 eV) in order to eliminate intervalley scattering mechanisms (i.e. the electrons are restricted to the central valley of the conduction band where the effective mass for electrons is a minimum) (See Appendix A3.0 for further details). Then the majority of these "hot" electrons will move at higher velocity than the maximum diffusion velocity of minority carriers. The width, and more generally, the shape of the spike must be designed so that tunneling through the complete barrier is prevented, therefore the majority of electrons can be accelerated at appropriate energy (and not at lower energy). The width of the spike region depends mainly on the doping level of the `n´ region (emitter).

A/2.3.0: The heterojunction bipolar transistor (HBT).

The concept of using a heterojunction in a bipolar transistor is almost as old as the bipolar transistor itself [1]. The first idea was to use a wide bandgap emitter material in order to improve the emitter efficiency γ, hence the current gain of the transistor. The HBT has an n type $Al_xGa_{1-x}As$ emitter, a p type GaAs base and an n type GaAs collector.

The potential advantages of HBTs include:-

(1) The larger emitter bandgap prevents back-emission of holes into the emitter, resulting in higher emitter efficiency and higher current gain;

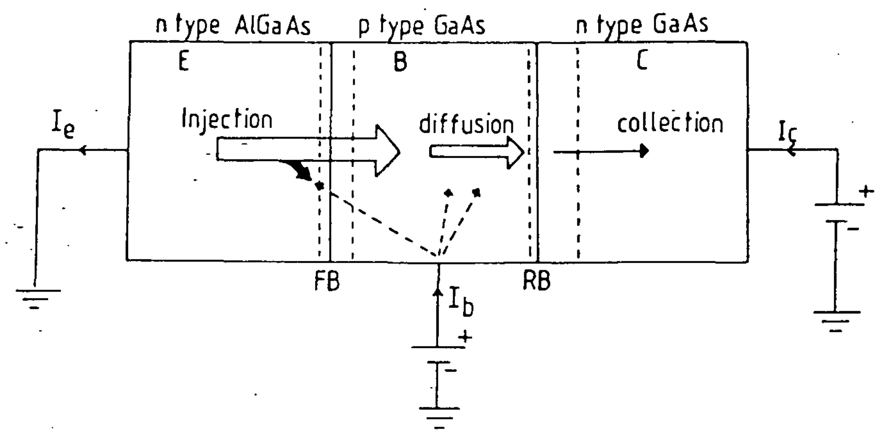


Figure A2.3: An NPN Heterojunction Bipolar Transistor in common emitter configuration.

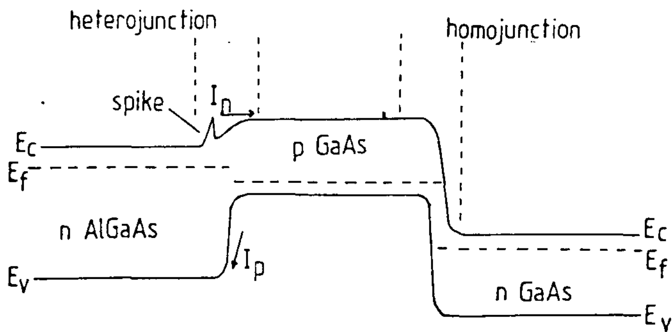


Figure A2.4: Energy band diagram of NPN HBT.

(2) High base doping for low base resistance and good resistance to punch through;

(3) Lower emitter doping for lower emitter-base capacitance;

(4) Improved frequency response because of higher current gain and lower base resistance;

(5) A wider temperature range of operation [2].

A/2.4.0: Grading of the emitter-base bandgap.

For an abrupt heterojunction, there is an additional potential spike (figure A2.4) at the emitter-base junction which reduces injection into the base and hence, the current gain. The spike may or may not limit current, depending on the rate of emission of electrons over the spike, their rate of thermalisation in the base, and the rate at which the thermalised electrons are carried away by diffusion [3]. `Grading´ the emitter-base heterojunction together with the composition and doping grading in the base may be used to improve the electron transit time there. A quasi electric field can be generated by creating an aluminium (Al) gradient in the base of an AlGaAs/GaAs HBT, decreasing in Al content from emitter to collector.

A/2.5.0: Current capability.

In the HBT, the presence of an emitter-base heterojunction profoundly modifies the transistor´s injection efficiency and thus its current gain. Figures A2.3 and A2.4 show carrier movement in an npn transistor. In normal operation, the emitter-base junction is forward biased and the collector-base junction is reverse biased. Electrons are injected from the n type emitter into the p type base. some of these electrons recombine in the

emitter-base interface, in the base region and some reach the collector (figure A2.3).

A common figure of merit for the current handling capacity of a bipolar transistor is the common emitter current gain h which is given by:

$$h_{FE} = \frac{I_c}{I_b} = \frac{I_n - I_r}{I_p + I_r + I_s} \qquad \text{Eqn A2.3}$$

where I_n is the electron current injected from the emitter to the base, I_p is the hole current injected from the base to the emitter, I_s is the current due to electron-hole recombination in the emitter-base space charge region and I_r is the electron injection current which is lost due to recombination within the base region.

Provided the base width W_b is less than about one tenth of the diffusion length of electrons in the base, the effects of I_r on the current gain can be ignored. Assuming that I_s is small relative to I_p, then equation A2.3 can be simplified to:

$$(h_{FE})_{max} = \frac{I_n}{I_p} \qquad \text{Eqn A2.4}$$

I_n and I_p can be expressed in terms of emitter-base voltage V_{eb} (Sze 1981):

$$I_n = \frac{q\ A\ D_{nb}\ n_{ob}}{L_{nb}} \left(\exp\left[\frac{q\ V_{eb}}{K\ T}\right] - 1\right) \qquad \text{Eqn A2.5}$$

where q = electronic charge,

A = cross sectional area of transistor,

D_{nb} = minority carrier diffusion coefficient (base),

L_{nb} = minority carrier diffusion length (base),

n_{ob} = equilibrium carrier concentration in the base,

K = Boltzman's constant,

T = temperature.

Similarly,

$$I_p = \frac{q\ A\ D_{pe}\ p_{oe}}{L_{pe}} \left(\exp\left[\frac{q\ V_{eb}}{K\ T}\right] - 1\right) \qquad \text{Eqn A2.6}$$

where D_{pe} = minority carrier diffusion coefficient (emitter),

p_{oe} = equilibrium carrier concentration in the emitter,

L_{pe} = minority carrier diffusion length (emitter).

Substituting equations A2.5 and A2.6 in equation A2.3, the current gain is given by:

$$(h_{FE})_{max} = \frac{D_{nb}\ L_{pe}}{D_{pe}\ L_{nb}} \times \frac{n_{ob}}{p_{oe}} \qquad \text{Eqn A2.7}$$

The two values n_{ob} and p_{oe} can be expressed in terms of n_i, the intrinsic carrier concentration, and the doping levels of the base and emitter, as follows:

$$n_{ob} = \frac{n_{ib}^2}{P_b} \qquad \text{Eqn A2.8(a)}$$

$$p_{oe} = \frac{n_{ie}^2}{N_e} \qquad \text{Eqn A2.8(b)}$$

where n_{ib} = intrinsic carrier concentration of the base,

n_{ie} = intrinsic carrier concentration of the emitter,

p_b = doping level of the base,

N_e = doping level of the emitter.

By using equations A2.8(a) and (b) in equation A2.7, we have:

$$(h_{FE})_{max} = \frac{D_{nb}\ L_{pe}}{D_{pe}\ L_{nb}} \times \frac{N_e}{P_b} \times \frac{n_{ib}^2}{n_{ie}^2} \qquad \text{Eqn A2.9}$$

where $$n_{ib}^2 = N_{cb}\ N_{vb}\ \exp\left(\frac{-E_{g2}}{K\ T}\right) \qquad \text{Eqn A2.10}$$

and $$n_{ie}^2 = N_{ce}\ N_{ve}\ \exp\left(\frac{-E_{g1}}{K\ T}\right) \qquad \text{Eqn A2.11}$$

Also, N_{cb} = Density of states of holes in the conduction band for the base,

N_{vb} = Density of states of electrons in the valence band for the base,

N_{ce} = Density of states of electrons in the conduction band for the emitter,

N_{ve} = Density of states of holes in the valence band for the emitter.

Combining equations A2.9, A2.10 and A2.11 will result for the current gain in the form of:

$$(h_{FE})_{max} = \frac{D_{nb}\ L_{pe}}{D_{pe}\ L_{nb}} \times \frac{N_e}{P_b} \times \frac{N_{cb}\ N_{vb}}{N_{ce}\ N_{ve}} \left(\exp\left(\frac{\Delta E_g}{K\ T}\right)\right) \qquad \text{Eqn A2.12}$$

where $$\Delta E_g = E_{g1} - E_{g2}$$

Also, the various density of states can be re-written in terms of effective masses of the carriers in the various bands as follows:

$$N_{cb} = 2\left[\left(\frac{2\pi\,[m_{pb}]^{*}\,K\,T}{h^2}\right)\right]^{3/2} \qquad \text{Eqn A2.13(a)}$$

where $[m_{pb}]^{*}$ = effective mass of a hole in the conduction band of the base,

h = Planck's constant.

Similarly,

$$N_{vb} = 2\left[\left(\frac{2\pi\,[m_{nb}]^{*}\,K\,T}{h^2}\right)\right]^{3/2} \qquad \text{Eqn A2.13(b)}$$

where $[m_{nb}]^{*}$ = effective mass of an electron in the valence band of the base,

and

$$N_{ce} = 2\left[\left(\frac{2\pi\,[m_{ne}]^{*}\,K\,T}{h^2}\right)\right]^{3/2} \qquad \text{Eqn A2.13(c)}$$

where $[m_{ne}]^{*}$ = effective mass of an electron in the conduction band of the emitter,

and

$$N_{ve} = 2\left[\left(\frac{2\pi\,[m_{pe}]^{*}\,K\,T}{h^2}\right)\right]^{3/2} \qquad \text{Eqn A2.13(d)}$$

where $[m_{pe}]^{*}$ = effective mass of a hole in the valence band of the emitter.

Substituting equations A2.13(a), (b), (c) and (d) into equation A1.12 yields the final expression for the current gain as follows (equation A2.14):

$$(h_{FE})_{max} = \frac{D_{nb}\;L_{pe}}{D_{pe}\;L_{nb}} \times \frac{N_e}{P_b} \times \left[\frac{([m_{nb}]^{*}\;[m_{pb}]^{*})}{([m_{ne}]^{*}\;[m_{pe}]^{*})}\right]^{3/2} (\exp(\Delta E_g/KT))$$

Thus, the ratio of the emitter doping to the base doping (N_e/P_b) and the energy difference between the n type emitter bandgap and the p type base bandgap are two important elements in determining the current gain of the HBT.

As a matter of interest, let us compare this expression with the expression for the current gain of a homojunction bipolar transistor (an example of which would be a silicon bipolar transistor) [Sze 1981]:

$$\langle (h_{FE})_{max} \rangle_{homo} = \frac{D_{nb} \; L_{pe}}{D_{pe} \; L_{nb}} \times \frac{N_e}{P_b} \qquad \text{Eqn A2.15}$$

Thus the ratio of the emitter doping to the base doping is one of the main factors affecting the gain of a homojunction transistor.

A/2.6.0: The transition frequency "f_t"

"f_t" is related to the sum of the different transit or charging times (τ_{ec}) between the emitter and the collector and is given by:

$$f_t = \frac{1}{2\pi \tau_{ec}} \qquad \text{Eqn A2.16}$$

$$\tau_{ec} = (\tau_{eb} + \tau_b + \tau_d + \tau_c) \qquad \text{Eqn A2.17}$$

where τ_{eb} = emitter-base junction capacitance charging time and is given by:

$$\tau_{eb} = r_e \; (C_e + C_c + C_p) \qquad \text{Eqn A2.18}$$

where $r_e = K\,T / q\, I_e$ is the intrinsic emitter resistance,

C_e = emitter capacitance,

C_c = collector capacitance,

C_p = parasitic capacitances associated with the emitter.

τ_b is the base transit time which is given by:

$$\tau_b = \frac{W_b^2}{\eta D_b} \qquad \text{Eqn A2.19}$$

where η is equal to 2 for a uniformly doped base layer.

τ_d is the base-collector depletion layer transit time and is given by:

$$\tau_d = \frac{x_d}{2V_s} \qquad \text{Eqn A2.20}$$

where x_d is the width of the collector depletion region and V_s is the saturation velocity of carriers in the collector.

τ_c is the collector resistance-capacitance charging time

$$= r_c \; C_c \qquad \text{Eqn A2.21}$$

where r_c = collector series resistance.

Thus, the transition frequency "f_t" is given by:

$$f_t = \frac{1}{2\pi}\left[(C_c + C_e + C_p)\frac{KT}{qI_e} + \frac{W_b^2}{\eta D_b} + \frac{x_d}{2V_s} + r_c C_c\right]^{-1} \qquad \text{Eqn A2.22}$$

From equation A1.22, it is clearly seen that to increase the f_t, the transistor should have a very narrow base thickness, a narrow collector region and should be operated at high current level. To obtain high f_t, each element contributing to the transition time τ_{ec} must be minimised. We shall see how the GaAs/Al_xGa_{1-x} As heterojunction transistor makes this possible.

At identical dimensions, the HBT can permit very low emitter-base charging time with a low current density due to the low emitter doping level compared to the base . The base transit time , another factor in the total transit time, varies with the square of the base thickness. Thus this time can be lowered by reducing the base thickness. Finally , the last two terms in τ_{ec} are, respectively, functions of the collector thickness and doping level.

A/2.7.0: Maximum oscillation frequency f_{max}:

f_{max} is given by:(Sze 1981)

$$f_{max} = (f_p \cdot f_t)^{1/2} \qquad \text{Eqn A2.23}$$

where f_t is the transition frequency and f_p is the parasitic frequency given by:

$$f_p = \frac{\alpha_0}{(8\pi \ r_{bb'} \ C_c)} \qquad \text{Eqn A2.24}$$

where $r_{bb'}$ and C_c are the base resistance and the collector capacitance respectively and α_0 is the dc common base current gain of the transistor:

$$\alpha_0 = \frac{\text{Collector current}}{\text{Emitter current}} \qquad \text{Eqn A2.25}$$

With the HBT, the base region is heavily doped, thus resulting in the low base resistance and therefore higher f_{max} can be obtained. To increase further the f_{max} in the HBT, the base series resistance $R_{bb'}$ must be lowered to a minimum.

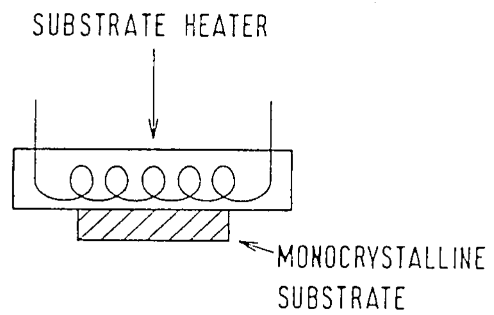
APPENDIX A3

A3.0.0: Molecular beam epitaxy (MBE)

One of the most versatile techniques for growing epitaxial layers is called `molecular beam epitaxy´ (MBE). This technique is capable of depositing a variety of very thin films at low temperatures, with a high degree of uniformity and reproducibility. Materials routinely deposited by MBE include those from the III-V category (GaAs, AlGaAs, GaP, AlAs, GaAsP, GaSbAs, InP, InGaAs, InAlAs, InSb, InAs, InGaP etc), from the IV category (Si, Ge, SiGe), from the II-IV (CdTe, CdS, ZnTe, ZnSe), and from the II-VI category (PbTe, PbSe etc) as well as various metals (Al, W, Mo, Au, Pt, Ti etc).

The properties of these materials as grown by MBE have proved to be especially well suited for fabricating both microwave and optoelectronic devices. In fact, MBE is presently the best epitaxial technique capable of meeting the requirements of devices such as GaAs/AlGaAs HBTs which may have more than fifteen alternating layers, some of which may be as small as 10Å thick. The device efficiency depends to a large extent on the abruptness of interfaces and the doping profile associated with each layer.

Compared to other epitaxial growth techniques, only MBE gives the high degree of control and versatility necessary to fabricate these kinds of structures. In addition, the dislocation densities, mobilities and minority carrier lifetimes of MBE grown films are generally equal or superior to those grown by other state-of-the-art epitaxy techniques. Liquid phase epitaxy (LPE) for example, is limited by poor uniformity and surface



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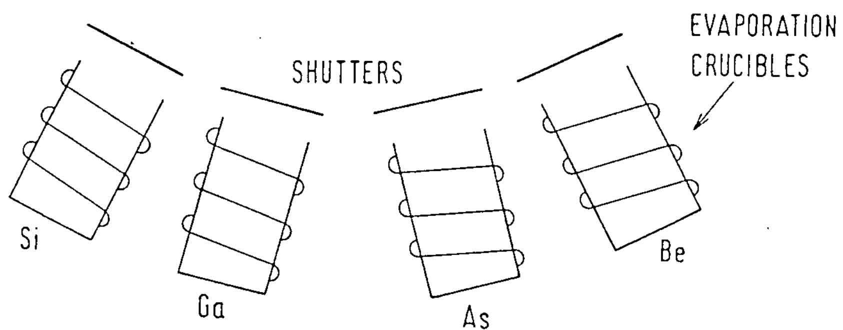

Fig A3.0: Schematic of an MBE growth system

morphology. Vapour phase epitaxy (VPE), on the other hand, is not capable of the film thickness control found with MBE.

In MBE, the substrate is held in a high vacuum while molecular or atomic beams of the constituents impinge upon its surface (figure A3.0). For example, in the growth of AlGaAs layers on GaAs substrates, the Al, Ga, and As components, along with the dopants, are heated in separate cylindrical cells. Collimated beams of these constituents escape into the vacuum and are directed onto the surface of the substrate. The rates at which these atomic beams strike the surface can be closely controlled, and growth of very high quality crystals results. The sample is held at relatively low temperature (about 560°C for GaAs) in this growth procedure. Abrupt changes in doping or in crystal composition (e.g., The ratio of Al to Ga in AlGaAs) can be obtained by controlling shutters in front of the individual beams. Using slow growth rates (1um/hr), it is possible to control the shutters to make composition changes on the scale of the lattice constant. Because of the high vacuum and close controls involved, MBE requires a rather sophisticated set-up, but the versatility of this growth method makes it very attractive for many applications.

In the microwave digital area, devices which are fabricated by MBE include IMPATT diodes, mixer diodes, HEMTs, HBTs and HIGFETs, among others. In the optoelectronic area, LEDs, single and double heterojunction lasers, multi quantum well lasers and GRINSCH (graded index separate confinement heterojunction) lasers, amonst others, have also been fabricated by MBE.

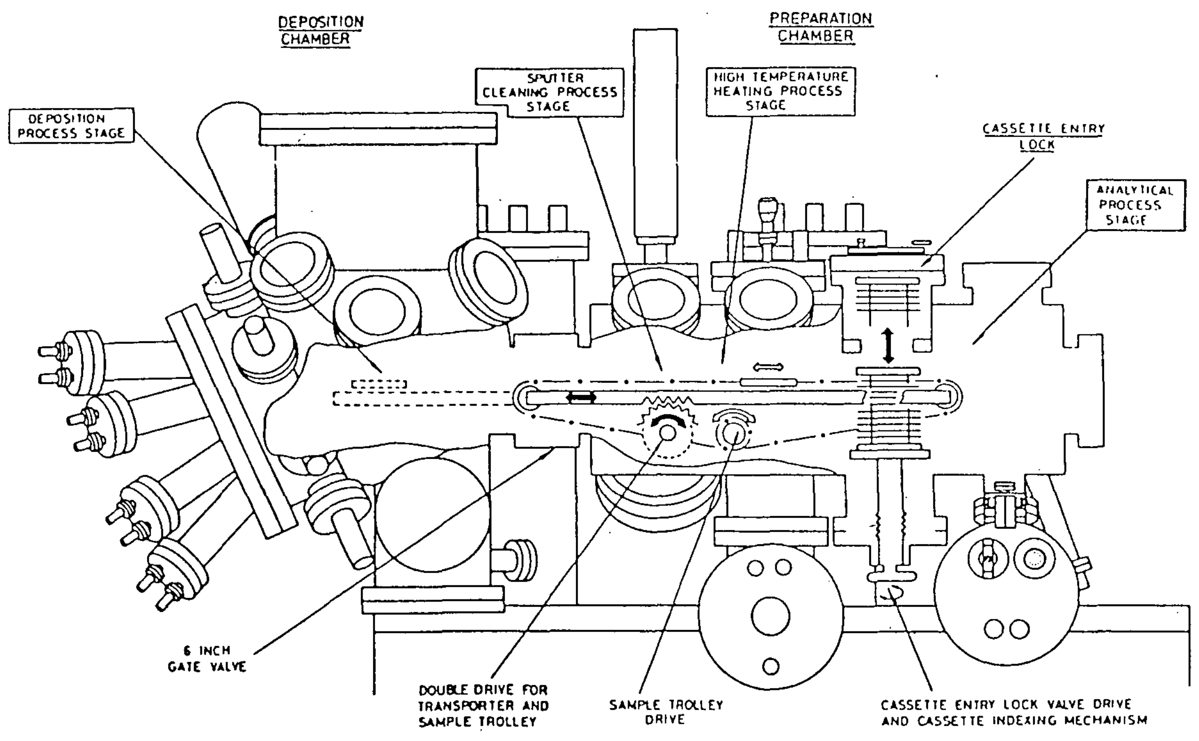

Fig A3.1:Cross-section of the VG V80H MBE III-V machine showing parts of the internal 'cassetrac' sample transfer system (courtesy of VG)

For our purpose, the epitaxial layers for the HBTs were grown by MBE on two inch diameter undoped semi-insulating (100) GaAs. Semi-insulating GaAs was used to minimise parasitic capacitance. Beryllium is used to dope the base (p type) and silicon to dope the n type GaAs and AlGaAs. Table A3.0 describes the typical epitaxial layers likely to be encountered while processing GaAs/AlGaAs HBTs.

The purpose of the cap layer is to prevent the AlGaAs layers of the emitter from being in direct contact with air, since AlGaAs oxidises readily in air. Also, the cap is usually heavily doped to provide good ohmic contact to the emitter. Some wafers include two cap layers, which are only necessary when the doping of the emitter is different to the doping of capl. Cap2 thus allows for only one parameter (doping concentration or material) to be changed at once since changing two parameters at the same time results in unstable electrical properties. The ´grading´, which gradually changes the lattice constant, allows the band gap of the cap (GaAs) to gradually change to meet the band gap of the emitter (AlGaAs). The superlattice layers minimise the migration of defects and impurities during the growth of the layers. The emitter-base interface can be parabolically graded by a variable superlattice. The base layers are confined between two undoped (100) GaAs layers in order to prevent the out-diffusion of Be atoms from the base during material growth. Basel is heavily doped to provide good ohmic contact to the HBT base (base2). The sub-collector provides a high breakdown voltage and consequently acts as a protective layer to the HBT collector (collector2). The layer configuration described can vary from wafer to wafer.

TABLE A3.0

HBT DOPING PROFILE					
TYPE OF WAFER : MBE 'example'					
Layers	Type	Thickness(Å)	Doping (cm^{-3})	Al%	Comments
Cap 1	n^+	500	5×10^{18}		-
Cap 2	n^+	500	2×10^{18}		-
Grading	n^+	700	2×10^{18}	0-30	-
Sub-emitter (or Emitter 1)	n	610	2×10^{18}	30	-
Emitter (2)	n	3000	2×10^{17}	30	-
Super lattice	n	90	2×10^{17}		-
Spacer layer	i	100			-
Base (1)	p^{++}	600	1×10^{19}		-
Base (2)	p^+	3000	1×10^{18}		-
Spacer layer	i	100			-
Sub-collector (or Collector 1)	n^-	10000	1×10^{16}		-
Collector 2	n^+	5000	2×10^{18}		-
Super lattice	i				-
Semi-insulating substrate	SI		undoped		-

APPENDIX A4

A/4.0.0: The Transmission line model (TLM) for assessment of contact resistance.

The most common method for assessing the performance of ohmic contacts to semiconductors is the four point probe 'transmission line model' experiment, originally proposed by Schockley. He suggested that the total resistance between two contacts (each contact of length 'd' and width 'W'), separated by a distance 'l', could be measured and plotted as a function of 'l'. To do this, a constant current through adjacent pairs of rectangular contact pads of varying separation (figures A/4.0 and A/4.1). The voltage drop across the contacts is then measured and used to calculate the observed resistance (R=V/I). Plotting the resistance values obtained against the corresponding contact separations results in a straight line graph, the characteristic equation of which is:

$$R_{total} = \frac{2\, R_{sk}\, L_T}{W} + \frac{R_{sh} \cdot l}{W} \qquad \text{Eqn A4.0}$$

where

R_{total} = Total resistance between any two contacts (ohms),

R_c = Contact resistance (ohms),

R_{sh} = Sheet resistance of layer between the contacts (ohms/square),

R_{sk} = Sheet resistance of semiconductor layer under the contacts (ohms/square),

L_T = Transfer length (i.e. the distance required for current to flow in or out of the contact; also known as the distance from the edge that the

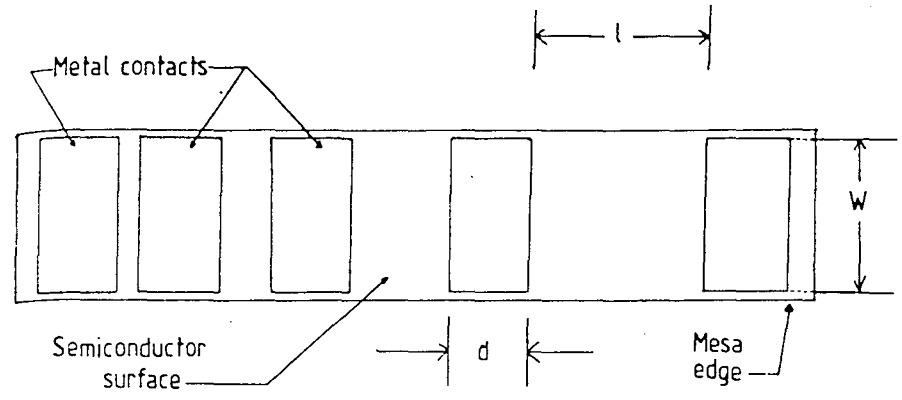

Figure A4.0: Top view of Transmission Line Model

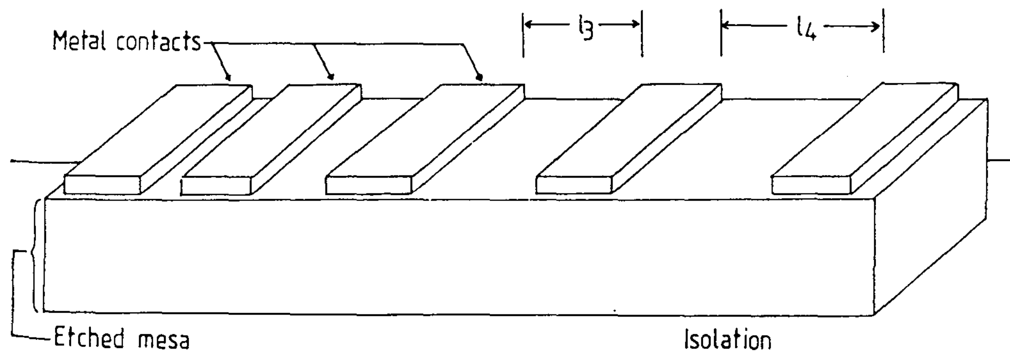

Figure A4.1: 3 dimensional view of Transmission Line Model

current in the semiconductor falls to 1/e of its original value, (μ)

W = Contact width (μ),

d = Contact length (μ),

l = Contact separation (μ).

The intercept on the resistance axis represents the resistance experienced at zero separation and corresponds to 2 R_c (twice the value of contact resistance), because the current flows into the contact and then returns through the same contact.

The contact resistance, R_c , is thus

$$R_c = \frac{R_{intercept}}{2} \qquad \text{Eqn A4.1}$$

Now,

$$R_{total} = \frac{2\, R_{sk} \cdot L_T}{W} + \frac{R_{sh} \cdot l}{W}$$

from the equation of a straight line (y = mx + c).

The slope of the graph is given by:

$$m = \frac{R_{sh}}{W} \qquad \text{Eqn A4.2}$$

The sheet resistance between the contacts (R_{sh}) can thus be determined experimentally from the above equation.

A/4.1.0: The transfer resistance (R_t)

Because of the obvious effect of size upon R_c, it has become useful to refer to the contact resistance in terms of a normalised contact size, usually 1mm (1000 microns). Therefore, R_c is often described in terms of an ohm-mm value and termed the

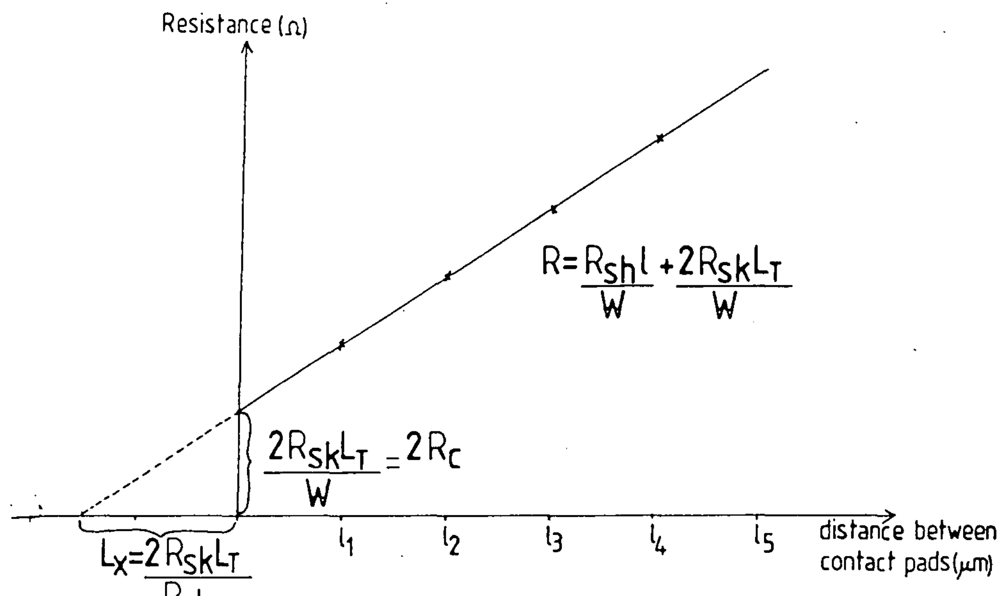

Figure A4.2: Graphical determination of contact resistance R_c from measurements of the TLM.

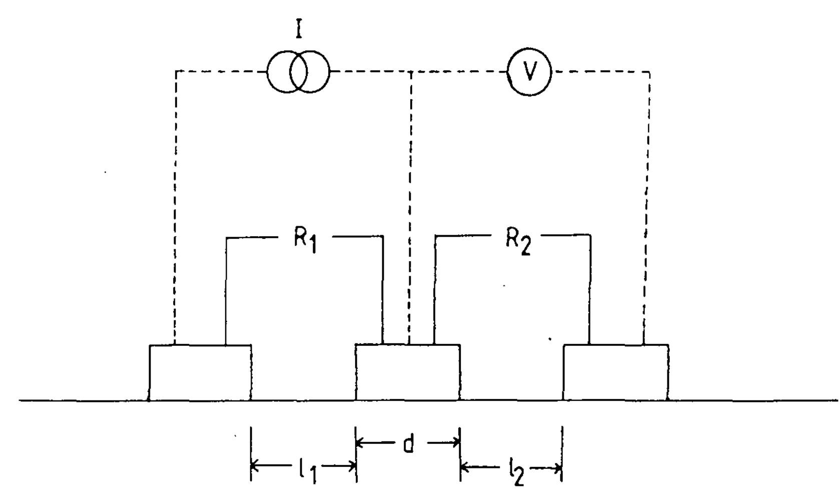

Figure A4.3: Method for the determination of R_E.

transfer resistance, which is given by:

$$R_t = R_c \cdot W \quad \text{(where W is in mm)} \qquad \text{Eqn A4.3}$$

A/4.2.0: Specific contact resistance (ρ_c)

For a more universally accepted assessment of contact performance, a specific contact resistance measurement is required. This, ideally, is the resistance of a unit area of the metal-semiconductor interfacial layer. Equation A2.0 provides an estimate of ρ_c (ohm-cm^2) through the transfer length L_T For an electrically long contact ($d >> L_T$), the sheet resistance under the contact is unmodified, i.e.

$$R_{sk} = R_{sh}$$

therefore,

$$L_x = 2L_T$$

and the specific contact resistance ρ_c is given by:

$$\rho_c = R_{sh} \cdot L_T \qquad \text{Eqn A4.4}$$

from the above definition.

However, in cases where a modification is made to the sheet resistance underneath the contact ($R_{sk} \neq R_{sh}$), extra experimental data is required to modify the equation. Such an experiment that will supply this data is the `end resistance´ measurement.

A/4.3.0: End resistance measurement (R_E)

(a) Method 1

The total resistance between any two contacts is given by:

$$R_{total} = 2R_c + \frac{R_{sh} \cdot l}{W} \qquad \text{Eqn A4.5}$$

However, R_c, the contact resistance, can be shown to be equal to

$$R_c = \frac{R_{sk} \cdot L_T}{W} \coth(d/L_T) \qquad \text{Eqn A4.6}$$

where

$$L_T = \sqrt{\frac{\rho_c}{R_{sk}}} \qquad \text{Eqn A4.7}$$

Hence, for $d \geqslant 2L_T$,

$$R_{total} = \frac{2R_{sk} \cdot L_T}{W} + \frac{R_{sh} \cdot l}{W} \qquad \text{Eqn A4.8}$$

The relationship of equation A4.8 is plotted in figure A4.2 and shows that, if the sheet resistance under the contact is significantly modified, then $L_x = 2L_T$. In this case, the correct value of ρ_c can be found by performing an additional measurement, the contact end resistance (R_E) measurement.

To measure R_E, the standard technique is to pass a constant current between two contacts and to measure the potential between one of these contacts and an opposite outside contact pad. The value of R_E is then V/I (figure A4.3).

In terms of TLM measurements,

$$R_E = \sqrt{\frac{R_{sk} \cdot \rho_c}{W}} \cdot \frac{1}{\sinh(d/L_T)} \qquad \text{Eqn A4.9}$$

$$R_E = \frac{\rho_c}{L_T \cdot W} \cdot \frac{1}{\sinh(d/L_T)} \qquad \text{Eqn A4.10}$$

on eliminating R_{sk} using equation A4.8 .

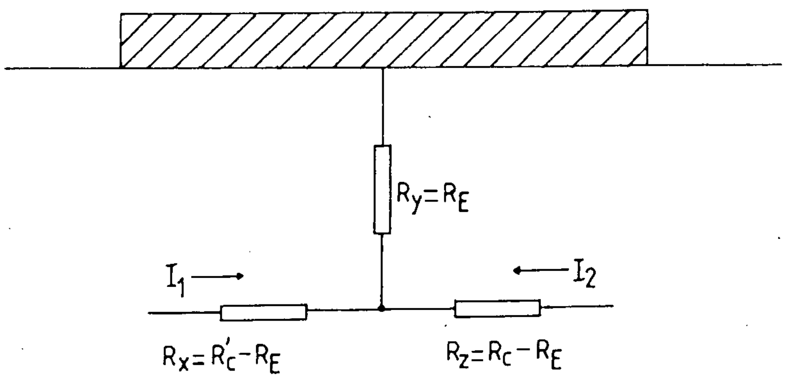

Figure A 4.4: Contact resistance evaluation with the current entering from the left (I_1) or the right (I_2).

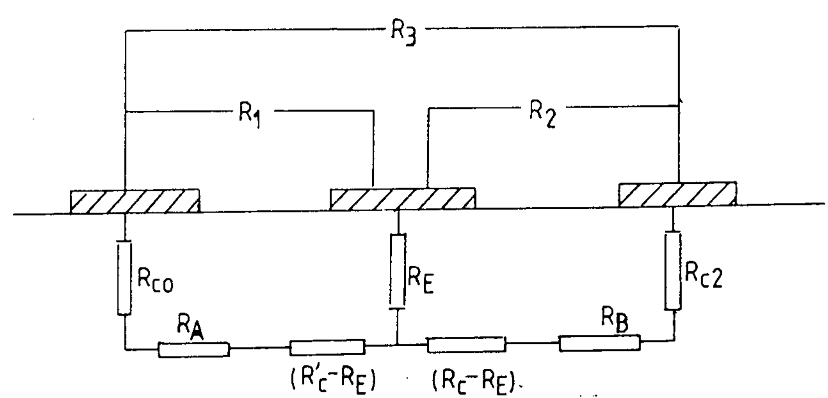

Figure A 4.5: Addition of an extra resistance (R_3) measurement on the TLM provides a value for R_E.

From the above equations,

$$\frac{R_C}{R_E} = \text{Cosh}(d/L_T) \qquad \text{Eqn A4.11}$$

Thus, L_T can be found and ρ_C can be determined from the equation of R_E.

(b) Method 2

It is possible when the contact resistance forms a significant part of the intercontact resistance, and particularly for electrically short short contacts ($d < L_T$), to determine R_E by an extension of the resistance measurements used to obtain the TLM graph. In figure A4.4, it can be seen that the contact resistance, with the current entering from the left, is R_C' (I_2=0) and from the right is R_C (I_1=0).

Therefore,

$$R_X = R_C' - R_E \qquad \text{Eqn A4.12(a)}$$

$$R_y = R_E \qquad \text{Eqn A4.12(b)}$$

$$R_Z = R_C - R_E \qquad \text{Eqn A4.12(c)}$$

In figure A4.5, the addition of an extra resistance measurement on the TLM test pattern provides a value for R_E.

$$R_1 = R_{CO} + R_A + R_C' \qquad \text{Eqn A4.13(a)}$$

$$R_2 = R_C + R_B + R_{C2} \qquad \text{Eqn A4.13(b)}$$

$$R_3 = R_{CO} + R_A + R_C' + R_C - 2R_E + R_B + R_{C2} \qquad \text{Eqn A4.13(c)}$$

Thus,

$$R_E = \frac{(R_1 + R_2 + R_3)}{2} \qquad \text{Eqn A4.14}$$

APPENDIX A5

A5.0: Sputtering: An overview.

Sputtering, i.e., the removal of surface atoms due to energetic particle bombardment, is caused by collisions between the incoming particles and the atoms in the selvage, i.e., the near surface layers of a solid. Generally, an incoming particle will collide with the atoms of the solid, thereby transferring energy to the atomic nuclei. If more energy is transferred than the binding energy at the lattice site , a primary recoil atom is created. The primary recoil atoms will collide with other target atoms distributing the energy via a collision cascade. In crystalline materials, the probability for collisions to create primary recoil atoms, as well as the development of collision cascades, is influenced by the crystal structure due to channeling, blocking or shadowing and focusing effects [A5.0].

Besides sputtering, several other effects are observed with particle bombardment of surfaces (figure A5.0). These are in general, backscattering [A5.1] as well as trapping and reemission of incident particles [A5.2], desorption of surface layers [A5.3], the emission of electrons [A5.4], the emission of photons [A5.5] and a change in surface structure and topography [A5.6].

Sputtering occurs if matter in two extreme states, such as a hot plasma and a solid, interact with each other, or if a directed beam of energetic particles hits a surface. Although application of the sputtering process to the deposition of thin films has been known and practiced for a long time, it is only relatively recently that this method has become a serious competitior to vacuum evaporation. Sputtering offers advantages

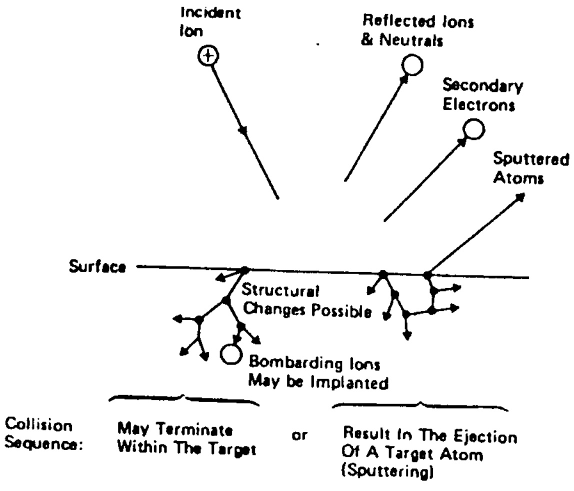

FIGURE A5.0: Mechanisms occurring during sputtering.

over most other deposition techniques if any of the following characteristics or film types are important:

1) Multicomponent films (alloys, compounds, etc.);

2) Refractory materials;

3) Insulating films;

4) Good adhesion;

5) Thickness uniformity over large planar areas;

6) Step coverage.

Sputtering mat not be a suitable method to use if any of the following limitations are unacceptable:

1) Source material must be available in sheet form;

2) Deposition rates are usually less than 2000 Å min^{-1} .

3) Substrate must be cooled.

A5.1: Radio-frequency (RF) sputtering

A typical rf sputtering system is depicted in figure A5.1. The gas (argon) inlet and vacuum pumping system are not shown here. The forward and reflected power meters shown separately here are commonly incorporated into the rf generator chassis. Unlike a dc glow discharge system, the rf system can operate at low gas pressures needed for reliable sputtering work and is capable of relatively high coating rates and can deposit both conducting and insulating materials.

Radio-frequency sputtering is a very simple operation. The proper target(s) is installed and the wafer(s) are loaded into the chamber which is then closed and evacuated to a good vacuum ($\leqslant 1 \times 10^{-6}\,\tau$). The argon pressure is then adjusted, and the rf generator is turned on and set for about one-fouth power. The two

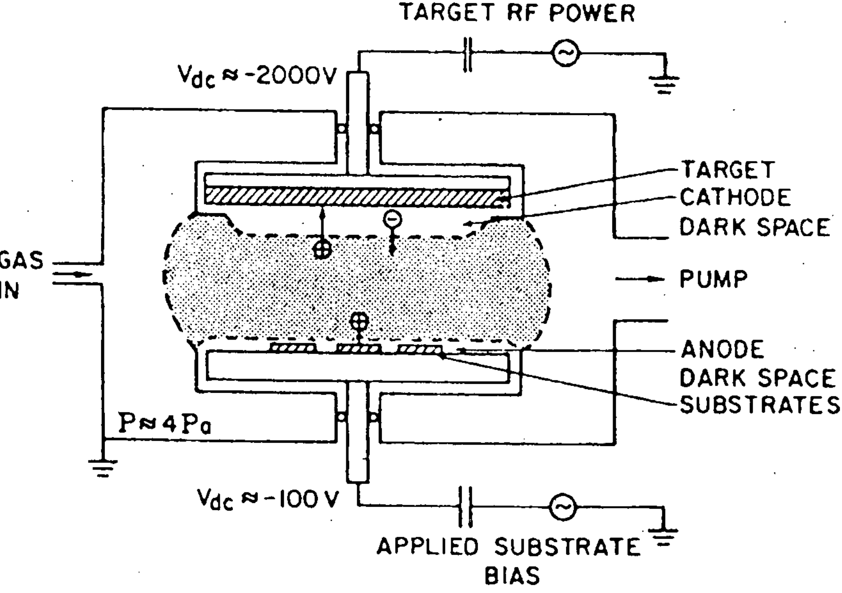

FIGURE A5.1: Cross section of an RF sputtering system.

adjustment controls of the matching network are then tuned to give zero reflected power. Subsequent steps of increasing the power level and retuning the matching network are needed to bring the power up to the desired operating level. The substrates are covered by a shield (or `shutter´, not shown in figure A5.1) during pumpdown, during initial tuning of the matching network, and during sputter cleaning of the target. A few minutes at the desired operating power level will sputter the target surface clean and ensure that the sputtered deposit will be pure. The shield is then opened and the wafer is coated to the required thickness of deposited material. It is necessary to shield the substrates and sputter the target clean each time new substrates are installed.

The sputter cleaning of the target serves two additional useful functions. The plasma always assumes a potential somewhat positive with respect to all surfaces to which it is exposed. As a consequence, all interior surfaces of the sputtering system are subjected to ion bombardment. The energies of ions impinging on surfaces other than the target are too low to cause sputtering, but are high enough to be very effective in causing desorption of gases. This scrubbing action is so effective that a burst of gas is detected (as an increase of pressure in the foreline) at the time the discharge starts. The foreline pressure goes back to its equilibrium value after a moment or two. In addition to the scrubbing action of the discharge, there is a highly effective pumping action due to the sputtering of the material from the target. The material sputtered during the target cleanup period will deposit on exposed surfaces including the back of the shield

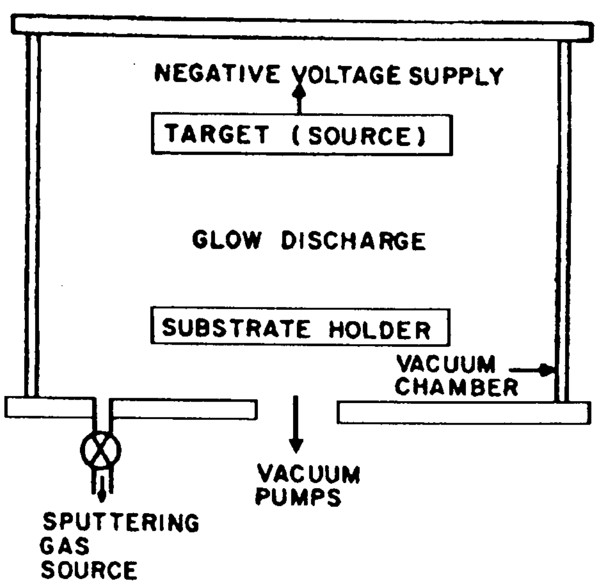

FIGURE A5.2: Simplified diagram of a sputtering system.

that is protecting the substrates. This deposit, being automatically clean, is highly reactive and combines strongly with any reactive gas remaining in the chamber. This action, known as `gettering´, removes reactive gases remaining in the chamber at a high rate, i.e., provides a very efficient pumping action.

Radio-frequency sputtering is very useful as a means of depositing thin film coatings onto parts and substrates. The rf system is very simple to operate and gives reliable, repeatable coatings.

A5.2: Unique characteristics of sputtering

It is not uncommon to try to make comparisons of the evaporation and the sputtering methods of depositing thin film coatings, looking for differences in quality, but it quickly becomes apparent that this is not a useful approach. The choice between evaporation and sputtering is usually a matter of convenience, although there are some things that can be done only by sputtering. Some of the unique characteristics of sputtering that are considered in evaluation of this coating method are the following:

i) Deposition rates do not differ a great deal from one material to another, this is often a useful feature in multilayer depositions.

ii) Thickness control is very simple. fter a calibration run has been made, thickness control is really a matter of setting a timer.

iii)The lifetime of a sputtering target may be as long as

hundreds of runs and is seldom less than 20. This is in sharp contrast to evaporation, where a source seldom lasts as long as 10 runs.

iv) In sputtering alloys and other complicated materials, the deposit maintains stoichiometry with the original target composition.

v) Cleaning of parts and substrates by reverse sputtering is an advantage that can be gained with no other process. One can combine sputter-cleaning with vacuum evaporation, but this obviously tends to complicate operations.

vi) Ejection of particles from sources during evaporation is a problem and is known as `spitting´. The latter does not occur in sputtering.

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APPENDIX A6

A6.0: Ion implantation

Ion implantation is widely used throughout industry as part of the technology for fabricating electronic devices and integrated circuits. Its use is due to several important advantages it has over other doping techniques. For example, the concentration of dopant atoms in the semiconductor can be controlled and varied between wide limits. Also, the technique enables the doping to be performed uniformly and reproducibly over large areas, and by varying the energy of the incident ion beam, it is possible to vary its penetration into the semiconductor (figure A6.0). Hence, the distribution of carriers with depth can be modified easily. With the aid of a suitable mask, it is also possible to implant selective areas to form, for example, the contact regions for the base of the HBT.

The technique of ion implantation entails the bombardment of a material with high velocity, positively charged ions produced in a source held at a high dc potential. After extraction from the source, the beam is mass analysed and allowed to accelerate to the target (sample) which is at earth potential. When the ions impinge on the target, the majority penetrate some distance and slow down by random interaction with the nuclei and electrons of the target. They come to rest at a depth which is a function of the ion energy and of the mass and atomic number of both ion and target atoms. Predictions of the depth distribution of implanted atoms are possible for amorphous targets and are characterised by a projected range, R_p, and a standard deviation ΔR_p (or half width) which signifies the spread in the profile (figure A6.1).

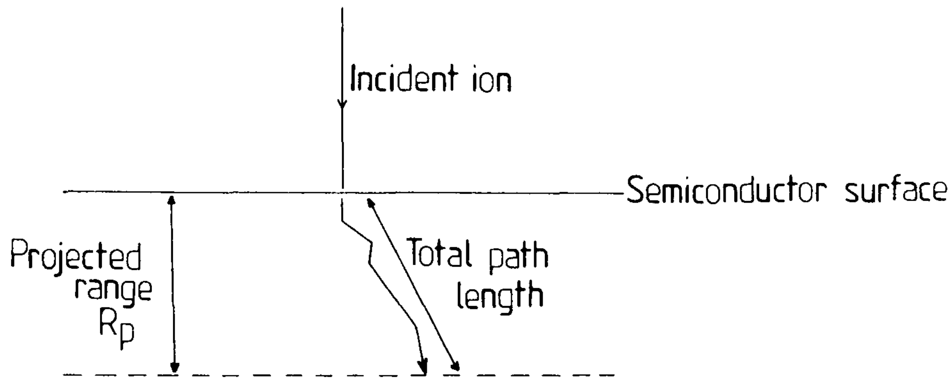


FIGURE A6.0: Range of penetration of ions during implantation.

Perhaps the main disadvantage of ion implantation is the structural damage caused to the substrate due to the dissipation of energy by the incoming ion. That is, the ion slows down and comes to rest by colliding with atoms of the target, so that they are displaced from their lattice sites. The amount of damage depends on the mass and energy of the ion, the temperature of the target and the number (dose) of ions received. In general, the heavier the ion, the greater the damage. In the extreme, a high dose of heavy mass ions can produce an amorphous or finely crystalline layer of thickness about 2-3 times Rp at the surface of a crystalline target. To remove this gross damage, an anneal is required, which not only repairs the lattice but provides the energy required to place the implanted atoms on the correct lattice sites for them to act as dopants. In GaAs, these two processes seem to be sequential since the lattice recovers prior to the electrical activation of the implanted atoms. However, there is always residual damage in the form of dislocation loops which tend to decrease in concentration as the temperature is raised. The necessary post-implantation annealing cycle has posed a serious problem to the application of ion implantation to device and circuit fabrication, since GaAs readily decomposes above 640°C. How this problem has been overcome is discussed next.

Early studies of ion implantation in GaAs revealed that thin layers ($\simeq$0.1um) of dielectrics such as SiO_2 and Si_3N_4 were able to suppress the decomposition of the GaAs and allow the electrical activation of implanted ions to occur. However, the efficiency of the encapsulating layer depends on the deposition

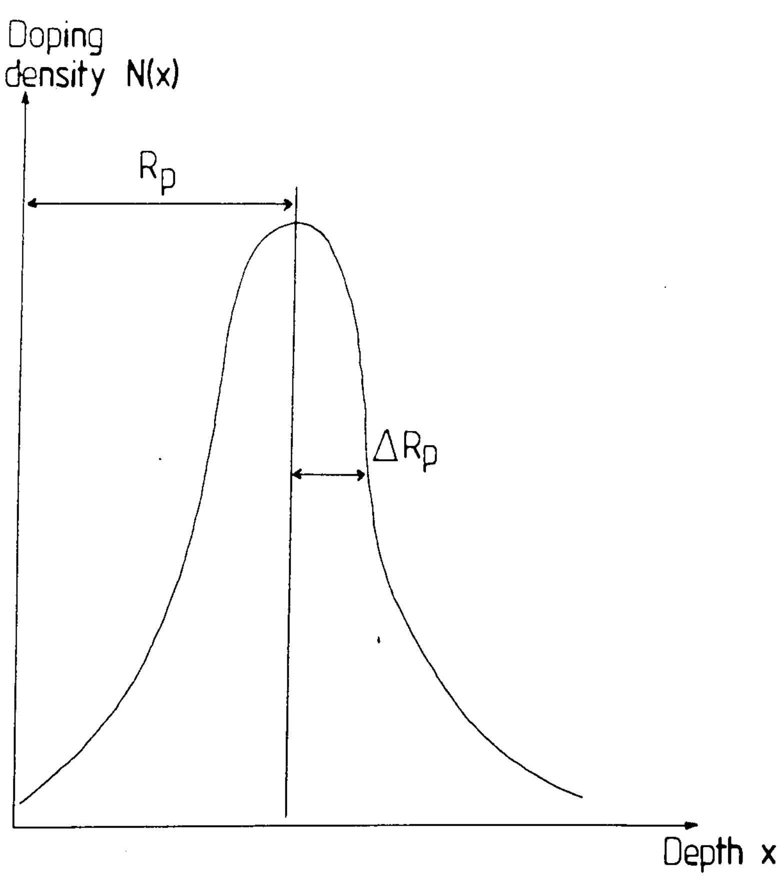


FIGURE A6.1: Distribution of implant density with depth.

method, on the substrate temperature during deposition and on the composition. The reason for this dependence appears to be associated with the strain set up between the layer and the GaAs which, if excessive, can cause bubbling and mechanical failure of the encapsulant. It was also thought for some time that the control of arsenic overpressure to prevent dissociation might allow capless annealing to be used. However, this seems to be true only for relatively low dose implants and temperatures below about 950°C.

Since most implanters are limited to a voltage of about 200KV, there has been emphasis on the use of light ions, in particular Si for n type regions and Be for p type applications. The heavy ions Se, Te and Cd are not favoured because the available ion range is too limited. The important difference between donor and acceptor implants in GaAs is the ease with which the acceptors become electrically active compared with the donors. The reason for this difference between acceptors and donors is not clear. During the annealing of acceptor implanted GaAs, there is often significant broadening of the profiles, the amount depending on dose and annealing temperature. Recently, rapid thermal annealing (RTA) has been used successfully to limit the diffusional broadening of the profiles that occurs during long time anneals in a furnace.

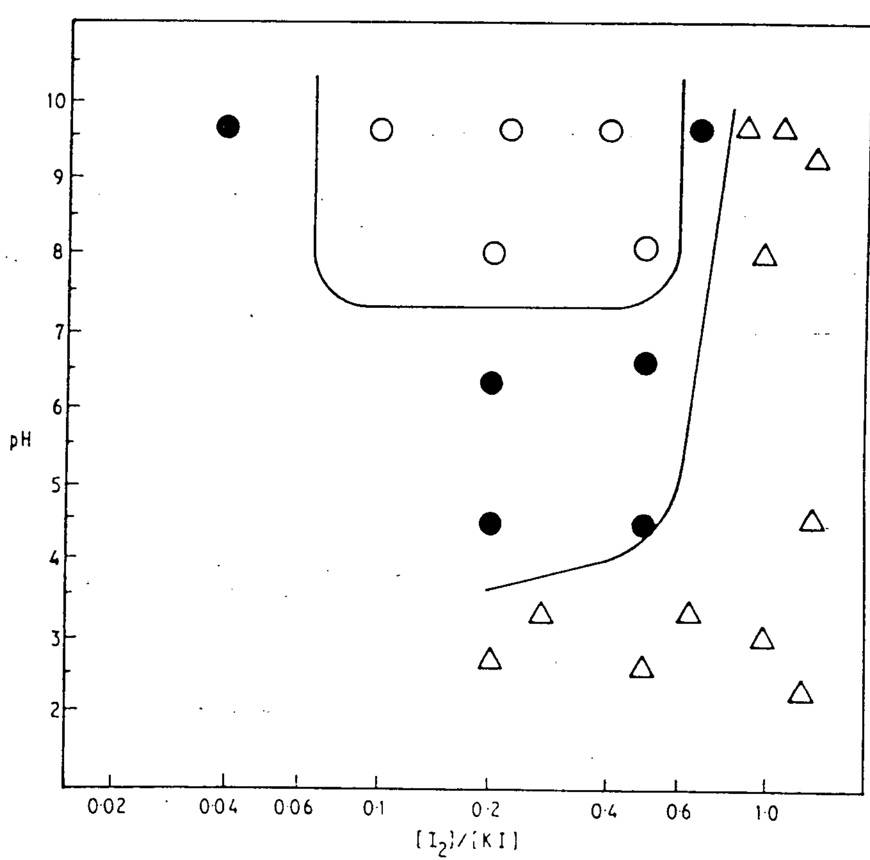
A method of obtaining the required isolation in GaAs devices is to create selectively, high resistivity layers using ion implantation. This can be achieved using, for example, protons, which create defects which compenstae both p type and n type GaAs. Heavier mass ions can be used instead of protons and may be

particularly useful for isolating very shallow layers. Boron and nitrogen implants have been used but, if good thermal stability is essential, then, oxygen ions should be used. Following implantation, oxygen implanted samples are usually annealed at temperatures between 600°C and 800°C to produce high resistivity layers due to the presence of deep levels associated with the oxygen. The radiation damage in this case will be removed during the high temperature anneal.

The annealing process produces high electrical activities and good mobilities for low dose implants and acceptable levels of activation for high doses.

APPENDIX A7

Selective etching behaviour of the
redox system I2-KI



APPENDIX A8

LIST OF ABBREVIATIONS

AES	Auger electron spectroscopy
CVD	Chemical vapour deposition
FA	Furnace annealing
HBT	Heterojunction bipolar transistor
LPE	Liquid phase epitaxy
MBE	Molecular beam epitaxy
MOCVD	Metal-organic chemical vapour deposition
MOVPE	Metal-organic vapour phase epitaxy
PMMA	Polymethylmethacrylate
RIBE	Reactive ion beam etching
RIE	Reactive ion etching
RHEED	Reflection high-energy electron diffraction
RTA	Rapid thermal annealing
SAHBT	Self-aligned heterojunction bipolar transistor
SEM	Scanning electron microscopy
STEM	Scanning transmission electron microscopy
SPE	Solid phase epitaxy
TLM	Transmission line model
VPE	Vapour phase epitaxy

APPENDIX A9

LIST OF SYMBOLS

A	Cross sectional area of device
α_0	DC common base current gain of transistor
C	Capacitance
C_c	Collector capacitance
C_e	Emitter capacitance
C_p	Parasitc capacitance
d	Contact pad length
D_n	Diffusion coefficient
D_{nb}	Minority carrier diffusion coefficient (base)
D_{pe}	Minority carrier diffusion coefficient (emitter)
E_g	Bandgap energy of semiconductor
f_{max}	Maximum oscillation frequency
f_t	Unity gain cut off frequency
f_p	Parasitic frequency
h	Planck´s constant
h_{FE}	Common emitter current gain (β)
I_b	Base current
I_c	Collector current
I_e	Emitter current
I_n	Electron current injected from emitter to base
I_p	Hole current injected from base to emitter
I_r	Electron injection current loss due to recombination within the base region
I_s	Current due to electron-hole recombination in the emitter-base space charge region
J_c	Collector current density

K	Boltzmann's constant
l	Separation between contact pads
L_{nb}	Minority carrier diffusion length (base)
L_{pe}	Minority carrier diffusion length (emitter)
L_T	Transfer length
m	Gradient
$[m_{nb}]^*$	Effective mass of an electron in the valence band of the base
$[m_{ne}]^*$	Effective mass of an electron in the conduction band of the emitter
$[m_{pb}]^*$	Effective mass of a hole in the conduction band of the base
$[m_{pe}]^*$	Effective mass of a hole in the valence band of the emitter
η	Numerical factor in equation for base transit time
n	Doping density
N_A	Acceptor concentration
N_D	Donor concentration
N_{cb}	Density of states of holes in the conduction band for the base
N_{ce}	Density of states of electrons in the conduction band for the emitter
N_e	Doping level of the emitter
N_{vb}	Density of states of electrons in the valence band for the base
N_{ve}	Density of states of holes in the valence band for the emitter

n_{ib}	Intrinsic carrier concentration of the base
n_{ie}	Intrinsic carrier concentration of the emitter
n_{ob}	Equilibrium carrier concentration in the base
ϕ	Work function
P_b	Doping level of the base
p_{oe}	Equilibrium carrier concentration in the emitter
q	Electronic charge
$r_{bb'}$	Base series resitance
r_c	Collector series resistance
r_e	Intrinsic emitter resistance
R_c	Contact resistance
R_E	End resistance measurement
R_p	Projected range
R_{sh}	Sheet resistance of layer between the contacts
R_{sk}	Sheet resistance of semiconductor layer under the contacts
R_t	Transfer resistance
R_{total}	Total resistance between any two contacts
ρ_c	Specific contact resistance
T	Temperature
τ_b	Base transit time
τ_c	Collector resistance-capacitance charging time
τ_d	Base-collector depletion layer transit time
τ_{eb}	Emitter-base junction capacitance charging time
τ_{ec}	Sum of the different transit or charging times between the emitter and the collector
V_{bi}	Built-in potential
V_{CE}	Collector-emitter voltage
v_{sat}	Saturation velocity of carriers in the collector

W	Width of contact pad
W_b	Width of the base layer
x_d	Width of the collector depletion region
χ	Electron affinity
γ	Emitter injection efficiency

APPENDIX A10

GLOSSARY OF TERMS AS APPLIED TO MATERIALS

Acceptor level:- An acceptor level is defined as an energy level in the forbidden gap which traps a certain density of holes (p type carriers) at T=0. Such levels are called acceptor levels because they may become occupied by electrons.

Acceptor saturation:- Filled acceptor levels in p type semiconductors. As a result, thermal activation does not increase the number of extrinsic carriers.

Activation energy:- Energy barrier which must be met prior to reaction.

Active region:- Region of a device where the function that is required of the device is actually taking place.

Alloy:- A composition of two or more metals; an alloy may be a compound of the metals, a solid solution of them, a heterogeneous mixture, or any combination of these. The term is sometimes extended to include non-metallic components; e.g. iron-carbon alloys.

Anisotropic:- Possessing different properties in different directions; e.g. certain crystals have a different refractive index in different directions.

Anisotype heterojunction:- A heterojunction where the two semiconductors forming the junction have different types of conductivity.

Annealing:- Regulated heat treatment, especially of crystal lattices, to relieve strains set up during processing.

Bandgap:- The separation between the energy of the lowest conduction band and that of the highest valence band is called the bandgap E_g .

Base transit time:- The finite time required for the majority carriers to travel from emitter to collector when the transistor is in operation.

Base transport factor:- The ratio of incremental hole current reaching the collector to the incremental total emitter current.

Charge carriers:- Particles that carry the charge when an electric current flows. In a metal they are the free electrons, in a semiconductor they are electrons and/or holes. In an electrolyte they are ions, and in a gas they are ions and electrons.

Cleavage:- The manner of breaking of a crystalline substance, so that more or less smooth surfaces are formed.

Conduction band:- The range of energy levels in a semiconductor corresponding to states in which the electrons can be made to flow by an applied electric field.

Conduction electron:- Electron raised above the energy gap to serve as negative charge carrier.

Conductivity:- Transfer of thermal or electrical energy along a potential gradient.

Crystal:- A physically uniform solid, in three dimensions, with long range repetitive order.

Crystal lattice:- The spatial arrangement of equivalent sites within a crystal.

Defect:- A discontinuity in the pattern of atoms, ions, or electrons in a crystal.

Depletion region:- The region of a semiconductor in which the density of mobile carriers is too low to neutralise the fixed charge density of donors and acceptors. It forms at an interface between two regions of different conductivity.

Dielectric:- An insulator. A substance in which an electric field gives rise to no net flow of electric charge but only to a displacement of charge.

Diffusion:- Type of movement of atoms or molecules in a material whereby the particles distribute themselves equally within the limits of the material.

Diffusion coefficient:- Diffusion flux per unit concentration gradient.

Donor levels:- A donor level is defined as an energy level in the forbidden gap which traps a certain density of electrons (n type carriers) at T=0.

Electric field:- The region surrounding an electric charge, in which a force is exerted on a charged particle; the electric field strength (or electric intensity) is completely defined in magnitude and direction at any point by the force upon unit positive charge situated at that point.

Electrical conductivity:- Coefficient between charge flux and electric field.

Electrical resistivity:- Resistance of a material with unit dimensions. Reciprocal of electrical conductivity.

Electron:- An elementary particle having a rest mass of 9.109558×10^{-31} kg and bearing a negative charge of 1.602192×10^{-19} coulombs.

Electron affinity:- (i) The tendency of an atom or molecule to accept an electron and form a negative ion; (ii) The energy required to release an electron from the bottom of the conduction band to the vacuum level.

Emission spectra (photon):- Range of wavelengths exhibited during emission of a photon.

Emitter efficiency:- Ratio of incremental hole current from the emitter to the incremental total emitter current.

Energy band:- Orbital electrons are associated with specific amounts of energy, the change from one energy level to another taking place in quantized steps. In a crystalline solid the energies of all the electrons and atoms fall into several `allowed´ energy bands between which lie `forbidden´ bands. These bands may be depicted on an `energy level diagram´. The range of energies corresponding to states in which the electrons can be made to flow, by an applied electric field, is called the conduction band. The range of energies corresponding to states that can be occupied by valence electrons, which bind the crystal together, is called the valence band. The valence band in an ideal crystal is completely occupied at the absolute zero of temperature, but in real crystals above absolute zero some electrons are missing from the valence band, and it is these electrons that give rise to holes.

Energy gap:- Unoccupied energies between the valence band and the conduction band.

Eutectic mixture:- A solid solution of two or more substances, having the lowest freezing point of all the possible mixtures of the components. This in taken advantage of in alloys of low melting point, which are generally eutectic mixtures.

Eutectic point:- Two or more substances capable of forming solid solutions with each other have the property of lowering each other´s freezing point; the minimum freezing point attainable, corresponding to the eutectic mixture, is the eutectic point.

Expansivity:- Coefficient of thermal expansion; the increase in length of unit length, caused by a rise in temperature of $1^{\circ}C$.

Field emission:- The emission of electrons from an unheated surface as a result of a strong electric field existing at that surface.

Fermi level:- The energy level in a solid at which the probability of finding an electron is 1/2. At absolute zero, all the electrons would occupy levels below the Fermi level. But at real temperatures, in conductors the Fermi level lies in the conduction band, in insulators it lies in the valence band, and in semiconductors it lies in the gap between the conduction band and the valence band.

Flux:- The rate of flow of mass or energy per unit area normal to the direction of flow.

Flux density:- The flux per unit of cross-sectional area.

Free electron:- An electron that is not attached to an atom, molecule, or ion, but is free to move under the influence of an electric field.

Frequency:- The number of cycles, oscillations, or vibrations of a wave motion or oscillation in unit time, usually one second.

Gain:- An increase in electronic signal power; usually expressed as the ratio of the output power (for example, of an amplifier) to the input power in decibels.

Getter:- Vacuum getter. A substance used for removing the last traces of air or other gases in attaining a high vacuum.

Glow discharge:- A silent electrical discharge through a gas at low pressure, usually luminous, due to recombination of oppositely charged ions.

Grain (metals and ceramics):- Individual crystal of a microstructure.

Grain boundary:- The zone of crystalline mismatch between adjacent grains.

Ground state:- The most stable energy state of a nucleus, atom, or molecule.

Hall effect:- If an electric current flows in a wire placed in a strong transverse magnetic field, a potential difference is developed across the wire, at right angles to both the magnetic field and the wire.

Hall mobility:- Drift mobility. The mobility of carriers in a semiconductor; numerically, it is the velocity of the carriers under the influence of an electric field of 1 volt per metre.

Hertz:- The derived SI unit of frequency defined as the frequency of a periodic phenomenon of which the periodic time is 1 second; equal to 1 cycle per second.

Heterogeneous:- Not of a uniform composition; showing different properties in different portions.

Hole:- The absence of an electron in the valence structure of a body.

Hot electron:- Electron with energy more than a few KT above the Fermi energy, where K and T are Boltzman´s constant and temperature respectively. Thus the electron is not in thermal equilibrium with the lattice.

Interface traps:- Energy levels in the bandgap. They trap transition of carriers between conduction band and valence band.

Junction (semiconductor):- Interface between n type and p type semiconductors.

Kirk effect:- A high field relocation phenomenon, which causes the effective base width W_b to increase and causes a reduction in h_{FE} .

Lattice:- The regular network of fixed points about which molecules, atoms or ions vibrate in a crystal.

Mean free path:- Mean distance travelled by electrons between deflections or reflections.

Miller Indices:- A method of defining the various planes, types of planes and directions in a crystal lattice. The planes are determined by first finding the latters´ intercept with the three basic lattice vectors in terms of the lattice constants, and then taking the reciprocal of these numbers and reducing them to the smallest three integers having the same ratio.

Minority carriers:- In a semiconductor, the type of carriers that constitute less than half the total number of carriers.

Mobility:- The drift velocity of an electric charge per unit electric field [(cm/s)/(volt/cm)]. Alternatively, the diffusion coefficient of a charge per volt [(cm^2/s)/volt].

Ohm:- The derived SI unit of resistance defined as the resistance between two points of a conductor when a constant difference of potential of 1 volt, applied between these two points, produces in the conductor a current of 1 ampere.

Orientation:- Strain process by which molecules are elongated into one preferred alignment.

Oxide:- A binary compound with oxygen.

Passive:- Denoting an electronic component, such as a capacitor, that does not amplify a signal.

Permeability:- A body is said to be permeable to a substance if it allows the passage of the substance through itself.

Permittivity:- The absolute permittivity of a medium is the ratio of the electric displacement to the strength of the electric field at the same point. The absolute permittivity of free space, ε_0, is a fundamental constant, called the electric constant. In a statement of Coulomb´s law for the force, F, between two charges Q_1 and Q_2, it is given by:

$$F = Q_1 Q_2 / r^2 4\pi\varepsilon_0$$

where r is the difference between the charges. ε_0 has the value 8.854185 x 10^{-12} Fm^{-1} . The relative permittivity, ε_r , also called the dielectric constant, is the ratio of the

capacitance of a capacitor with a specified medium (dielectric) between the plates, to the capacitance of the same capacitor with free space between the plates, i.e., $\varepsilon_r = \varepsilon/\varepsilon_0$.

Peroxide:- An oxide that contains more oxygen than the normal oxide of an element.

Phonon:- The quantum of thermal energy in the lattice vibrations of a crystal.

Photon:- A quantum of electromagnetic radiation that has zero rest mass, and energy equal to the product of the frequency of the radiation and the Planck constant. Photons are generated when a particle possessing an electric charge changes its momentum, in collisions between nuclei or electrons, and in the decay of certain nuclei and particles.

Point defect:- Crystal imperfection involving one (or very few) atoms or molecules or ions.

Proton:- A stable particle, with electric charge equal in magnitude to that of the electron but of opposite sign, and with mass 1836.12 times greater than that of the electron (1.672614×10^{-27} kilogram). The proton is a hydrogen ion (i.e. a normal hydrogen atomic nucleus) and is a constituent of all other atomic nuclei.

Quasi Fermi levels:- Under thermal equilibrium, the densities of electrons and holes are specified by the position of the Fermi level through the following equations:

$$n = n_i e^{(E_{fn} - E_i)/KT}$$

$$p = n_i e^{(E_i - E_{fp})/KT}$$

where E_{fn} and E_{fp} are called the quasi Fermi levels.

Rectifier:- Electric valve which permits forward current and prevents reverse current.

Resistance, electrical:- The potential difference between the ends of a conductor divided by the electrical current flowing through the conductor.

Semiconductor:- A material with controllable conductivities, intermediate between insulators and conductors. Extrinsic semiconductors are semiconductors which have impurities added to them to increase or decrease the conductivity whereas intrinsic

semiconductors consist of the pure material without any impurities added to them.

Vacancy:- Unfilled lattice site.

Valence band:- The range of energies in a semiconductor corresponding to states that can be occupied by the valence electrons binding the crystal together.

Work function:- At the absolute zero of temperature, the free electrons present in a metal are distributed amongst a large number of discrete energy states E_1, E_2, etc., up to a state of maximum energy E. At higher temperatures a small proportion of the electrons have energies greater than E. The work function of a metal is the enrgy that must be supplied to free electrons possessing energy E, to enable them to escape from the metal.

Zincblende:- Sphalerite. Natural zinc sulphide, ZnS. An important ore of zinc.

APPENDIX 11

FURTHER USEFUL INFORMATION

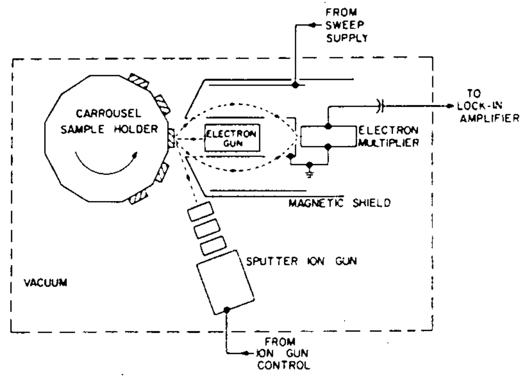


FIGURE A11.1: Schematic diagram of electron energy analyser for Auger electron spectroscopy.

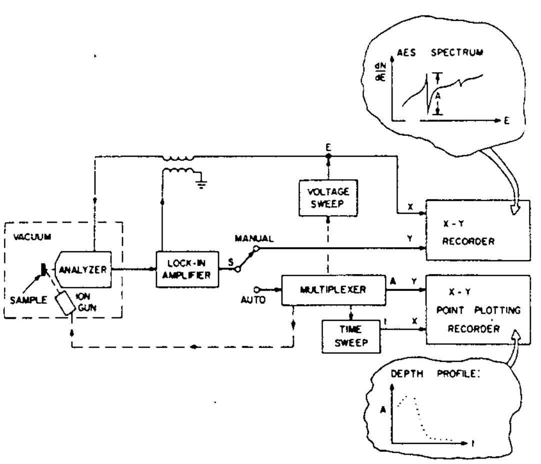


FIGURE A11.2: Schematic diagram of overall system for Auger electron spectroscopy and depth-composition profiling.

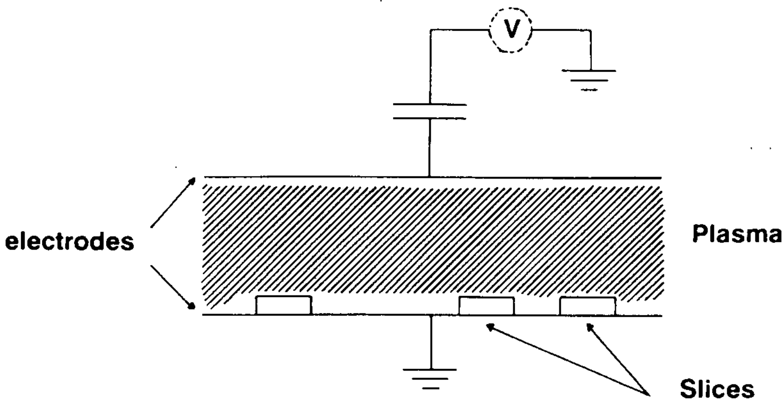


FIGURE A11.3: Simplified diagram of parallel plate, planar, plasma etching machine.

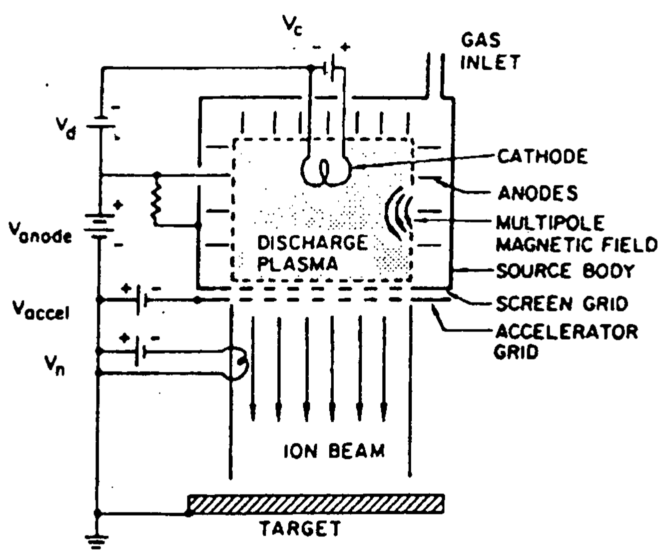


FIGURE A11.4: Simplified diagram of an 'ion beam milling' system.

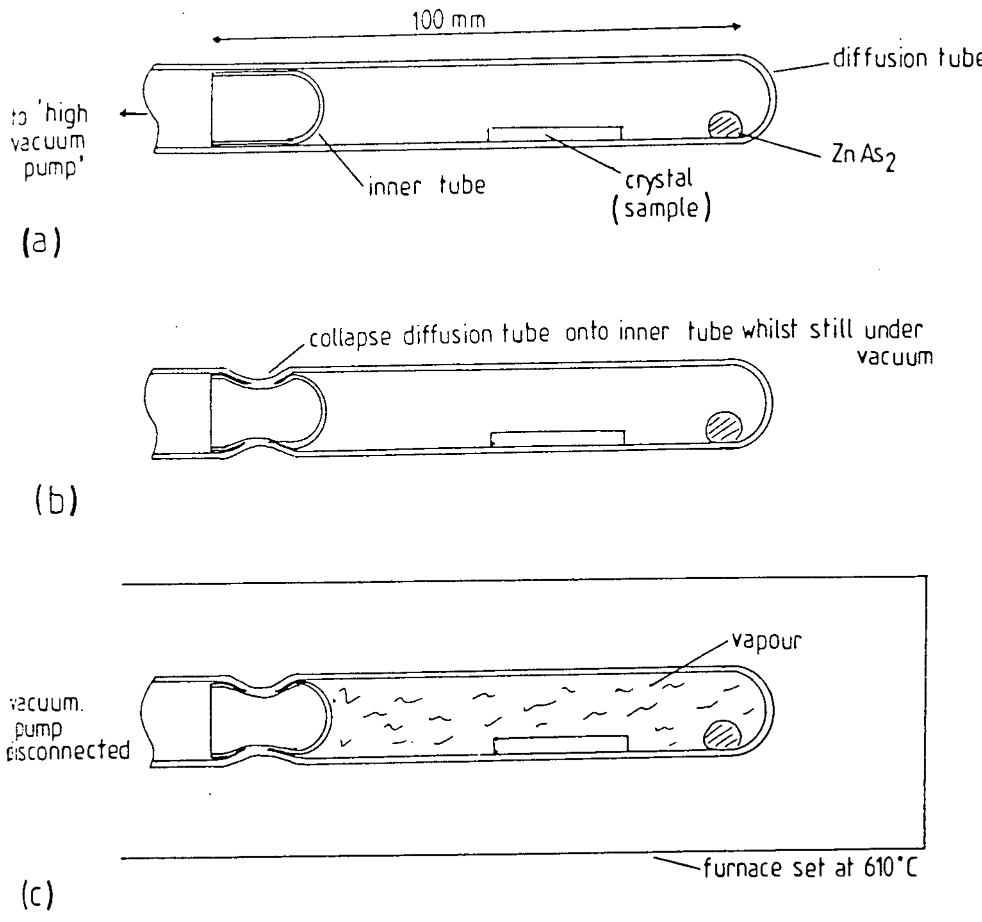


Figure A11.5: The "sealed tube method" for Zinc Diffusion.

(a) After opening the diffusion windows, the sample is cleaned, dried and loaded into the degassed diffusion tube. Pumping is immediately started.

(b) Seal tube at appropriate pressure.

(c) Load tube inside furnace for diffusion.

SOME IMPORTANT PROPERTIES OF MATERIALS

Electrical resistivity (Microhm-cm) of elements at 20°C:

Arsenic	33.3
Beryllium	4.0
Boron	1.8×10^{12}
Gallium	17.4
Germanium	46.0×10^{6}
Gold	2.35
Molybdenum	5.2
Nickel	6.84
Silicon (at 0°C)	10.0
Titanium	42.0
Tungsten	5.65
Zinc	5.92

Melting and boiling points (°C):

Material	Melting point	Boiling point
Beryllium	1278 ± 5	2970
Boron	2300	2550
Gallium	29.78	2403
Germanium	937.4	2830
Gold	1064.43	2807
Molybdenum	2617	4612
Nickel	1453	2732
Silicon	1410	2355
Titanium	1660 ± 10	3287
Tungsten	3410 ± 20	5660
Zinc	419.58	907

Coefficients of linear expansion of some metals: $[(\times 10^{-6})/(°C)]$

Beryllium:	12
Gold:	14.2
Molybdenum:	5
Nickel:	13
Titanium:	8.5
Tungsten:	4.5
Zinc:	35

APPENDIX A12

Measurement equipment and techniques:

(1) Microwave measurements performed on `HP8510 Network Analyser on Wafer Probing´.

(2) DC measurements performed on `HP4145A Semiconductor Parameter Analyser´.

(3) Sheet resistances of metal layers deposited by sputtering were measured using a `Veeco 4-point probe´, Model FPP5000.

(4) Resistivity and impurity concentrations of semiconductor layers were measured by the `Hall and Stripe´ method. A description of this method is given in "Physics of Semiconductor Devices" by S.M.Sze, Wiley-Interscience Publication, Section 1.5.2, pp. 30-34.

(5) Contact resistance measurements performed by the standard `Transmission Line Model´ technique, using `Micromanipulator Probe Station, Model 4320´ and `Thurlby Digital Multimeter Model 1504 (true rms)´.

(6) Etched depths measured using `Dektak II´.

(7) Other probe staions used:
 (i) Wentworth Laboratories Inc. Model MPO 901;
 (ii) Pacific Western Systems Inc. Model CE1.

(8) Other DC measurements performed on `Tektronix Type 575 Transistor Curve Tracer´.

APPENDIX A13

Notation used in this thesis:

XY: denotes an alloy of two elements, X and Y (eg. AuGe, an alloy of gold (Au) and germanium (Ge)).

XY(a:b w/w %): As above, with a and b denoting the respective percentages by weight of elements X and Y in the alloy (e.g. AuGe(88:12 w/w %)).

X/Y/Z: denotes a metallisation scheme with the metals deposited in the order X, Y and Z, i.e. metal X is in direct contact with the semiconductor (e.g. Cr/Zn/Au, a metallisation scheme consisting of chromium, zinc and gold; note that in some cases, X and Z may be the same metal, e.g. Au/Zn/Au).

X(aÅ)/Y(bÅ)/Z(cÅ): As above, with a, b and c denoting the the respective thicknesses of metal layers X, Y and Z in angstroms (Å) (e.g. Cr(200Å)/Zn(600Å)/Au(2000Å)).

n type: denotes a semiconductor region or layer(s) with a certain donor doping concentration; also denotes a metallisation scheme deposited onto a semiconductor layer or region doped with a donor concentration.

n^-: denotes a semiconductor region or layer(s) with a low donor doping concentration (for GaAs or AlGaAs, $n < 9 \times 10^{17}$ cm^{-3})

n^+: denotes a semiconductor region or layer(s) with high donor doping concentration (for GaAs or AlGaAs, $1 \times 10^{18} < n < 5 \times 10^{19}$ cm^{-3}).