Design of a CMOS Active Electrode IC for Wearable Electrical Impedance Tomography Systems

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***Abstract*—This paper describes the design of an active electrode integrated circuit (IC) for a wearable electrical impedance tomography (EIT) system required for real time monitoring of neonatal lung function. The IC comprises a wideband high power current driver (up to 6 mA_{p-p} output current), a low noise voltage amplifier and two shape sensor buffers. The IC has been designed in a 0.35-µm CMOS technology. It operates from ±9 V power supplies and occupies a total die area of 5 mm^2. Post-layout simulations are presented.**

I. Introduction

Each year fifteen million babies are born prematurely and many suffer from respiratory failure due to immaturity of the lung and lack of breathing control. Although respiratory support, especially mechanical ventilation, can improve their survival, it also causes injury to the vulnerable lung resulting in severe and chronic pulmonary morbidity lasting to adulthood [1]. Heterogeneity of lung aeration, resulting in areas of lung over inflation and lung collapse, plays a crucial part in the risk of mortality and morbidity due to respiratory failure. Currently available bedside monitoring and imaging tools cannot detect this distribution of lung aeration.

Electrical impedance tomography (EIT) is a non-invasive, radiation-free technique that can facilitate real time dynamic monitoring of lung aeration – recent studies have shown that it is effective in monitoring aeration in preterm babies [2] [3]. EIT images an object by injecting ac currents through electrodes on its boundary, and measuring the resulting potentials developed on the same or other electrodes. This process permits the estimation of the distribution of the inner conductivity (resistivity) of the object. EIT lends itself particularly well to the development of a neonatal lung function monitoring/imaging system in the form of wearable technology (e.g., wearable belt) that could be used at the bedside. Such a system requires the development of 'active' electrodes with the electronic circuits (e.g., current driver, voltage amplifier, sensors etc.) intimately connected to each electrode, allowing the implementation of a parallel EIT system with simultaneous recording from all the electrodes.

An active electrode for EIT is reported in [4], and an EIT system based on active electrodes is described in [5]. In these systems only the voltage amplifier using discrete components is intimately connected to each electrode. However, the current driver is also an equally important part of any EIT system. Its bandwidth defines the maximum frequency that the EIT system can measure, its output current amplitude enhances the signal-to-noise ratio of the EIT system, and a high output impedance ensures accuracy of the measurement. The commonly used Howland current driver can only offer limited bandwidth and output impedance. For a high output impedance the Howland current driver requires tight matching of resistors, which makes it unsuitable for integration.

Provision of an integrated circuit (IC) containing both the current driver and voltage amplifier intimately connected to each electrode offers good performance and small size. Such ICs for EIT applications are reported in [6], [7]. However, their output current is limited to hundreds of µA whereas for the targeted application of lung imaging currents up to 5 mA are required [2], [3]. In addition, both these designs have a relatively low operational bandwidth (100 kHz in [7] and 256 kHz in [6]) and low output impedance. A high voltage current driver IC is reported in [8] but the design is not suitable for a parallel EIT system using active electrodes.

This paper presents the design of a CMOS active electrode IC containing a wideband, high power current driver and a low noise voltage amplifier. The current driver is designed to provide an output current up to 6 mA_{p-p} and has an output impedance over 1.7 MΩ at 500 kHz. The voltage amplifier has an input-referred voltage noise of 23 $nV/\sqrt{Hz}$ at 10 kHz. Used as a unity gain buffer, the amplifier provides an output voltage swing of 14 V for signal frequencies up to 500 kHz and is able to drive large capacitive loads. The targeted wearable EIT system requires patient-specific boundary shape estimation to improve the forward model for image reconstruction. This can be facilitated by using shape sensors (e.g., stretch and bend resistors) in the wearable EIT system [9]. For this reason, two shape sensor buffers are provided on chip.

The rest of the paper is organized as follows. Section II presents the IC system architecture and Section III describes the circuit details of its building blocks. Section IV shows the performance of the IC with post-layout simulations. Finally, conclusions are drawn in Section V.

II. System Architecture

Fig. 1 shows the high level architecture of the 16-electrode wearable EIT system under development incorporating active electrodes. Each active electrode IC comprises a current driver, a voltage amplifier and two sensor buffers. The current driver has a differential difference transconductance amplifier (DDTA) followed by a wideband operational transconductance

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amplifier (OTA). The DDTA measures the output current through the sensor resistor, Rf, and forms a linear feedback. In a single EIT rotation as shown in Fig. 1(a), two adjacent active electrodes (16 and 1) are configured as the current drivers with excitation signals, Vin, provided from the central hub (not shown). One current driver is configured as a current source and the other as a current sink, both working together to form a complete current path.

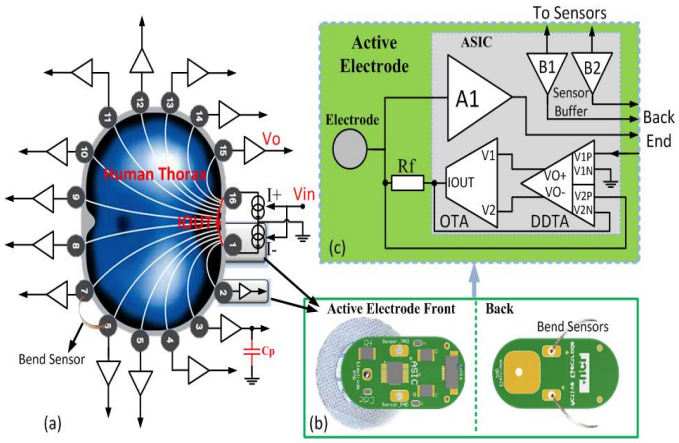

Fig.1. (a) EIT system using active electrodes with shape sensors connected; Cp is the parasitic capacitance in the cable wires. (b) Active electrode PCB incorporating the contact electrodes and shape (resistive bend) sensors. (c) Architecture of the active electrode IC where A1 is the voltage amplifier.

The excitation inputs of all the current drivers in the rest of the active electrode ICs are connected to ground (0 V), and the ICs only function as voltage amplifiers to provide the recorded voltages (Vo) to the central hub. The recorded voltage may vary from millivolts to a few volts, depending on the injected current amplitude and the electrode measurement position. Thus, the voltage amplifier requires wide input dynamic range and low-noise performance. Also as shown in Fig. 1(a), it needs to drive large parasitic capacitance loads (Cp) due to the wire connections to the central hub. For the next EIT rotation cycle, another pair of active electrodes (e.g., 1, 2) is configured as current drivers and the operation continues until all adjacent electrode pairs are used as current drivers.

The shape sensors can be connected between adjacent active electrodes. As the sensor bends or stretches its resistivity changes. Two sensor buffers in the active electrode IC can measure this dc voltage across the sensor to obtain the shape information as described in [9].

III. Circuit Implementation

A. Voltage Controlled Current Driver

The voltage-controlled current driver employs a DDTA and an OTA as shown in Fig. 1 (c), with Rf = 500 Ω (implemented off-chip for improved accuracy). The transconductance *Gm* of the current driver is

$$Gm = \frac{\text{Iout}}{\text{Vin}} = \frac{A_{loop}}{R_f + R_{load} + A_{loop}R_f} \approx \frac{1}{R_f} = 2\ \text{mA/V} \qquad (1)$$

where A_{loop} is the overall open loop gain of the current driver and R_{load} is the load.

The DDTA schematic is shown in Fig. 2. The circuit compares two differential input signals (V1, V2). Its transfer function is

$$\text{VO+} \approx \frac{\beta \times gm_1}{g_{out}}\{(V1P - V1N) - (V2P - V2N)\} \qquad (2)$$

where g_{out} is the admittance at node VO+, β is the transistor *W/L* ratio between M6 and M8, and gm_1 is the transconductance of M1. In this application, a fully differential output is provided by adding a duplicate of the output branch, so that it can be connected to the wideband OTA. Transistors MC1 to MC4 provide triode common-mode feedback for the output stage. By adjusting the bias voltage VB2, the output dc level at VO+ and VO- can be set. Transistors Ma, Mb, Mc, Md are source degenerated pairs added to increase the linear-range defined by the overlap voltage of the input pairs. Two compensation capacitors Cc are added to improve the phase margin of the current driver.

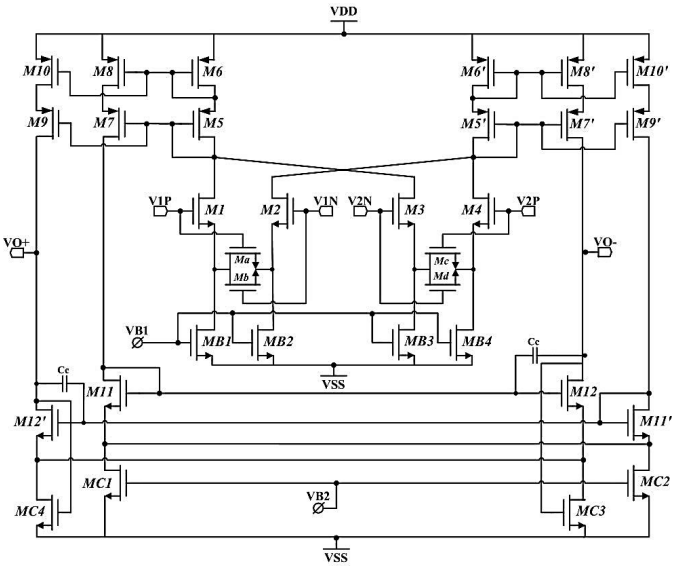

Fig. 2. DDTA circuit schematic.

The DDTA was designed for an open loop gain of 54.5 dB, a gain-bandwidth of 6 MHz with a -3 dB frequency of 8 kHz. The input linear range of the DDTA is ±2 V, sufficient to provide an output current of 6 $mA_{p\text{-}p}$ from the OTA.

The OTA schematic is shown in Fig. 3. This circuit provides wide bandwidth and large current output capability. Its transconductance is

$$\text{Gm}_{\text{ota}} = \beta \times \sqrt{2K_n I_{D1} \frac{\text{W1}}{L1}} \qquad (3)$$

where the symbols have their usual meanings. As a result of the feedback loop, the output impedance of the OTA can be expressed as

$$\text{Zout} = \left[ro_{\text{ota}} + R_f(A_{\text{DDTA}} \times Gm_{\text{ota}} \times ro_{\text{ota}} + 1)\right] \qquad (4)$$

where the ro_{ota} is the impedance node at IOUT, and A_{DDTA} is the open loop gain of the DDTA.

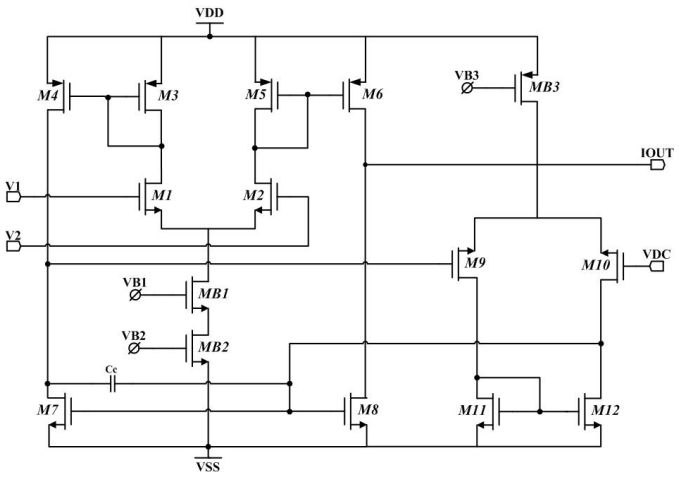

Fig. 3. OTA circuit schematic.

In Fig. 3, transistors M6 and M8 form the current output branch. Transistors M4 and M7 form a pseudo branch that can be also seen as the second stage of the differential input pair constructed by M9 to M12. This part of the circuit forms a two-stage OTA connected in unity feedback. With the input of M10 connected to a dc level (e.g., 0V), this feedback loop forces the output dc level of IOUT to be at 0V by setting the gate-source voltage of M8 accordingly. The compensation capacitor Cc improves the phase margin of this dc output regulation feedback-loop. The OTA is designed for an overall open loop gain of 42 dB and a gain-bandwidth of 142 MHz

Since the OTA has a very wide bandwidth, the bandwidth of the current driver is limited by the f_{3dB} of the DDTA. The complete current driver has an open loop gain of 61 dB, and a gain-bandwidth of 8.45MHz using Rf = 500 Ω. The current sensing resistor Rf must be accurate and is therefore off-chip. This introduces added parasitic capacitance at IOUT that reduces the phase margin of current driver. Thus the phase margin is set slightly higher than 65° by adjustment of the Cc in the DDTA.

B. Voltage Amplifier and Buffers

The schematic of the voltage amplifier is shown in Fig. 4. It is the combination of a two-stage miller OTA labelled as LNA, and a line-driver, which is necessary to drive the large capacitive load.

The two-stage LNA is designed based on [10]. With a current injection of 2 $mA_{p\text{-}p}$, the input-referred voltage noise for the LNA is in the region of 25 $nV/\sqrt{Hz}$ at 10 kHz. The line-driver is a common source push-pull buffer configuration with a shunt feedback. Transistors M1 to M4 and M5 to M8 are two error amplifiers that regulate the quiescent current in M9 and M10 and provide compensation for the loop stability. With this configuration, the voltage amplifier is able to drive a capacitive load of up to 20 pF.

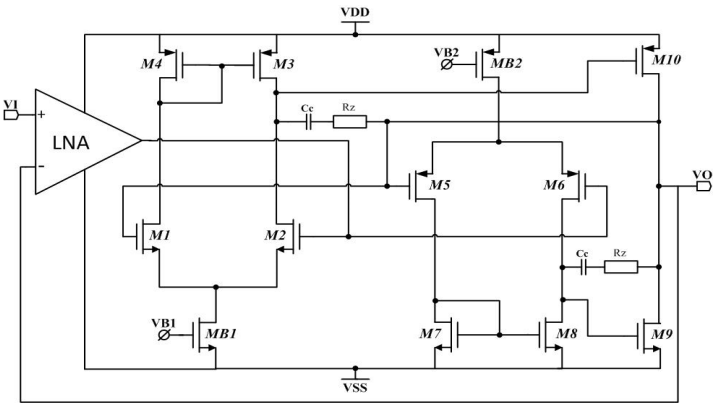

Fig. 4. LNA with line driver circuit schematic.

Each of the two sensor buffers is an OTA connected in unity feedback to accommodate a measurement range of millivolts to a few volts.

IV. Post Layout Simulation

The active electrode IC has been designed in a 0.35-µm high-voltage CMOS process and operates from ±9V power supplies. Fig. 5 shows the layout of the chip; it occupies an area of 3.1 mm × 1.45 mm. The IC is internally biased by a high-voltage bandgap block. This allows the IC to be easily integrated on small electrodes with only one feedback resistor as the external component. Switches are implemented for power-down of each circuit block to reduce power consumption by switching off blocks that are not needed (e.g., when the IC is configured as a current driver the voltage amplifiers are not needed).

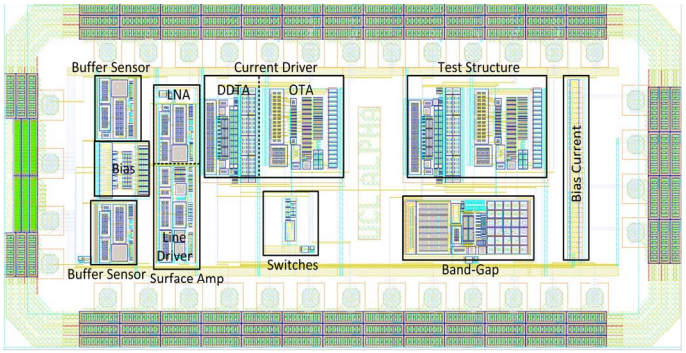

Fig. 5. Layout of the active electrode IC.

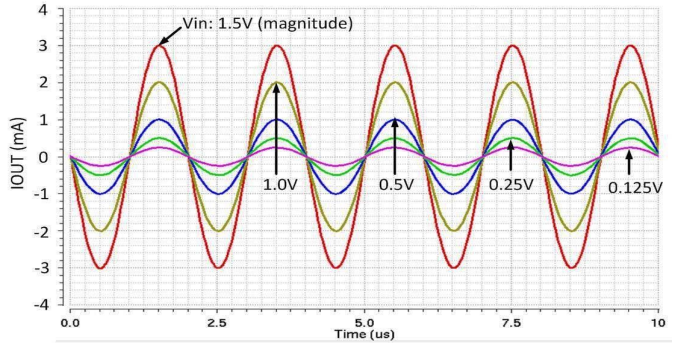

Fig. 6. Simulated output current amplitude with different excitation input voltages with a 2 kΩ resistive load at 500 kHz.

A. Current Driver

Cadence post-layout simulations have been performed on the current driver using a 2 kΩ resistive load. As shown in Figs 6 and 7, the current driver transconductance is 1.99 mA/V up to 500 kHz with a phase delay of -4.32°. The output current amplitude can reach 6 mA_{p-p}, compared to only $2mA_{p-p}$ in [8]. At 500 kHz the output impedance is 1.7 MΩ (excluding the effects of off chip stray capacitance).

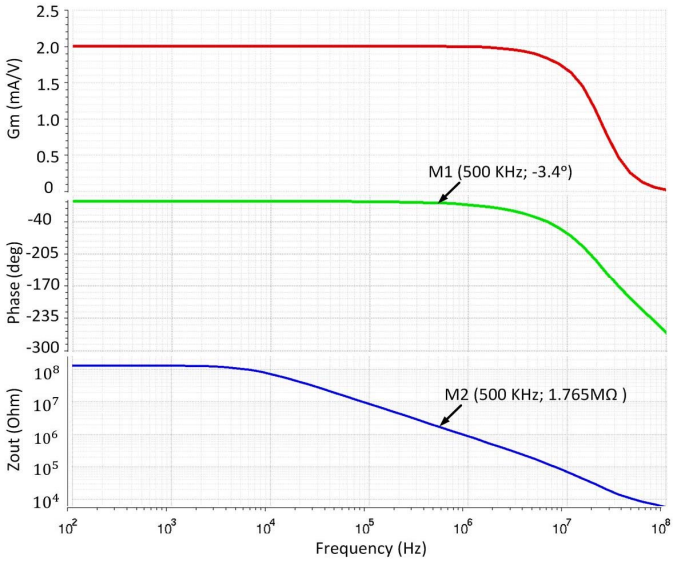

Fig. 7. Simulated transconductance, phase and output impedance of the current driver with a 2 kΩ resistive load.

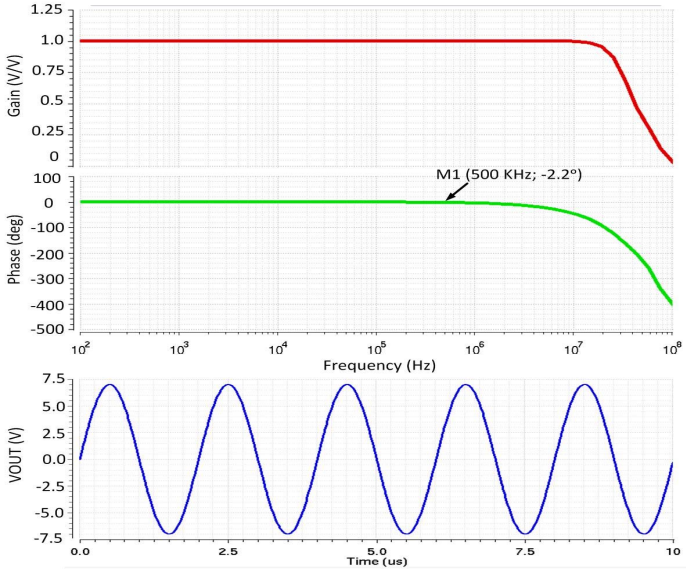

Fig. 8. Gain and phase response and transient simulation of the voltage amplifier as unity gain buffer with a 20 pF capacitive load.

B. Voltage Amplifer

Fig. 8 show the post-layout simulated results of the voltage amplifier as unity gain buffer. It has an output swing of 14 V when loaded with a 20 pF capacitive load. For stability a small resistor of 300 Ω is added in series at the output.

Table I summarizes the performance of the active electrode IC.

Table I. Active Electrode IC Performance Summary

Specification	Current Driver	Voltage Amp
Aol	61 dB	65 dB
GBW	8.45 MHz	28 MHz
PM	68°	65°
Gm/Gain	1.99 mA/V	1 V/V
Zout	1.7 MΩ @ 500 kHz	30 mΩ
Input referred-voltage noise	-------	23 $nV/\sqrt{Hz}$ @ 10 kHz

V. Conclusion

An active electrode IC has been presented. It comprises a high performance current driver, a voltage amplifier and two sensor buffers. Post-layout simulations show that the current driver is able to deliver output currents up to 6 mA_{p-p} amplitude with an output impedance of 1.7 MΩ at 500 kHz. The voltage amplifier has low noise performance, wide dynamic range and is able to drive large capacitive loads.

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