A THIN MONOCRYSTALLINE DIAPHRAGM PRESSURE SENSOR USING SILICON-ON-INSULATOR TECHNOLOGY

by

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This thesis is dedicated to
the memory of my father

ABSTRACT

The sensors market is huge and growing annually, of this a large sector is pressure sensors. With increasing demands on performance there remains a need for ultra-miniature, high performance pressure sensors, particularly for medical applications.

To address this a novel capacitive pressure sensor consisting of an array of parallel connected diaphragms has been designed and fabricated from SIMOX substrates. The benefits of this include single crystal silicon diaphragms, small, well controlled dimensions, single sided processing and the opportunity for electronics integration.

Theoretical modelling of this structure predicts a high sensitivity and low stress device with opportunities for scaling to suit alternative applications.

A novel, process technology was developed to achieve the required structure with the inclusion of procedures to address the specific issues relating to the SIMOX material.

The sensor was fully characterised and the results demonstrated high performance compared with similar reported devices. Alternative structures such as cantilevers, bridges and resonators were fabricated as a demonstrative tool to show the feasibility of this technology in a wider field of applications.

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1.0 INTRODUCTION

This chapter introduces the project, identifying the project aims and gives a brief guide to the thesis. The basic construction of capacitive pressure sensors is outlined together with the design of the sensor utilised in this work. An overview is given of silicon-on-insulator (SOI) materials, in particular, separation by implanted oxygen substrates (SIMOX) which is used here for pressure sensor fabrication. SIMOX has a silicon dioxide layer implanted between the bulk silicon substrate and a thin, monocrystalline silicon layer which forms the top surface of the wafer. The benefits offered by the proposed sensor over alternative structures are outlined, with respect to both fabrication and performance. The research is put into context by an examination of the past and present sensor and semiconductor markets along with projections for the future. The silicon material properties are outlined and a background to micromachining techniques is given. Finally a summary of the chapter is given.

1.1 PROJECT AIMS

The primary aim of this work was the fabrication and evaluation of a novel pressure sensor, suitable for medical applications, from an SOI substrate. This device is expected to display high performance, due primarily to the thin monocrystalline silicon sensing element and small, well controlled diaphragm thickness and plate separation resulting from the use of SOI material. The SOI microstructure takes full advantage of the material, by utilising solely the monocrystalline silicon overlayer for the moving element since it has improved mechanical properties compared with polycrystalline silicon. This was expected to provide substantial improvements in performance over many existing pressure sensors. A secondary aim was to design and fabricate a range of other microstructures by the same process as the pressure sensor. These structures were expected to display equally high performance and the intention was to demonstrate the wide applicability of this research.

In order to achieve these aims a full investigation into the micromachining of SOI material was conducted. A further objective was the development of a repeatable process will be developed for each step of the pressure sensor fabrication. This was expected to incorporate non-standard steps due to the combination of SOI and small

dimensions while remaining compatible with standard integrated circuit (IC) processing techniques. The pressure sensors processed in this way would then be tested under applied pressure in order to demonstrate their functionality.

A final objective was to demonstrate the potential of SOI material for the manufacture of pressure sensors and other microstructures for many applications. The multibillion pound, world-wide field of sensing and actuating, with current and projected rapid growth and continued demand for improvements to device performance gives the technology developed in this work increased significance.

1.2 PROJECT OUTLINE

A feasibility study was undertaken to test the feasibility of fabricating a pressure sensor from a SIMOX substrate using novel micromachining techniques. These include controlled wet underetching, anti-stiction rinsing and polymer cavity closure. The possible benefits of this device were examined; such as the provision of a monocrystalline silicon sensing element, single-sided etching, and the potential for integrated, isolated electronics. SIMOX was considered the most appropriate SOI substrate for use due to the maturity of its manufacturing technology, good layer uniformity and appropriate layer thicknesses. A literature survey was also conducted to identify the performance of similar pressure sensors currently reported, such that efforts could be made to fabricate a device offering improved performance.

Simple calculations were carried out in order to estimate the membrane size necessary to function in the pressure range suitable to medical applications, given the dimensions fixed by the material. Modelling was then used to investigate the behaviour of the proposed sensor with regard to sensitivity, membrane stress and breakage. Experiments were undertaken to identify several silicon and silicon dioxide etchant schemes which would provide the required control, orientation dependency and repeatability necessary to fabricate this sensor and other suspended structures. This work initially utilised silicon with a thermal oxide coated with photoresist to mimic the role of the SIMOX top silicon layer

Having selected and characterised an etchant for each fabrication step, a mask was prepared for SIMOX etching to form single isolated diaphragms. Limit testing structures were also included to provide information about undercutting characteristics, underetching maxima and achievable areas of material suspension. The novel fabrication technique developed in this work was also applied to alternative structures utilising suspended elements such as cantilevers, bridges, cogs and resonators. This was intended to emphasise the potential of these techniques to other aspects of micromechanics.

Following the fabrication and microscopic analysis of single diaphragm structures, certain changes were made to both the structure geometry and processing sequence in order to improve the yield. The technique for sealing the etch windows was also tested on these structures. A mask was then designed for the fabrication of a matrix consisting of 50 x 50 pressure sensing diaphragms, sealing plugs and metal interconnects. A variety of alternative suspended structures were included on the mask. The matrices were then fabricated, microscopically inspected and packaged. Testing was carried out using a rig built to allow the controlled application of a known pressure. The results were analysed in order to establish sensor parameters for comparison with those devices previously reported in the literature. These topics will be discussed in detail in chapter 5.

1.3 THESIS GUIDE

This thesis reports on the design, fabrication and testing of a novel capacitive pressure sensor made from a SIMOX substrate. An investigation was made of several fabrication techniques appropriate to the production of sensing devices. The benefits of a SIMOX device are examined and the relevance of the technique to alternative microstructures for other applications is demonstrated. Each chapter begins with a summary which outlines its contents and the reason for its inclusion in the thesis. They are each concluded with a summary which reviews the primary outcomes of the work incorporated in that chapter and indicates the direction of progress.

The first chapter introduces the work by outlining the project aims and describing SOI materials and the principles of capacitive pressure sensing. An overview of the range

of applications and the ever increasing market for these sensing and other semiconductor devices illustrates the importance of this work.

In the second chapter, standard micromachining techniques, such as photolithography, etching and material deposition, which are relevant to the processing used in this work, are detailed.

Chapter 3 describes the pressure sensing device which has been fabricated with regard to its design and the expected behaviour. A review of existing pressure sensing devices is given, highlighting their limitations which give opportunities for new device development where current devices prove inadequate. An analysis of the theory of capacitive pressure sensing is detailed together with conclusions from simulation work.

In Chapter 4, the experimental techniques used in the SIMOX pressure sensor fabrication and analysis are discussed, identifying the innovations made to traditional processes. The experimental methods used for determining and characterising the optimum etchants for each material removal step are detailed. This work has provided a catalogue of information on SIMOX etching for reference by future researchers. This information is not available in the literature.

In chapter five the project results are presented. The experimental results such as etch rates are detailed and the final process sequence is defined. Micrographs of the resultant structures are also included. Electrical results measured during pressure testing of the packaged devices are given, such as the pressure sensitivity and the thermal behaviour. The device performance is analysed and compared with characteristics for analogous sensors reported in the literature.

In chapter six the range of other suspended microstructures fabricated by the same process are also described, modelled and illustrated. This demonstrates the flexibility of this work.

Chapter 7 gives the conclusions of the research, presents the results and analyses its success. Opportunities for further work are also identified.

1.4 BASIC PRINCIPLES OF CAPACITIVE PRESSURE SENSING

There are two main types of silicon micromachined pressure sensor, those which sense by capacitive means and those which sense by piezoresistive means. In piezoresistive sensing the strain resulting from the flexing of a membrane under applied pressure changes the resistance within a sensitive layer. This is commonly measured by a Wheatstone bridge configuration. In 1954 Smith discovered that the piezoresistive effect is a hundred fold greater in single crystal materials such as silicon than in amorphous materials [1].

A capacitive pressure sensor consists of a cavity, covered by a diaphragm and free to move under applied pressure. The base of the cavity acts as the bottom plate of a capacitor and the diaphragm as the top plate. As pressure is applied, the diaphragm deflects, bringing the two plates closer together. This increases the overall capacitance of the sensor.

This change in capacitance under an applied pressure is measured and related to the value of the pressure, resulting in a pressure measurement system. The relationship between capacitance and applied pressure is dependent on the diaphragm geometry and method of support.

By connecting several micromachined pressure sensors together to form an array, a larger electrical signal can be obtained for a particular pressure change. The disadvantage is the increase in sensor dimensions and complexity. In the design of a capacitive pressure sensor, several parameters such as plate separation, thickness and area, may be used to adjust the sensor's functional pressure range. Furthermore, the plate separation may be chosen such that, at a particular pressure, the diaphragm and cavity base actually come into contact. The device will then operate as a switch, which can also be manufactured as an array, with each element of the system switching at the same or different applied pressures.

A capacitive design was used in the present work, since typical performance is considered superior to piezoresistive devices for low pressures and temperature insensitive measurements. The capacitive pressure sensor structure in this project is formed by the removal of a section of the buried silicon dioxide from the SOI

substrate, via a window in the top silicon. The window is then plugged to form a continuous diaphragm free to deflect above a cavity.

Starting with the SIMOX substrate a cavity is formed by the removal of a section of the buried oxide by wet chemical underetching through a small window in the silicon overlayer. The single crystal silicon layer surrounding this window forms a diaphragm above the cavity. A photoresist 'plug' is used to seal the cavity. Metal electrodes and interconnections are then deposited to allow device capacitance measurement. This structure is shown in figure 1.1. An applied pressure deflects the diaphragm, as a result of which the capacitance between this and the substrate changes.

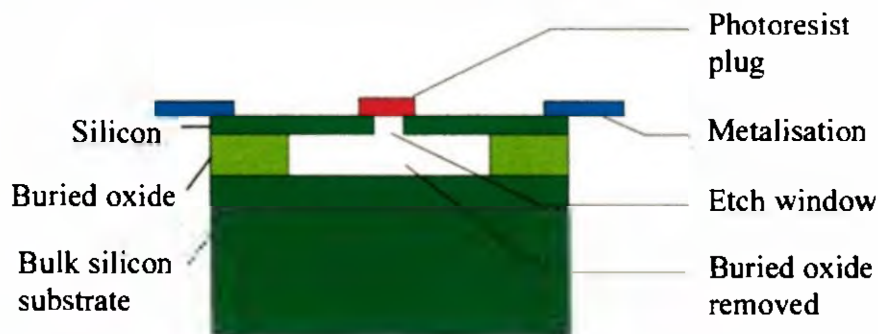


Figure 1.1 Sensor Structure.

1.5 SILICON-ON-INSULATOR (SOI) MATERIALS

Silicon-on-insulator (SOI) material consists of a top single crystal silicon overlayer separated from the single crystal silicon substrate by a buried silicon dioxide layer (BOX) (except in the case of silicon-on-sapphire, see section 1.5.1.1). SOI substrates have been under development for 20 years with increased interest and volume production in the 1990's. Towards the end of the century, as more devices which are unrealisable in bulk silicon are developed on SOI, the market potential for this material, and structures made from it, is expected to grow. Despite the expense of the material, the overall process costs generally remain comparably low. Currently an 8" SOI wafer costs $200 compared to $120 for standard silicon. SIMOX technology has reached a high degree of maturity, producing SOI wafers with a top silicon quality close to standard bulk silicon wafer specification. The ability of implanter manufacturers to produce equipment will enable sufficient SIMOX to be made to

satisfy predicted SOI growth. To achieve the predicted future demands with low dose production just 50 implanters would be needed by the year 2000 [2].

The fundamental benefits of devices fabricated on SOI over those on bulk are derived from the dielectric isolation which provides radiation hardness, reduced junction capacitance and allows smaller components resulting in higher integration densities. SOI circuits have been demonstrated operating up to 50 % faster than their bulk counterparts. Complimentary metal oxide semiconductor (CMOS) circuitry on SOI also has the advantages over bulk of elimination of latch up and reduction in parasitic capacitances [3]. High performance MOS and bipolar devices have been demonstrated on SIMOX substrates [4] and CMOS devices have been reported operating at speeds twice that of similar bulk devices [5]

1.5.1 SILICON-ON-INSULATOR MATERIAL TYPES

There are several different methods for fabricating SOI, resulting in material of different cost and quality which hold different benefits for different applications. The most common SOI substrates are described below, along with their methods of production, an analysis of the substrate quality and an indication of their applications. A more detailed comparison can be found in [6].

1.5.1.1 SILICON ON SAPPHIRE (SOS)

SOS consists of a thin film (0.1 - 0.5 um) of single crystal silicon, on an insulating sapphire substrate as shown in figure 1.2. Developed in the 1960's and utilised for military applications, SOS has remained a niche market [6]. Material problems are crystalline quality, unsuitability for batch fabrication [7], high production costs and imperfections in the silicon layer resulting from the mismatch in lattice constants between silicon and sapphire.

Figure 1.2 SOS Material Structure.

1.5.1.2 BONDED, ETCHED-BACK SILICON-ON-INSULATOR (BESOI)

This material has a single crystal silicon overlayer on a silicon dioxide layer on a single crystal silicon substrate as shown in figure 1.3. It is formed by bonding two standard silicon wafers, at least one of which has previously been oxidised. The two silicon wafers are brought into contact (with the oxidised surface facing the other wafer) at room temperature or above and annealed at 800 - 1100 °C, to form a strong bond. The top silicon wafer is thinned by grinding, polishing or etching (using an implanted dopant etch stop which is subsequently dissolved). The defect density and electrical properties of the resulting silicon overlayer are unchanged from bulk. However, disadvantages of this material are the occurrence of voids or bubbles during bonding and difficulty in producing layers less than 300 nm thick [6].

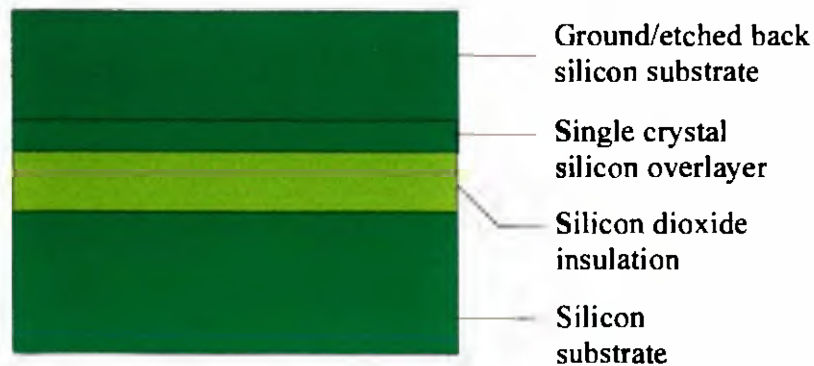


Figure 1.3 Bonded Etched Back Process for SOI Formation.

1.5.1.3 ZONE MELTING RECRYSTALLIZATION (ZMR)

This consists of a single crystal silicon substrate, silicon dioxide insulating layer and a recrystallized silicon overlayer as shown in figure 1.4. In production a polysilicon layer, followed by a silicon dioxide capping layer, is deposited on a thermally oxidised silicon wafer. The polysilicon layer is then locally melted using a linear heat source which recrystallises the layer in a single scan. Preheating is used to avoid fracture and defect initiation, the resultant defect density is 10^5 cm^{-2} [6]. An advantage is the ability to recrystallise several silicon layers at one time, separated by insulating layers, but low yield and heat conduction can result [6].

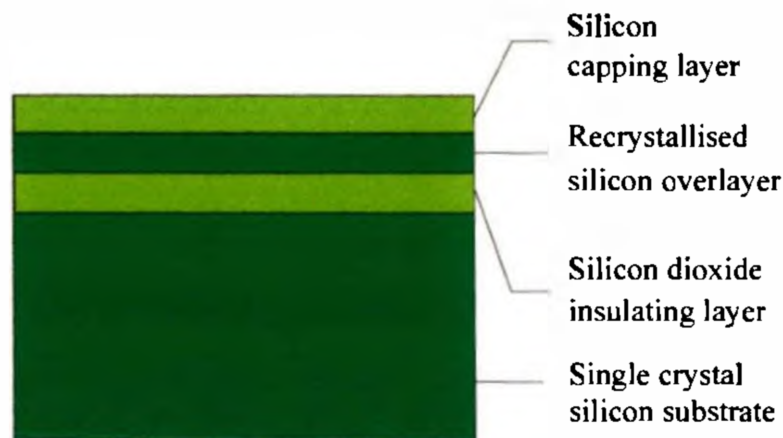


Figure 1.4 ZMR structure.

1.5.1.4 SMART CUT SOI

This material with a single crystal silicon substrate, silicon dioxide insulating layer and single crystal silicon overlayer as shown in figure 1.5 is manufactured using heat induced micro slicing [8]. Hydrogen is implanted into a thermally oxidised wafer at a dose of 2×10^{16} - 1×10^{17} cm^{-2}. This wafer is then bonded by its oxide surface to a second substrate at room temperature. The assembly is heated to 400 - 600 ^{o}C, where it splits at the point of the mean hydrogen ion penetration depth.

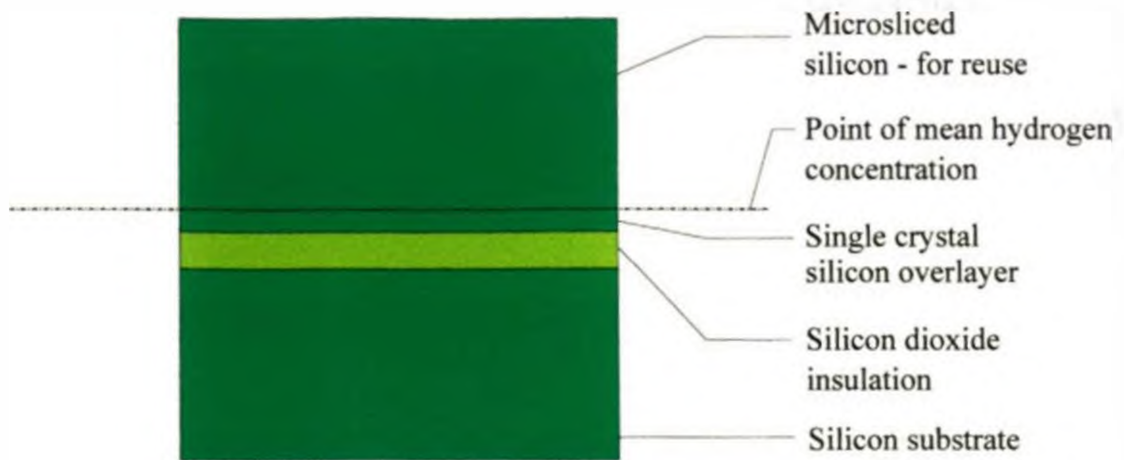


Figure 1.5 Smart cut production of SOI.

1.5.1.5 FULL ISOLATION BY POROUS OXIDISED SILICON (FIPOS)

FIPOS material has a monocrystalline silicon overlayer on buried silicon dioxide, on a single crystal silicon substrate [6]. A layer of porous silicon is produced by anodization in HF. The porous structure comprises many branches and sub branches which meander into the wafer from the surface. The diameter of the pores varies widely. Selective oxidation of the porous silicon is used to manufacture the SOI substrates. This oxidation is a low temperature, high speed process due to the large surface area of the porous silicon.

1.5.1.6 SEPARATION BY IMPLANTATION OF OXYGEN (SIMOX)

This material typically consists of a 0.2 µm thick monocrystalline silicon overlayer on a 0.4 µm thick layer of implanted silicon dioxide on a single crystal silicon substrate as shown in figure 1.6. A high oxygen ion dose (1.5×10^{18} - 2×10^{18} cm^{-2}), at a temperature above 500 °C is used to form the oxide layer below the surface of a silicon substrate. Annealing is carried out at 1300 °C for 6 hours. This dissolves silicon dioxide precipitates and reduces defects in the top silicon layer. Good control of the implantation dose, direction and energy produces good quality material.

The implanted material allows the thinnest silicon layers of all SOI technologies, combined with good uniformity, controllability and reproducibility. The disadvantages of this technique are the requirements for high ion dose, long implantation time, resultant high cost and heavy metal contamination (< 10^{17} cm^{-3}). Implanted samples can be examined using Rutherford backscattering (RBS), secondary ion mass spectroscopy (SIMS), transmission electron microscopy (TEM) in addition to these, Auger and X-ray photospectroscopy can be used [9]

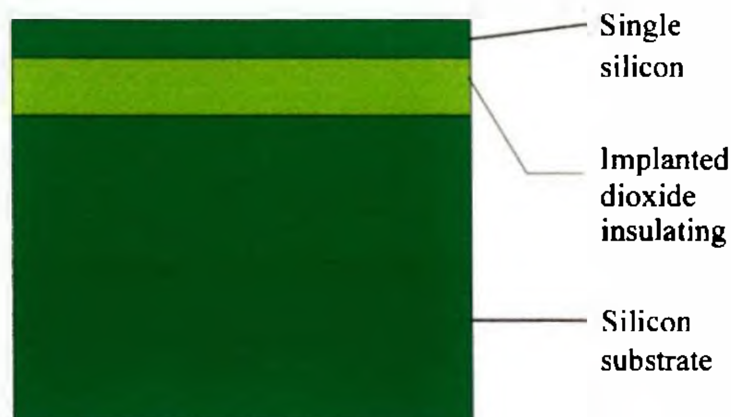


Figure 1.6 SIMOX structure.

1.5.2 SIMOX DEFECTS

Defects may arise in the silicon overlayer, buried oxide or at the interface between them. When large numbers of defects are present, devices show inferior electrical performance [10]. However in this project the SIMOX is being used as a platform for a mechanical device and in this case we would not expect the integrity of the performance to be affected to a great degree by this defect density. In essence the diaphragm performance will be close to one of ideal monocrystalline silicon which exceeds that of a polycrystalline diaphragm. Elevated temperature implantation has also been used to retain a high degree of surface crystallinity [11]

The buried oxide differs from thermal oxide in several ways [12] again this is not expected to degrade the sensor performance. Structural and stoichiometric differences are evidenced by a difference in the etch rates observed between thermal and implanted oxides [13]. The lower BOX etch rate is thought to be due to structural

differences such as densification. Local fluctuations in the BOX etch rates have also been observed, thought to be a result of film inhomogenity [13]. The implanted oxide takes on a Gaussian profile [14]. A slower etch rate has been observed at the maximum of the Gaussian oxygen implant profile, where the most dense material is likely to be [15].

Following the anneal step, silicon islands with well formed facets with the same orientation as the substrate have been detected in the BOX [16]. If silicon pipes in the oxide exist which connect the top silicon to the substrate this would result in a problem in sensor performance, however no evidence of this was seen in the measurements which were made.

Standard SIMOX has a density of dislocations and other defects $< 10^6$ cm^{-2}. Typically, approximately 2 % of the BOX volume is actually silicon [17].

Various adaptations of the standard SIMOX production process have been reported which can produce lower defect density material [2, 3, 17, 18], the resultant substrates having advantages for some applications but were not thought to be necessary in this work. Examples of these processes are multiple implantation [17], reduced energy implantation [18], combined oxygen and nitrogen implantation [3] and low dose implantation [2]. It has also been reported [19] that an oxygen dose four times lower than in standard SIMOX can be used to provide an effective etch stop for the batch fabrication of membranes.

1.5.3 SILICON-ON-INSULATOR APPLICATIONS

Applications for SOI devices are constantly being developed causing the substrates and technology to be more accessible. The specifications for SIMOX are now close to those of bulk silicon and the price has become more competitive as a result of its use in mainstream ultra large scale integration and power devices. The first SOI applications were radiation hard devices such as SRAM's for military use, where they replaced SOS designs [20]. SOI devices display a lower sensitivity to transient radiation than bulk. Microwave devices and optical waveguides have now been demonstrated in SIMOX material [20]. Other SIMOX structures have demonstrated a

current leakage three to four orders of magnitude smaller than equivalent bulk devices together with a reduction in threshold voltage variation [21]. Well logging, automotive, aircraft and commercial nuclear applications require devices to operate at temperatures restrictively high for bulk technology. However, SOI SRAM's have been demonstrated operating up to 300 °C and ring oscillators up to 500 °C [21], indicating that SOI devices could be suitable for these high temperature applications. The SOI benefits are evident at every scaling level; 0.5 μm scale SOI devices have comparable performance to those made in bulk 0.35 μm scale technology [20]. High speed devices have been shown on this material with a 10 year lifetime [21].

For sensors, SIMOX provides the opportunity for integration of the mechanical component with electronics to produce smart devices displaying improved mechanical and electrical stability over their bulk counterparts particularly at high temperature [21]. For this reason the above passage has been included to demonstrate the ability to produce high performance electronics from SIMOX material in addition to mechanical structures. Ultimately the pressure sensor fabricated from SIMOX could be integrated with electronics to provide improved performance.

Silicon-on-insulator material is expected to make possible a new generation of sensors employing single crystal silicon technology with performance advantages such as high sensitivity, freedom from hysteresis and creep, high temperature range and a micromachining capability. The SOI layering, providing insulation and etch stop facilities gives added value. Some of these features are exploited in the SIMOX pressure sensor designed in this project. The benefits the device will offer over conventional designs are considered to justify the used of the higher cost starting material. An example, a SIMOX piezoresistive pressure sensor with impressive performance has been reported by Diem [7]. It displays improved temperature sensitivity and reduced parasitics, compared with bulk devices. This sensor has been operated at up to 400 °C. No effects such as stress or temperature leakage currents were observed following 100 hours of high temperature cycling. An infrared thermal sensor has also been fabricated, from SIMOX and operates successfully operates at elevated temperatures [22]. A final example of a SIMOX sensor is a light modulator, made using standard IC technology. The SOI substrate allows a monocrystalline silicon bridge to be used which gives the device a high sensitivity [23].

1.5.4 SUMMARY OF SOI MATERIAL POTENTIAL

In summary it can be seen that the general benefits of SOI devices include reduced masking levels, reduced power and increased operation speeds. Some SOI device performance has been shown to be much improved over bulk silicon structures, outweighing the higher material costs. For sensors, SOI can allow the combination of the excellent mechanical properties of single crystal silicon sensing elements, with integration possibilities. SIMOX is currently the most advanced SOI technology and as the material quality improves so its applications increase. From initial niche military uses, several devices have now been demonstrated on SIMOX for a variety of applications, including high performance sensors.

1.6 ADVANTAGES OF THE PROPOSED PRESSURE SENSOR

The capacitive pressure sensor investigated in this project uses SIMOX, an SOI substrate, as a starting material. The main features of the pressure sensor are its capacitance measurement method, the monocrystalline silicon diaphragm, the scope for single sided fabrication, avoidance of etch stop or sacrificial layer formation, a thin, uniform diaphragm, small plate separation and the circular diaphragm design.

As previously outlined, a primary application of pressure sensors, with increasingly stringent specifications, is medical engineering. Solid-state piezoresistive devices have been marketed for roughly 20 years [24] to perform, for example, arterial pressure measurements. These systems measure accurately dynamic pressure changes but do not perform well for long term measurements of low pressure [24], typically suffering a drift of 100 Pa per day. A possible solution is a fluid-filled catheter, coupled to a precise manometer system outside the patient, but this is cumbersome, restraining to the patient and unsuitable for telemetry applications [24]. Furthermore, the limited power available for internal sensing makes the use of piezoresistive devices difficult, especially for long term continuous monitoring and implantable systems. These considerations support the development of a capacitive type pressure sensor for biomedical analysis. The combination of the SIMOX starting material with novel undercutting techniques, results in a structure with improvements over traditional capacitive sensors particularly for medical applications.

Capacitive pressure sensors potentially offer a higher sensitivity and lower power consumption than the piezoresistive type as shown in table 1.1. Piezoresistive pressure sensors display high temperature drift and diaphragm thicknesses is limited by the junction depth required for diffused resistors, thus limiting their ability to measure in lower pressure ranges [25]. Furthermore the relative change in resistivity of a piezoresistor yields a 10 - 20 times lower sensitivity than that from the change in capacitance of a capacitor [26].

Property	**Capacitive**	**Piezoresistive**	**Reference**
Pressure sensitivity	14 % - 10's of %FS	<1 %FS - 1 %FS	[27, 28, 29]
Thermal sensitivity	100 ppm / °C	2000 ppm / °C	[30]
Full scale dynamic range	50 %FS	1 %FS	[30]
Burst pressure	1000 xFS	10 xFS	[29]
Power consumption	100 μW	10000 μW	[31]
Stability	0.3 mmHg / mo.	1 mmHg / mo.	[31]
Temperature drift	almost temperature independent	can be 600 %	[29/31]

Table 1.1 Comparison of the performance of capacitive and piezoresistive pressure sensors.

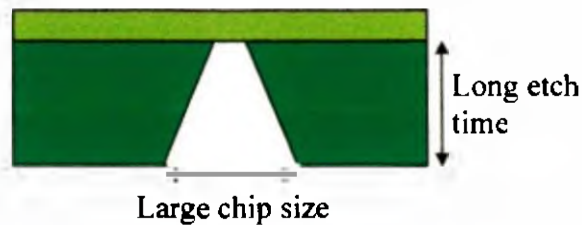
A fundamental benefit of the SIMOX pressure sensor design is the use of monocrystalline silicon as the diaphragm material. Most current devices use a diaphragm composed of either polycrystalline silicon or a silicon compound e.g. silicon nitride. Monocrystalline silicon exhibits superior physical characteristics as a mechanical component. For example, it displays high mechanical strength which is not degraded with repeated stress and the mechanical and thermal properties of single crystal silicon are not dependent on prior processing [32]. Polycrystalline silicon is composed of small grains of silicon crystals separated by grain boundaries [33]. When employed as a diaphragm, polysilicon shows a low flexibility due to these grain boundaries. Polycrystalline silicon also has a strong dependence on its deposition parameters which are not easily controlled. This causes variable performance.

Polysilicon deposition itself can be problematic to optimise [34]. In the case of polycrystalline silicon, the maximum dimensions of suspended structures are limited due to the internal residual stress resulting from deposition. Subsequent to release, structures will often curl and/or fracture, limiting the dimensions of bridges and cantilevers [35]. Although high temperature annealing can be used to reduce this problem, this then restricts the integration of electronic circuitry during fabrication. Contrastingly single crystal silicon yields virtually stress free structures, facilitating larger suspended elements which provide improved mechanical sensitivity [35]. The sensitivity of a polysilicon diaphragm pressure transducer is typically half that of a single crystal silicon device of equal diaphragm size. When silicon dioxide is employed as the mechanical component of a sensor, layers are formed in growth which shift during operation. This can lead to sudden changes in the apparent zero position - one of the most difficult errors to compensate for in many sensing applications.

Some of these problems with polysilicon sensing structures can be overcome by using silicon-on-insulator substrates. The SIMOX pressure sensor does not suffer from a mismatch of thermal expansion coefficients between diaphragm and substrate since they are the same material. Many other devices experience mismatch which leads to stress resulting in complex deflections, warpage and subsequently device failure [36]. This mismatch is a particular problem in pressure sensors bonded to pyrex. Other sensor types also favour the use of monocrystalline silicon, for example its Seebeck coefficient is twice that of polycrystalline silicon, a factor utilised in a SIMOX thermopile [22] and a single crystal silicon piezoresistive element has higher sensitivity of one fabricated from polysilicon [34].

The use of SIMOX material, combined with novel micromachining techniques, allows fabrication using only the front side of the wafer. As a result of this the chip has increased mechanical strength and reduced size [36] as shown in figure 1.7. Furthermore lower processing times are required compared with back etched designs [37] where typically almost the thickness of the entire wafer is removed in certain areas of the device.

(i) Back etched design:



(ii) Front etched design:

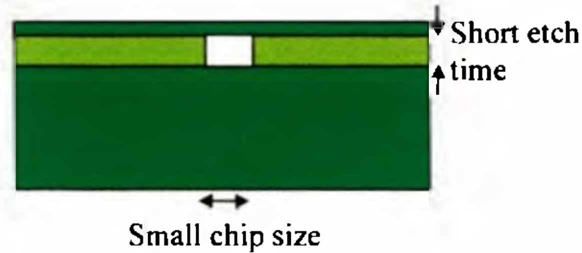


Figure 1.7 Comparison of (i) back and (ii) front etched designs.

The layering of the SOI material forms natural etch stops. For example, a silicon specific etchant will stop etching or drastically drop in etch rate on reaching the buried oxide layer. This avoids the need for:

(i) doping - which results in large lattice strains in membranes owing to the high dopant concentrations required [38];

(ii) electrochemical control - which can suffer from resistive voltage drops resulting in etch non-uniformity and junction leakage current causing a premature stop to etching [39].

In addition, the high quality of the interfaces of the SIMOX material layers leads to accurate control of the diaphragm thickness and plate separation resulting in good pressure range control of the final device.

The composite material also avoids the need to form a sacrificial layer prior to microstructure fabrication. This would be carried out either by material growth, which is time consuming, or by silicon fusion bonding, which requires specialised equipment, consumes two silicon wafers and can result in low yield due to void formation [40].

The fabrication techniques allow devices of very small sizes to be made, incorporating an ultra thin diaphragm which gives high sensitivity. The small, controlled plate separation inherent in this design increases the device sensitivity and can allow the cavity floor to act as a stop when overpressures are applied. Literature suggests that devices employing this feature can withstand overpressures of up to 500 psi [41]. As previously suggested, this plate contact could actually be exploited as a sensory feature for switching devices. A circular membrane is used in the SIMOX sensor rather than a square design in order to increase the ease of fabrication and the pressure at which rupture occurs [26]. Circular membranes have a higher resonance frequency than square ones, but do suffer from lower sensitivity.

In addition to the intended medical applications of the device, uses of pressure sensors are numerous e.g. automotive, aerospace and process control. By choice of diaphragm dimensions or SIMOX starting material characteristics, for example by epitaxial growth to thicken the top silicon, the design can be adjusted to facilitate the measurement of different pressure ranges for alternative applications. Once optimised, the technology demonstrated by this project will be applicable to the fabrication of not only pressure sensors, but many other microstructures for physical sensors such as resonators, accelerometers, vibration and optical devices, leading to an even more diverse range of application fields.

1.7 APPLICATIONS AND MARKETS

The world's ever increasing need for higher performance, moderately priced sensors is illustrated in the following sections. These outline the numerous applications and exceptional market growth in the field of sensing. The enormity of the sensors industry demands continued research and justifies interest in such novel methods as the SIMOX pressure sensor fabrication.

1.7.1 SENSOR APPLICATIONS

The formation of a suspended member above a cavity plays a fundamental role in the design of many sensing structures. The work undertaken in this project has therefore

not only allowed diaphragm structures to be fabricated for the measurement of pressure but a number of associated structures have also been demonstrated, using the same fabrication methods. This technique results in a suspended, sensing element which, unlike many alternative designs is constructed of single crystal silicon, fully exploiting this excellent mechanical material. Polysilicon is commonly used in reported devices as the sensing element material [42], a comparison of the properties of poly and monocrystalline silicon is given in table 1.2. This is separated from the substrate by an insulating silicon dioxide layer which increases the versatility of the fabricated structures. Static and dynamic capacitive membrane sensors can be realised using this SOI technology, along with damped and undamped cantilever structures and diaphragm arrays for pressure and tactile sensors. Cantilevers are used in many applications including chemical, force and vibration sensors [35]. Many other microstructures can be fabricated to allow the manufacture of flow, displacement and temperature sensors, vibration measurement devices, microswitches, micro-valves, bridges, rotors, and resonators [43]. This work could therefore form the basis for the development of a new technology important to the micromachining industry as a whole, and to the applications reliant upon it.

Property	**Monocrystalline silicon**	**Polycrystalline silicon**
Density / gcm^{-3}	2.33	2.6
Toughness / $MPam^{1/2}$	0.95	0.75
Gauge factor	-102 to + 135	-30 to + 40
Hardness / GPa	10.2	4.9
Elastic constant / GPa	186.5	130.5
Young's modulus / GPa	190	167
Poissons ratio	0.06	0.22

Table 1.2 Comparison of the properties of mono and polycrystalline silicon [39, 44, 45].

The range of sensor applications is constantly growing and extends into every sector of life. Sensors can be manufactured with a high degree of versatility with regard to measurement range and application environment, for example for specialised purposes such as operation in high temperature or harsh chemical environments [46]. Increasing attention is being given to multiple sensor systems where many identical or different

sensors are interconnected to form one device. These and multi parameter sensors increase further the application opportunities and provide cost benefits. Capacitive based pressure sensors often have an output of the order of femtofarads (fF, 10^{-15} F) making the integration of signal conditioning electronics necessary [47]. This is called smart sensing and requires divergence from the traditional analogue output [48]. The incorporation of sensor electronics can also facilitate testing, calibration, cancellation if cross sensitivities and control functions [49]. Integrated sensors can process information or communicate with a microprocessor, actuators can also be smart or the entire system can be integrated to form a microrobot. These electronic additions do, however, present concerns for their long term resistance to the harsh environments common in sensor applications. Other problems include sensor heat dissipation adversely affecting the integrated circuitry and complications in the packaging where the sensor requires exposure to an environment while the electronics requires protection from it.

Domestic sensors are in their infancy, with applications including load and temperature sensors for washing machines, and humidity and temperature sensors for microwave ovens in addition to chemical sensors to monitor the level of "browning gases" [50]. Other domestic appliances utilising sensors include video and CD players, lighting and security systems. Office automation is another growing field for sensor implementation, and is currently the largest application area for photomicrosensors [51].

The increasing concerns for environmental protection, in such issues as global warming and ozone depletion together with localised considerations for quality of drinking water and urban air, are leading to the emergence of a multi-million pound market for environmental sensors [52]. An environmental sensor is defined as a sensor monitoring or controlling the environmental state [53]. In the UK, many applications have arisen in response to legislation or European Union laws. The 1972 European Summit Conference in Paris led to the introduction of a range of environmental policies and laws covering, for example, the emission of toxic gases, incineration, quality of drinking water and composition of industrial discharge [53]. In some cases quantities are measured which are not pollutants themselves but indicators of pollution. Research has shown that some carcinogenics, for example can be absorbed into certain particulate materials such as diesel soot [53]. Therefore capabilities likely

to be required from particulate monitors in the future include the ability to quantify and categorise (by size and chemical species) the particulate materials in a sample. The industrial gas sensors market enjoyed moderate growth from 1992 – 1995 with projections indicating a growth for the US market from $443 million in 1996 to $525 million in 2002 [54]

Liquid monitoring can sometimes be carried out more accurately and cost effectively using existing analytical methods rather than sensing devices. These are more necessary when monitoring is required at, or near to the point of discharge. The National Rivers Authority carries out 4.3 million analyses a year, of which only 5 % use sensors and it is predicted that this figure will never exceed 10 % [53]. Nevertheless a single analysis for some complex organic compounds, such as dioxins, can cost up to £1k using laboratory techniques. Since legislation is only effective if realistic technologies exist to enforce it, there is good reason to investigate sensing techniques for such areas which are currently not feasibly measurable. The 1990 Clean Air Act Amendments implicate 189 chemical species as health threatening [53], but a survey by Kelly [55] showed that only 126 of these have suitable methods for sampling and analysing them.

Alternatively air monitoring is usually carried out using sensors since it is (a) a fairly recent practice, (b) often required at source and (c) involves only a limited number of species. Economic factors are important for on-going analysis and these are not just equipment costs as highlighted in a recent Severn-Trent Water survey [56]. This found that costs, for the 5 year lifetime of on-line aluminium monitors could be as much as 282 % of their purchase price.

The automotive industry is one of the major markets for sensors. Applications of just one sensor type, the Hall sensor, are numerous [51] including position and speed monitoring, proximity and limit switching, and level/flow rate monitoring within gear wheels, drive shafts, anti-lock brakes, crankshafts, manifolds and camshafts. In the US, air bag sensors are already in high volume manufacture driven by the demands of large automotive companies [57].

The measurement and control of manufacturing processes make extensive use of sensors in, for example, hydraulic systems, paint and agricultural spraying,

compressing, refrigeration, heating, ventilation and air conditioning, water level measurement and telephone cable leak detection [58]. The monitoring of machine vibrations with accelerometers is used to predict equipment failure.

Other less mainstream applications for sensors include the control of scuba diving equipment, barometric and diving watches, fitness equipment and even sports shoes with cushioning adjusted by internal air pressure controls! [58]. An interesting future possibility exists for an electronic 'nose', incorporated into washing machines to assess the cleanliness of clothes [50].

Although silicon technology is successful in sensing in many fields of sensing, it has shown specific promise in both precision and low accuracy (low cost) pressure sensing. Important areas for the employment of pressure sensors are automotive engineering, process control, telecommunication and aerospace. Environmental monitoring and medicine were relatively untapped areas but are now growing, holding great potential for the future [50]. Consumer applications generally need a short implementation cycle but may then dominate the market in the next decade. In contrast, aerospace, military and avionic applications need long development times to meet the stringent operational specifications. As older applications become obsolete, new marketing opportunities are constantly created. New areas in automotive pressure sensing are being led by demanding performance requirements. These include manifold absolute pressure sensors (MAP's), oil and tyre pressure controls and smart suspension systems [58]. For silicon to retain its importance in the field of sensing, for new and old applications, continued research into traditional and novel methods is essential.

1.7.2 MEDICAL APPLICATIONS

Extensive advances in microelectronics technology have created opportunities for high performance, reliable measurement and control systems for improved biomedical research and health care. Biomedical sensors and actuators not only need the high sensitivity, selectivity and time stability of industrial devices but also require miniaturisation and reduced power consumption [59]. For implantable sensors, bio-compatibility is critical [60]. There are three categories for medical devices, 'in vitro'

where a body sample is removed for analysis, 'ex vivo' where a body sample is continuously removed and monitored and 'in vivo' in which continuous internal monitoring takes place [61].

For implant applications where communication between the biological system and outside is required, device packaging must be compatible with body tissues and resistant to corrosion by body fluids. Leads and signal processing circuits must also be insulated from these fluids which are conductive. One method reported for achieving this uses anisotropically etched back contacts, such that the lead connections are not exposed to the sensor environment [59]. Miniature sensors which are designed for operation in the hostile body environment are often unsuitable for mass production, and limited by problems with long term stability.

There is currently a market opening for in dwelling sensors for continuous patient monitoring. These are required urgently by clinicians. In a recent survey [61] other medical applications requiring research were identified, including: monitoring of urine for dialysis patients, anaesthetic gases such as carbon dioxide (CO_2) and blood sugar level measurement for diabetes patients - possibly linked to an insulin dispatch system. Blood pressure, salt level, heart rate and breathing monitoring would all be advantageous for providing extensive information on a patient's general state of health. Currently there are only a few examples of commercial, medical pressure sensors such as a disposable blood pressure sensor [46], an intrauterine pressure sensor for use in childbirth and a sensor for angioplasty pressure measurement inside a 'balloon' for insertion in a blood vessel [58]. Other clinical sensing devices include glucose sensors and blood pH sensors which are ion selective field effect devices [50]. In the near future, instruments for hormone level measurement and diagnosis using smell sensitive arrays are expected to be developed.

Current targets for micromachined sensor technology to facilitate advanced health care are [59]:

(i) Intelligent sensor systems with built-in logic, computing, data acquisition and analysis functions.

(ii) Complex systems for the measurement and correlation of related parameters to analyse and project a patients complete condition.

(iii) Continuous on-line monitoring for the critically ill.

(iv) A reduction in the invasive nature of patient monitoring.

(v) Patient care outside hospitals.

(vi) Closed loop control of prostheses and therapeutic systems.

Devices which are intended to achieve these targets are detailed in table 1.3, along with their areas of application.

THERAPEUTIC SYSTEMS:	
Disease	**Treatment**
Cardiac Arrhythmia	Physiologic Pacemakers
Sensory Aids	Implantable hearing and visual aids
Respiratory Apnea	Diaphragm or nerve pacing
Urinary Incontinence	Bladder control system
Hypertension	Automatic blood pressure control
Hydrocephalus	Ventricular size control
Pain, Cancer and others	Drug pumps
ARTIFICIAL ORGANS:	
Organs	**Hardware System**
Artificial Heart	Blood pump and control
Artificial Pancreas	Insulin perfusion system
Artificial Kidney	Dialysis Machine
Pressure measurement of foot contacting ground	Computer controlled walking for the disabled

Table 1.3 Examples of closed loop control medical systems, adapted from [59].

Medicine makes heavy use of silicon micromachined sensors compared with other sensing technologies, because of the high precision and small sizes which are achievable, some of these applications are listed in table 1.3. Other applications for pressure sensors include tonometers (devices which measure the pressure in the eyeball) [62] and infusion pump pressure sensors used to control the release of intravenous fluids and mixing of drugs in one flow channel [63]. Catheter tip sensing, respirators, lung capacity meters, barometric correction of instrumentation,

intracranial pressure measurement, blood pressure measurement in intensive care and home cuffs are all emerging technologies reliant on pressure sensors [59].

1.7.3 SUMMARY OF SENSOR APPLICATIONS

Clearly there is a large and growing, diverse range of applications for micromachined pressure and other sensors. Current technologies such as bulk micromachining and deposition of polycrystalline silicon have broadly served the requirements of these markets to date, particularly in the areas where lower precision can be tolerated e.g. automotive applications. As new application areas emerge and improved performance is expected, these traditional techniques are increasingly unable to cope. The SIMOX technology developed and discussed in this thesis enables the benefits of single crystal silicon to be exploited. This could provide devices for applications where high precision, and, for example, low hysteresis are important. Cost is an essential consideration in most sensor applications. As will be discussed in detail later, a further benefit of SIMOX fabrication is the facility for single-sided wafer processing. The result is processing simplicity and significant cost savings, in contrast to many technologies, both current and under development, which require two-sided and more complex processing.

1.7.4 THE SENSORS MARKET

Many industrial, commercial and domestic processes use some form of measurement, many of which have a sensor as the central component. Sensor production has become a rapidly changing field, initially relying directly on IC technology in terms of materials, equipment and massive investments [51] and then adapting and refining it to cope with the specific demands of sensor fabrication. It is estimated that 40 - 60 % of sensors in the 1990's are semiconductor based and in particular utilise silicon [64]. Micromachining, the sculpturing of small, three-dimensional structures, most frequently from silicon, is further extending and diversifying the silicon sensors market. As a result, silicon microsensors are taking an increasing share of the current market and generating new application areas, due to outstanding performance, small size and high reliability achieved at minimal cost. The automotive segment is the

largest current and near term consumer of silicon sensors [46], many new applications will arise from higher emission control and safety standards. Accelerometers for airbag deployment, ride control and inertial navigation are produced in quantities of 10 million a year.

The medical market is also expanding. Formerly fragile pressure sensors cost $600 each, and required a further $50 for sterilisation and re-calibration before each use [58]. Silicon sensors have cut these costs dramatically while also increasing equipment capabilities. The annual production of blood pressure meters increased from 40000 in 1982 to 17 million in 1994 and the unit price fell from $60 to $10! [58].

Within the field of environmental monitoring, while many new market sectors are developing rapidly, some are expected to saturate and thereafter diminish as users complete their purchasing programmes.

Optical devices such as waveguide couplers and switches are another expanding market, estimated to be worth nearly $900 million by the year 2000 [55].

Since the first smart pressure transmitter made by Honeywell in 1983, in just one decade the market grew 22 % annually to become worth $500m a year [58]. Over 25 million silicon micromachined pressure sensors were fabricated world-wide in 1992, and this figure has continued to rise [52]. It was recently reported that pressure sensors, fibre optic alignment structures and camera microlens arrays were already being manufactured at a rate of ten thousand per month world-wide [57]. Micromachined piezoresistive silicon pressure sensors are a steadily growing market. Micromachined silicon resonator pressure sensors are a slowly growing market. However, deposited thin film piezoresistive and micromachined capacitive silicon pressure sensors are more rapidly expanding markets [46]. It is predicted that in the year 2000, 30 % of the world market for micro-electromechanical systems (MEMS) will be accounted for by sales of pressure sensors for medical and transportation applications [66].

A study by Battelle Europe [52] identified approximately 300 companies, research organisations and universities engaged in work related to silicon sensing. Peterson

has reported [52] that in 1993, the German government promised roughly $60 million a year investment in research and development in this field, Japan's Ministry of Trade and Industry has provided $200 million and the US Congress' Office of Technology Assessment has recommended federal funding for micromachining [52]. Europe's position in the world sensors market is strengthened by a large technical knowledge base and good innovation skills, but it is disadvantaged by poor marketing and weak industrial/academic links [57]. Europe's research and development funding is equal to that Japan and the United States of America, but it requires direction toward marketable products in order to compete in the world market [57].

The complete global market for all microsystems is anticipated to be worth 7500 million ECU by 2000. In the UK, the largest sensors application area is plant and process control. This market was worth £22 million in 1990 and is expected to grow to £46 million by the year 2000 [43]. World-wide, this market was £7 billion in 1990 and is projected as being £25 billion in 2000 [50]. It is estimated that in Western Europe a growth of 110.7 % will be witnessed in the total sensors market between 1992 and 1997. Areas for high growth have been identified as low cost pressure sensors, accelerometers, flow and temperature sensors [46]. Rapidly expanding sensor markets are presented in table 1.4 which shows the Western Europe growth for 1997, compared with 1992.

Sensor type	1992	1997
Temperature sensors	18.7m	31.0m
Low cost pressure sensors	14.5m	35.0m
Pressure transducers and transmitters	420 000	650 000
Flow sensors	53 000	600 000
Low cost accelerometers	10 000	10.5m
Precision accelerometers	3 500	5 000

Table 1.4 Current projections for growth in the sensors market (numbers of units) compiled from data discussed in [46].

Much of the expected expansion in the automotive micromachined acceleration sensors market will be in low G devices for suspension control and high G devices for crash detection in air-bag systems. To give an idea of the rapidity of development in this field, in 1994 Analogue Devices marketed a low cost, 50 g, integrated micromachined airbag accelerometer. By 1995 a 5 g version was on sale with ten times the precision [51]. For low cost sensors, the most important market will remain the automotive field, while the demand for high precision devices will increase as more manufacturers adopt silicon sensor technology. As illustrated in the preceding sections, sensors have an important role to play and their success in terms of commercial exploitation is largely determined by performance, cost and reliability. For continued growth of the sensors industry a commitment to quality control must be undertaken with a resultant reduction in current defect levels which are unacceptable to many consumers.

1.8 SILICON MICROMACHINING

Micromachining is a broad term which encompasses techniques familiar from the IC industry, such as photolithography, selective etching and material deposition, with the addition of some other machining methods, such as laser drilling. Micromachining is the process in which a material (commonly silicon) is physically and mechanically machined on a micron scale to produce intricate miniature three dimensional structures. Microstructures and microsensors including the pressure sensor demonstrated in this project are fabricated using micromachining. In general it has facilitated reductions in device size and cost in parallel with performance enhancements. Micromachining, which was first investigated in the 1950's is reliant upon selective etching techniques which allow the controlled removal of specific areas or materials [67]. Directionally selective etching (anisotropy) was reported in the mid to late 1960's and this increased the precision achievable with etching [33]. This allowed batch processing and led to practical applications in aerospace and industrial control sensing [39]. Micromachining was first demonstrated with plated metals in the 60's and "rediscovered" in the early 80's [51]. Most of the sensing and fabrication techniques developed over the past 20 years are applicable to SOI, allowing the creation of complex and versatile microstructures with the mechanical component made of single crystal silicon, giving devices with improved performance

and high temperature capabilities. Important aspects of micromachining for sensor production are thin film deposition techniques, isotropic and anisotropic etching of single crystal silicon, polysilicon and other materials to form mechanical structures [50].

For centuries, engineers have built macro-mechanical structures and similar design rules can often be applied to the development of micron sized devices. The microelectronic achievements of recent years, particularly in integrated circuit manufacture, have reduced costs and increased sophistication, to allow the production of advanced but cheap systems. Most sensor fabrication processes, being adaptations of this silicon manufacturing for integrated circuits have been able to take full advantage of these achievements, utilising batch processing techniques leading to high quality, low cost products, supplies of high quality materials, sophisticated equipment and packaging knowledge also existed.

This allowed the fabrication of complex silicon microstructures to expand into an essential industry in recent years with numerous applications such as physical and chemical sensors, and moving microstructures for actuators. Examples of devices fabricated from micromachining include hall sensors [68], magneto-resistors [69], radiation sensors [70], fluid handling structures [71], infrared detectors [72] and displacement sensors [73]. Electrostatic silicon micromotors and free moving polysilicon rotors are also being extensively researched in many university laboratories [50].

Micromachining techniques are now said to be 'revolutionising sensor and actuator fabrication' and 'a vast array of silicon micromachined sensors is available' while 'actuators loom on the horizon' [52]. It has finally proven feasible to apply high standard, batch processes from IC production to microstructure and sensor fabrication, and on occasion combine the two on one 'smart' chip to give excellent performance to cost ratios.

1.8.1 SILICON, AN IDEAL MATERIAL FOR SENSORS

Single crystal silicon is particularly appropriate for use as the active element of a sensing structure. As described above it can be machined to micron and sub-micron dimensions, and mass production facilities can be used, resulting in high throughput and low unit cost. Silicon outperforms many traditional mechanical materials as demonstrated by the figures in table 1.5.

Property	Silicon	Aluminium	Quartz	Steel (stainless)
Yield strength / GPa	7	0.17	14	2.1
Young's modulus / GPa	190	70	380	200
Density / kgm^{-3}	2.3	2.7	1.5	7.9
Coefficient of thermal expansion at room temperature / $x10^{-6}K$	2.33	25	12	7.3
Thermal conductivity at room temperature / $Wm^{-1}k^{-1}$	157	236	11	33
Poissons ratio	0.2	0.3	-	0.3
Knoop hardness at room temperature / $kgmm^{-2}$	850	130	800 (fibre)	660

Table 1.5 The mechanical properties of silicon and other traditional mechanical materials [50, 58, 74, 43].

Silicon has a yield strength twice that of steel, this means silicon has a greater range of operation without hysteresis. However, their Young's moduli are comparable and its hardness is close to that of quartz - much higher than most common metals. For sensors this offers a resistance to physical damage and high frequency of vibration. The density of silicon is similar to that of aluminium (one third that of steel). This allows light weight devices to be fabricated. The coefficient of thermal expansion for silicon is one-fifth of the value for steel but the thermal conductivity is roughly 50 % higher. Silicon is therefore suitable for temperatures up to 200 ^{o}C compared, for example, with germanium which can only withstand low temperatures [33] (<80 ^{o}C), with little cross sensitivity to temperature. High temperature operation is important for

many sensor applications. Silicon displays virtually no mechanical hysteresis, its entirely plastic behaviour making it highly applicable to sensing applications. The cost of process silicon is low. In 1986, silicon cost \$0.85 in^{-2} (compared to gallium arsenide with a cost of \$10 - \$20 in^{-2}) [52]. It is difficult for newer materials to compete with silicon with regard to performance, cost, availability and process knowledge.

1.9 SUMMARY

In this chapter the aims of the project have been clearly identified as the fabrication of a capacitive pressure sensor from SIMOX material together with the evaluation of this sensor and a demonstration of the application of the developed technology to alternative microstructures. Considering these aims, this chapter has been used to introduce the basic concepts applicable for this type of pressure sensor.

A guide to the structure of this thesis has been given to aid the reader. A short introduction to capacitive sensing techniques used for sensors has also been given.

An overview of silicon-on-insulator materials, in particular SIMOX, has been presented, describing the benefits it offers over bulk silicon, its disadvantages and some of its applications. The advantages of the proposed sensor, particularly with regard to the expected high performance are detailed. A review of the markets and applications for sensors, which catalogues the huge growth in these fields, has been carried out. The objective of this section is to justify the development of a high performance pressure sensor. The chapter is completed with a very general introduction to the field of silicon micromachining to be used for sensor fabrication. The initial work for this project was to develop a full understanding of silicon fabrication technology, which is reviewed in chapter 2.

1.10 REFERENCES

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CHAPTER 2: MICROMACHINING TECHNIQUES

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2.0 INTRODUCTION

Following the definition of the project objective to fabricate a pressure sensor, chapter 2 investigates the appropriate technology with which this might be achieved. Micromachining combines traditional machining techniques with photolithography, etching and film deposition, each of which will be discussed in the following sections. These techniques must be fully understood to allow decisions to be made on which processes are optimum to achieve each step of sensor fabrication. A review of contamination issues and packaging technology has been included.

2.1 AN INTRODUCTION TO MICROMACHINING

Micromachining adapts the traditional techniques from the semiconductor industry to address the specific requirements of microstructures and microsensors, such as mechanical elements, miniaturisation and material sensitivity to produce micromachines with high performance to cost ratios. Such devices would previously have been conventionally machined with the inherent restrictions to larger dimensions. The technologies used in micromachining are clean, easily automated and precise and their success and subsequent growth has had a major influence on many aspects of life. The concept of micromachining was first demonstrated in the late 1960's with metal films. It was first employed to manufacture pressure sensors in the 1970's [1, 2] with interest renewed when such devices, fabricated in polysilicon, were extensively reported at the Transducers'87 conference.

Over the years, microprocessing has developed from the fabrication of simple diodes and transistors to that of highly complex, microstructures and dense, miniature, very large scale integration (VLSI) circuits with low power consumption and cost, coupled with increased reliability and speed. In the future, with the advent of new semiconductor materials and devices, higher packing densities and complexity are expected as ultra large scale integration (ULSI) circuits and advanced microstructures are realised, displaying high operating speeds, combined with decreased component size (i.e. sub-micron). The challenges which accompany sub-micron dimensions include scaling, smaller voltages, control of the resultant current density with electron migration problems in conductors and an increase in the significance of noise.

Micromachining is now an established technology in the field of sensors, producing low cost devices in high volume for the automotive industry and high performance devices in low volume for such applications as aerospace and medicine, several devices being commercially available. Micromachining offers potential benefits to many device types. It enables smaller, lighter versions of existing devices, production of sensors not otherwise possible, use of materials and processes common in microelectronics and batch processing. Study suggests that microengineered devices or those containing microengineered components will become substantial markets in the future. High growth is anticipated also for miniaturised sensors [3]. The ability to combine grooves and holes with diaphragms, extends the applications of such

diaphragm structures to chromatography, optical and printing devices. Mechanical resonant and acceleration devices have also been heavily researched and are now widely available.

Bulk micromachining involves the creation of structures within the body of a silicon wafer by selectively removing regions of the substrate material. It is a mature process, based on single crystal silicon etching and is used routinely for the fabrication of structures such as pressure and flow sensors, ink jet nozzles and microvalves. The main drawbacks of bulk micromachining are the long process times and restrictions to structure geometry imposed by the inherently high aspect ratios. For example, the fabrication of a thin diaphragm by bulk micromachining necessitates removal of almost the entire thickness of the wafer (see figure 2.1). This requires long etch times and results in large device sizes due to the angular profiles formed by common reagents.

Figure 2.1 Diaphragm Formed by Bulk Micromachining

Surface micromachining is a more versatile method of processing which is popular for the fabrication of three dimensional micromechanical structures. In this technique, thin film materials such as polysilicon, aluminium, silicon dioxide and silicon nitride are added and selectively removed. These films then form the structural, mask, interconnection, isolation and sacrificial layers in the final device. Surface micromachining allows smaller structures than bulk micromachining, (see figure 2.2) with improved dimensional control but residual stresses in the deposited films can be problematic.

Figure 2.2 Diaphragm Formed by Surface Micromachining

Surface micromachining techniques often involve the use of sacrificial or spacer layers. These are grown, implanted or deposited for later removal from beneath overlaid patterned materials. On dissolution, a suspended structure is formed from the overlayer, separated from the substrate by a thickness equal to that of the former sacrificial layer (see figure 2.3). Phosphorus doped silicon dioxide is a popular sacrificial layer for which etch rate and reflow characteristics can be controlled by adjusting the dopant levels.

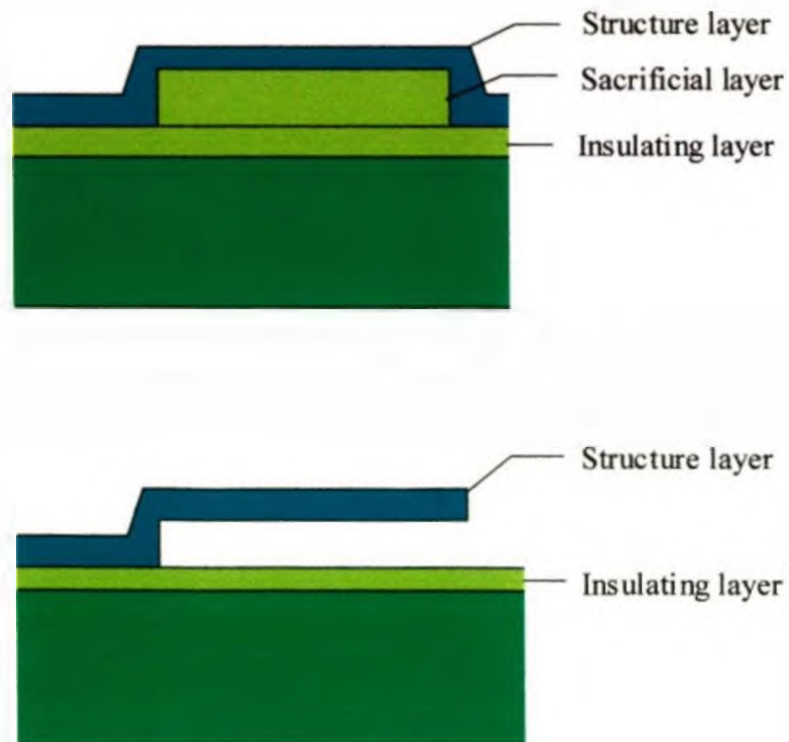

Figure 2.3 Cantilever formed by surface micromachining

The following sections examine the techniques available in more detail.

2.2 LITHOGRAPHY

In any silicon processing sequence, lithography is the first step used for structure definition [3, 4]. Lithography is the transfer of a pattern, via a radiation sensitive layer called a resist, from a mask on to the wafer surface as shown diagramatically in figure 2.4. Lithography is used primarily to determine which areas will be exposed to, and which will be protected from, etching or other processing used to form devices. The basic steps of photolithography are shown in figure 2.4. Where UV is used for pattern transfer, the process is called photolithography (or optical lithography). The definition of optical lithography is variable, sometimes referring to just the visible part of the spectrum or including the deep UV and occasionally the x-ray wavelengths [5].

An ideal lithographic system is one of high contrast where the dissolution rate of non-imaging resist is high compared with that of image forming resist. The relationship between the exposure tool, resist, processing parameters and pattern transfer is complex. In optimisation the interdependence of each step must be considered. Parameters used to indicate the effectiveness of a lithographic process are [6]:

(i) Resolution - the minimum feature size transferable with high fidelity.
(ii) Registration - the precision with which successive masks can be aligned.
(iii) Throughput - the number of wafers which can be processed in a given time.
(iv) Overlay - the cumulative distance between various levels of a mask for a given device.

Since initial lithography techniques in which physical scrubbing was used to remove non-image areas, tremendous advances have been made [7]. Now complex, computer operated, high yield processes are used to manufacture devices while research is extending to self developing resist and resistless imaging.

The future of lithography is guaranteed by both its existing uses and by the continuous development of new applications such as flat panel displays, micro/nano structures, microsensors and micro-electro-mechanical structures (MEMS) [5]. Process monitoring and control, e.g. on-line scanning electron microscope (SEM), critical dimension measurements are essential to meet the quality goals and can reduce or eliminate the need for final electrical testing. End point detection systems can be implemented in photolithography, for example to avoid overdevelopment with

associated changes to feature geometries. Lithographic equipment can represent as much as one third of the cost of outfitting a fabrication facility [8]. Considerations for the adoption of new lithographic techniques are: technology maturity, economics (cost of ownership versus yield), resolution, overlay, mask availability and critical dimension control.

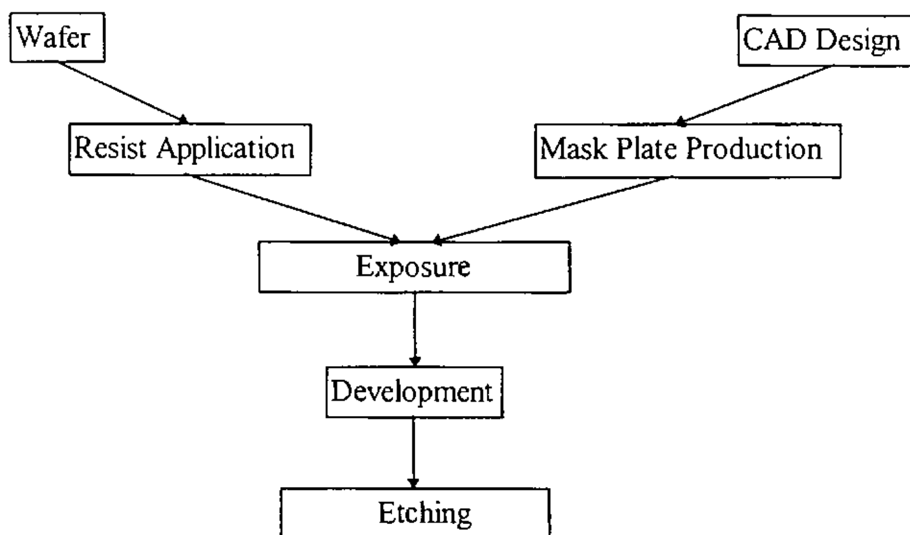

Figure 2.4 A Typical Lithography Process Procedure

Contact and proximity exposure were used first in the early seventies for LSI applications with 10 μm geometries and for nearly thirty years, with continual development, optical lithography has continued to form the baseline of the semiconductor industry [5].

Projections for the replacement of optical lithography by alternative techniques have not been fulfilled and it remains useful for current and future device fabrication. Despite costly increases in complexity, ultra violet (UV) and deep ultra violet (DUV) exposure techniques have maintained alternative technologies in niche application areas [5]. This success is due partly to computer aided lens design, improvements to micropositioning stages and advances in materials and photoresist chemical systems, allowing increased numerical aperture and decreased exposure source wavelengths to be used, enabling smaller geometries to be defined. This, together with improvements to wafer planarisation, led to greater benefits than expected when technology changed from g-line (436 nm) to i-line (365 nm) UV exposure [9]. The advance to the deep

UV (l < 300 nm) is, however considered to be inevitable. At DUV, the photoresist transparency loss can necessitate an extra step to transfer the 'surface image' to the remainder of the resist depth which has not been imaged. This is a technique which is still at the research stage. Despite increased hard and software complexity and the triple sequence of prime, resist and overcoat required, DUV must display high throughput to be competitive with mid UV (MUV). Layer specific photolithography can be implemented where different layers are exposed by different techniques depending on the accuracy required [10].

By 1998 it is expected that 248 nm wavelength step-and-scan exposure will be used for the 0.25 μm IC generation [11]. With enhancement techniques e.g. isofocal bias. further reduction to 193 nm is expected to extend this technology to 0.15 μm - 0.18 μm geometries by 2003. 248 and 193 nm wavelengths will be produced by excimer lasers, as no other efficient, high power UV sources are available. 193 nm may prove to be the minimum wavelength used in conventional techniques, without large and costly efforts. Only a limited number of mask materials exists for below 193 nm. Absorption in fused silica is prohibitive and radiation damage significant [12].

2.2.1 OPTICAL LITHOGRAPHY

Optical lithography is usually carried out in a room lit by yellow light, since photoresists are insensitive to wavelengths greater than 0.5 μm [6]. However 'mini-environments' are growing in popularity to replace expensive photolithography rooms. Photolithography environment is maintained to a high standard of cleanliness with a low particle count to minimise patterning defects. Optimisation of photolithography conditions gives control over the resist critical dimensions, sidewall angle, chemical resistance, resolution, veiling and resist adhesion, all of which affect pattern definition and ultimately device integrity. A photolithographic system should have minimal energy requirements and low sensitivity to secondary images from scattering. Process times, temperatures and concentrations may be adjusted to increase production rates. In optical lithography the minimum feature size and depth of field are dependent on the numerical aperture and wavelength in exposure as given by [13]:

$$S = \frac{k_1 \lambda}{NA} \qquad (2.1)$$

$$DOF = \frac{\lambda}{NA^2} \qquad (2.2)$$

k_1 is a constant which is dependent on variables such as the exposure tool, resist and process technology employed. Smaller features can be imaged accurately by a reduction in k_1, λ or numerical aperture (NA).

2.2.1.1 PHOTOLITHOGRAPHIC PROCESS SEQUENCE

The typical sequence in photolithographic wafer patterning is shown in figure 2.5 below:

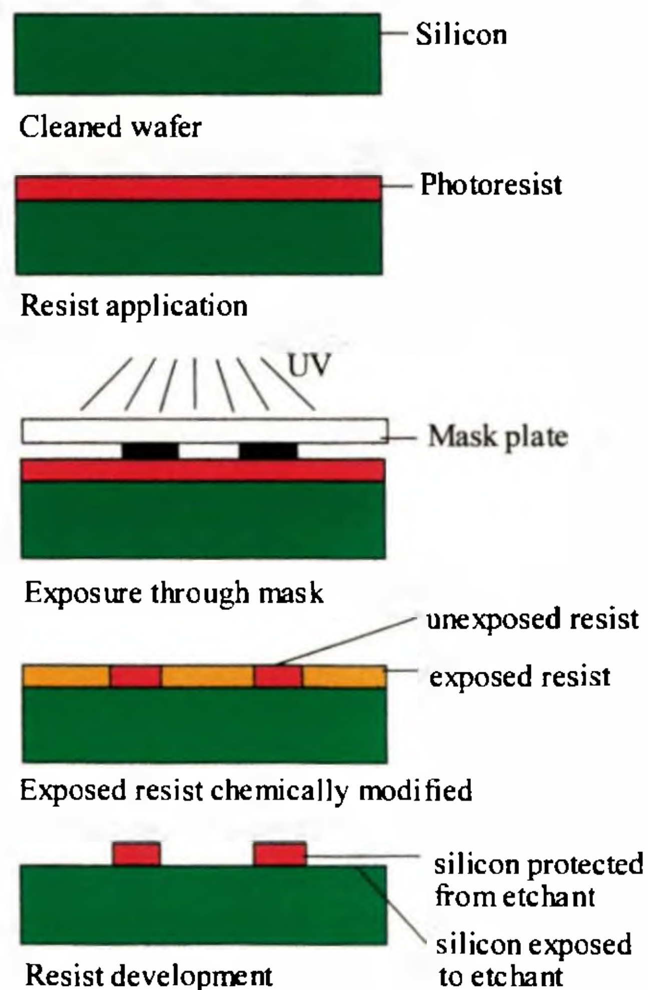

Figure 2.5 Photolithography Sequence

2.2.1.2 PHOTORESIST

Light sensitive photoresists can be either positive or negative in action [6]. Photoresist can be applied to a semiconductor surface by various methods, to form, ideally, a uniform adherent and defect free layer. A short air dry may be used to even out the layer and maintain more resist on step corners. With positive resist, the pattern formed in the resist is the same as that on the mask [13]. UV exposure increases resist solubility in developer solution by a chemical conversion. For negative resists the opposite is true [13]. Positive resists are polymer based systems consisting of a solvent carrier with a photosensitive compound, for the exposure response, see figure 2.6 [6]. Despite a lower throughput, positive resists have become popular because they can achieve the fine geometries demanded in modern processing [14]. Negative resists suffer from a loss of pattern resolution due to swelling during development. There is a trade off between a thin resist which will give increased image resolution and thicker layers which have increased resistance to subsequent steps such as dry etching and improved coverage of topography [6].

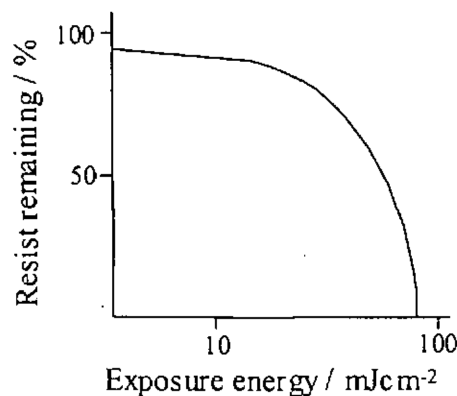

Figure 2.6 The exposure response curve for positive resist (taken from [6])

Prior to photoresist application, a wafer is prepared by cleaning and baking to remove moisture and coating with an adhesion promoting or priming layer. The most commonly used compound for priming is hexamethyldisilazane (HMDS). Water free HMDS links with the wafer surface to prevent the reabsorption of water after a dehydration bake, improving photoresist adhesion which consequently reduces undercut and the occurrence of pinholes, allowing improved dimensional control [15].

Photoresist should ideally be applied within 60 minutes of priming. Adhesion promoters may be applied by spin, dipping or vapour methods. Spinning allows easy variation of temperature and concentration, results in a thick layer and requires no additional equipment over that required for photoresist application. Dipping has similar benefits but can be performed in batch. Vapour priming can be performed in large batches, in-line which provides high throughput with potentially reduced contamination over the alternative methods, this results in high uniformity with economical and environmental benefits. Following vapour priming, an approximately 5 minute delay should be allowed for the evaporation of any primer condensate on the wafer surface.

Photoresist can be coated in a variety of ways including roller and spray application or most commonly spinning [7]. In the last, a wafer is held flat on a vacuum chuck within a bowl designed to prevent splashback and with controlled exhaust. The wafer is then accelerated to a constant rotational speed, typically 1000 - 10000 rpm, depending on the resist viscosity [6]. During spinning, the centrifugal force removes much of the resist, producing a uniform film with a thickness controlled by substrate surface tension forces and resist viscosity [7]. The main parameters which determine the final film quality are; spin time, spin speed and resist viscosity. Numerous other factors also affect the film to a lesser degree. For example, within the dispense step alone, overdrip, wafer and chuck diameter, bowl temperature, downdraft exhaust, dispense volume and spin acceleration all have an effect [7].

Single, thick resist layers can become striated or develop ripples. As an alternative multilayer resists can be used to achieve high aspect ratio structures [13]. A bottom resist layer planarises the wafer topography while a second thinner coat is patterned and used in turn to define the thick layer beneath. A third, intermediate layer can be used to address chemical incompatibility [13]. The main disadvantages of multilayer resists are the additional process steps required with departure from well practised techniques and increased costs.

An antireflective (AR) coating (e.g. a spin applied organic polymer) can be used under the resist to improve focus/exposure latitude and enhance critical dimension control by eliminating substrate reflections and thin film interference which can

produce uneven exposure [16]. Chemical compatibility between the AR coating and photoresist is important [17].

Self developing resists are attractive for reductions in equipment, personnel, cleanroom space, the number of process steps, handling defects, breakages and contamination [7]. Residue free images can be produced by exposing a resist in deep UV, E-beam or x-ray environments or with lasers. However, these products are still in development and image hardening solution dips, plasma or thermal treatments are invariably required to improve resistance to subsequent processing [6].

2.2.1.3 SOFTBAKE

Soft baking, is a short heating cycle, used to drive solvents from the resist and improve adhesion to the wafer [6]. If large quantities of solvent remain in the resist, the solubility of the image forming material increases. Therefore improper soft baking results in poor final image quality. A compromise in soft bake conditions is sometimes used to increase throughput by allowing a reduction in the exposure and develop time required. However, geometric control and chemical resistance of the image are sacrificed [7]. The glass transition temperature is the point below which a polymer has the physical characteristics of glass, with stationary molecular chains. This is 110 - 120 °C for positive optical resists. Soft baking above this temperature increases thermal flow by chain movement which seals small micropores in the film and improves uniformity [7]. This also relaxes the stress resulting from the spinning process, reducing the probability of stress induced shattering and cracking of the resist in subsequent steps. Hot plate heating is preferable to oven baking for high definition images, as good, uniform thermal control is achievable and allows the resist to dry from the back, allowing the escape of solvents to avoid bubbling and film stress. Equipment is basic, in-line track systems can be used and particle contamination reduced [13].

Delays between bake and expose or expose and develop steps can cause variations in image dimensions.

2.2.1.4 MASK PLATES

A mask plate is placed between the radiation source and resist during exposure to define the areas to be sensitised. Masks are typically manufactured from glass plates coated with a soft material such as emulsion for feature sizes of the order of 5 μm and above, or with hard layers such as chromium or silicon for smaller dimensions [6]. An antireflective coating may also be applied. Originally each step of mask fabrication was conducted manually. The first step in mask production is the drawing of a composite layout, (typically between 100 and 2000 times the final device dimensions) [6], this is now carried out using a computer aided design (CAD) package such as Autocad or Cadence. The composite design consists of several layers each corresponding to one photolithography step and resulting in an individual mask [6]. The drawing can then be cut into a plastic laminate such as rubylith by a plotter using digitised data. The red layer is cut and peeled to reveal the pattern in terms of red and clear regions. This is illuminated and reduced onto a polished glass plate coated with high resolution gelatin emulsion (or chromium). Step and repeat projection printing transfers the design from the reticle onto the mask plate. Each mask site has an identical pattern resulting in a matrix of sites each containing the complete device pattern for that masking level [6]. This method, which is no longer used in industry, was used for the test design masks in this project.

An alternative technique uses the digital data from the CAD system to drive an optical pattern generator which writes directly on to a photosensitised, chrome coated mask plate [6]. The design may be raster or vector scanned by the E-beam but can be limited to small areas which then need 'stitching' together [13]. Electron beam direct writing has been developed in which 0.15 μm feature sizes are achievable. However, some problems can result from scattering [13]. The final product may be used as a working mask or as a master, from which copies are taken as working masks.

2.2.1.5 EXPOSURE

Following resist application and soft bake, the wafer is ready for patterning, i.e. the transfer of the mask pattern onto the resist coat. Cooling of a wafer to room temperature is essential prior to exposure. Typically UV light is shone on the wafer

through a photomask. Exposure energy uniformity, exposure time and environmental cleanliness are the important factors affecting image quality [6]. The exposed regions of positive resist are converted by the UV light to an alkali soluble carboxylic acid [13]. Exposure of negative resist forms a relatively insoluble diazo inhibitor in a phenolic resin complex and the unexposed regions remain soluble [13]. Overexposure of positive resist is used occasionally to eliminate widening of images at the base of a step with thick resist [7].

During exposure, pattern transfer may be achieved by contact, proximity or projection methods. The difference between these techniques is the distance between the mask and substrate during exposure [6]. Contact printing, in which the wafer and mask are in intimate contact, provides high resolution but particles can become embedded in the mask, damaging it for current and subsequent exposures [6]. This arrangement was used in this work and is shown in figure 2.7. In proximity printing a 10 - 50 μm gap is sustained between the wafer and mask. Particle effects are reduced but resolution can be degraded due to optical diffraction occurring at the edges of photomask features [6].

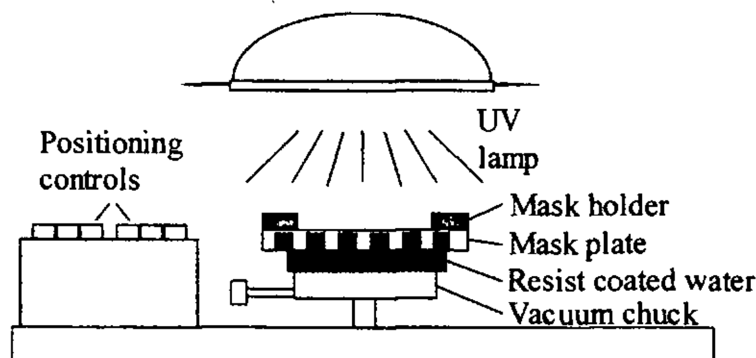

Figure 2.7 Set-up for Contact Printing Exposure

When projection printing is used for exposure, the resist coated wafer is several centimetres away from the larger than actual size, mask [6]. To increase resolution, small sections of the mask plate are exposed individually, and scanned or stepped over the entire wafer surface. Some key advantages of projection printing are [7]:

(i) the use of masks ten times the final image size which gives a reduction in distortion, line deviation and defects (e.g. a 3 μm reticle defect now becomes a 0.3 μm device defect).

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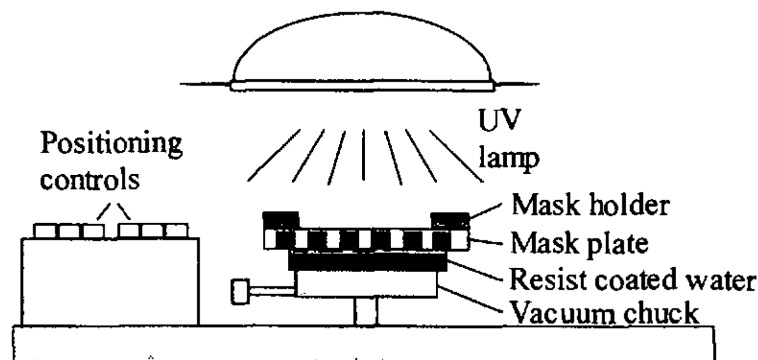

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(i) the use of masks ten times the final image size which gives a reduction in distortion, line deviation and defects (e.g. a 3 μm reticle defect now becomes a 0.3 μm device defect).

In immersion developing, the simplest technique, substrates are placed in a solution bath and agitated to ensure a constant development rate. Immersion developing is used primarily in research and prototyping as it is inexpensive and easily monitored. Bath concentration is a primary parameter for process control and decreases with resist dissolved. Solutions should be covered when not in use to maintain concentration as environmental carbon dioxide reacts with positive developers and solvents evaporate from negative solutions [7]. Alternatively in production environments, puddle or spray/stream flood developing may be used [13]. It is highly repeatable and economic with developer. In the puddle technique, developer is dispensed on to the wafer on a track system to form a meniscus [7]. After a predetermined time, the wafer is sprayed with water to end development. Heated spray heads with sub-micron filters and multiple dispensing branches can be used to supply fresh developer over the entire surface of each wafer, which minimises uneven developing. Spray/stream developing is rapid and repeatable [7]. Low spray pressures eliminate foaming and air trapping. Centrifugal flood-spray developing combines puddle and spray techniques. A fan-shaped developer spray wets each wafer surface while the carrier is rotated to achieve puddling. The combined motion scrubs the surface promoting uniform development. Process time is low but developer consumption is high. Dry developing techniques have been demonstrated with high process control and yield using positive, negative and multilayer resists but are not fully developed for implementation in production [7].

2.2.1.7 HARDBAKE

The final step in the photolithographic sequence is the hard bake (or post bake). In this process the substrate is heated, typically to 100 - 180 °C, depending on the resist type [6]. This improves photoresist/wafer adhesion and removes residual moisture remaining from the development process [6]. Postbaking may round the top profile of features, but base dimensions (at the substrate) should remain unaffected [13]. Extensive heating can be used to 'harden' the resist, improving its chemical resistance to etchants or promote plastic flow [13].

Following etching to transfer the resist image to the wafer, complete removal of the imaging photoresist is carried out commonly using a specific resist stripper, acetone, a

sulphuric acid/hydrogen peroxide clean or an oxygen plasma [13].

2.2.2 OTHER FORMS OF LITHOGRAPHY

To compete with optical lithography, alternative techniques must demonstrate comparable throughput, resolution, overlay and critical dimension tolerances. Lasers have not, in general, been implemented for lithography due to interference between the various optical lengths. However, excimer lasers can be used with special resists e.g. poly (methyl methacrylate) (PMMA) [13].

Electron beam lithography is a high resolution direct writing technique [7], most commonly used for the manufacture of mask plates. For substrate patterning its popularity has been limited due to poor resist sensitivity, electron-electron interaction at the substrate-resist interface, high system cost and slow beam movement resulting in low throughput. x-ray lithography [7] is an alternative technique which has high resolution due to the ultrashort wavelengths involved and uses aligners similar to optical equipment. Defect densities are low as dust and particles of resist, silicon, its compounds and similar low molecular weight defects are all invisible to x-rays. However, problems include edge blur, complex mask preparation and a lack of available sources for high volume production [6]. Focused ion beam lithography allows sub-micron patterns to be directly written into standard optical resists and semiconductor layers by the penetration of ion species. Scattering, resulting in changes to feature sizes, is mostly eliminated, resulting in high resolution [13]. Energy transfer from the beam to the resist is extremely efficient due to the similarity in atomic masses and the elevated energy of the beam [7]. In extreme ultra violet (EUV) lithography a radiating hot plasma source is used in conjunction with a reflection mask. However, the accuracy of mirror surface required for such a mask is beyond current measurement technology, let alone fabrication capabilities. Despite this, EUV lithography is being heavily researched in the US, Japan and Europe [12].

2.3 ETCHING

Etching is the process by which a material layer is selectively removed by the

chemical reaction between an etchant and substrate and/or by the physical action of ion bombardment. Etching can be realised by wet (solution) or dry (plasma) techniques. Etching can be applied to the uniform removal of layers e.g. polishing and defect removal and the local removal of layers e.g. pattern delineation. In the latter, which is the most relevant to this work, etching results in the transfer of the mask pattern to the substrate material. Clearly the masking material must be relatively unreactive with the chosen etchant system. All etchant systems should fulfill certain general criteria [18] such as:

(i) Etch uniformity over the wafer surface.
(ii) Wafer-to-wafer repeatability.
(iii) Ability to function at low temperature conditions.
(iv) Minimal surface damage.
(v) High selectivity between different materials.
(vi) Good directional control.
(vii) High resolution.
(viii) Short processing time to give high throughput.
(ix) Low cost.

High selectivity is particularly important as it allows for accommodation of etch rate gradients or other non-uniformities across the wafer, control of critical thickness and preservation of the etch mask.

2.3.1 WET ETCHING

Wet etching, material removal using a liquid etchant is used extensively in silicon technology [6]. This type of etching is highly effective but can result in photoresist undercut giving ragged edges and breakage of fine lines. Generally, a wet etchant comprises a chemically active component, a complexing agent and a diluent and etches in a three step process [6]:

(i) Reactants are transported to the reaction site.
(ii) Chemical reactions occur at the surface.
(iii) Reaction products are transported away from the reaction site.

In most cases, step 2 involves either the dissolution of a material in a solvent or the conversion of materials into a compound which subsequently dissolves [6]. Wet etching is commonly carried out in an etch bath with temperature and agitation control, but spray methods are also available [7]. Agitation is used in most wet processing techniques including photolithography. This ensures a continual supply of fresh solution to the reaction site to sustain a high reaction rate. There are several methods of agitation [19] including hand, thermal, mechanical arm, rocking mechanism, nitrogen bubbling or ultrasonic. These vary in effectiveness. If no agitation is used slow etch rates are recorded with a high degree of isotropy. The end point of an etch process is often recognised by knowledge of a predetermined etch rate but alternative methods e.g. laser interferometry can be used in production lines. The shape, size and profile of an etched feature are readily controlled by a number of factors, for example: etch time, etchant concentration, temperature, material structure, material layers, dopant concentration and crystallographic orientation [7].

An increase in the etch time, etchant temperature or etchant concentration would be expected to affect the etching by increasing the reaction rate. Typically a ten degree rise in temperature results in an approximate doubling of the etch rate [13]. Low temperature is sometimes chosen in order to increase process control. The exact shape of the mask opening, e.g. roundness of corners, also has an effect on the final etched feature shape [20].

Different materials can etch at radically different rates in the same etchant, therefore a material interface can be used to control etching. For example, silicon etching can slow so as effectively to cease at a silicon/silicon dioxide boundary in a highly selective process. Doping is also commonly used to control etching [13]. Doping of specific areas is carried out prior to etching and the etchant will attack that area at a faster or slower rate compared with bulk material. For example, for boron concentrations greater than $\sim 10^{18}$ cm^{-3}, a significant reduction in silicon etch rate is seen with most common etchants. However, for microstructures, the high stress caused by this heavy doping can be problematic [21]. Many etchants show a dependence on the crystallographic orientation of a sample, etching the various crystal planes at different rates. This is known as anisotropy [6] and is routinely used for etch control. For potassium hydroxide (KOH), a commonly used wet etchant, etch rate

ratios between planes can be as much as 100 : 16 : 1 for the planes (100) : (110) : (111) [6]. The anisotropy of an etchant is given by equation (2.3), where A = 1 indicates complete anisotropy and A = 0, complete isotropy [6]:

$$A = 1 - \frac{V_h}{V_v} \qquad (2.3)$$

V_h and V_v are the horizontal and vertical etch rates respectively.

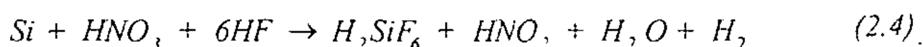
Although an indispensable tool for etch control, anisotropy and material selectivity can prove detrimental by allowing non-uniformities such as microparticles of resist to serve as masks which become exaggerated in etching [7]. An isotropic etchant is unaffected by the crystallographic orientation of a material, giving a single etch rate, identical in every direction for a particular material/etchant combination [6].

Wet etching can be controlled by electrochemical means, where the etchant is placed in a cell containing 2, 3 or 4 electrodes depending on the degree of control required [22]. In this arrangement, etching will cease at the interface of a region of different polarity in a biased p-n junction within the material [22].

2.3.1.1 SILICON ETCHING

Silicon etching usually proceeds by a process of oxidation, followed by the oxide dissolution and transport of reaction products away from the etch site [6]. A wide range of liquid based etchant systems have been studied and discussed in the literature. A common etchant composition is nitric acid (HNO_3) and hydrofluoric acid (HF) in water or acetic acid (CH_3COOH), e.g. 5 : 3 : 3 volume parts HNO_3 (diluted to 79 wt%) : HF (diluted to 49 wt%) : undiluted CH_3COOH [6]. Nitric acid acts as the oxidant, HF dissolves the oxidised products, and the acetic acid diluent allows improved process control. The silicon etch rate for this etching is typically 80 $\mu m min^{-1}$, [13].

The isotropic reaction is [6]:



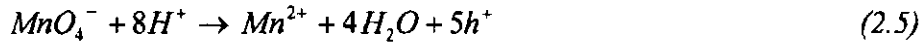
$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2 \qquad (2.4)$$

This system has been studied extensively [23], and numerous alternative formulations can be used. Potassium or sodium hydroxide (KOH or NaOH) based etchants are used commonly for anisotropic silicon etching [24, 25] or alternatively ethylenediamine pyrocatechol (EDP) can be used. A typical etchant composition would be 45 % KOH and 55 % water, at 90 °C in which the etch rate for (100) silicon is 25 $\mu m min^{-1}$. Isopropyl alcohol is often added to the potassium hydroxide and water (H_2O) to reduce the silicon dioxide etch rate, thus allowing its use as a mask. This alkaline etching proceeds by a reaction dependent on the number of dangling bonds present at the silicon surface. Such an etchant provides excellent uniformity with no agitation being necessary.

Etchants based on oxidizing reagents such as potassium permanganate can also be used for silicon and show a higher selectivity over silicon dioxide than the above system [13]. Since this is a requirement for sensor fabrication from SOI, the remainder of this section will concentrate on this etchant system, an example of which is potassium permanganate ($KMnO_4$). The HF, $KMnO_4$, H_2O silicon etching system has been used since the 1970's [26]. At high concentrations (7 g $KMnO_4$ in 100 ml HF) a vigorous exothermic reaction occurs on mixing which displays limited stability and inconsistent etching [26]. It is thought that at high $KMnO_4$ concentrations, the SiF_6 formation rate is too fast for its removal by H_2SiF_6 production and some remains to form K_2SiF_6. The liquid etchants diffuse through the K_2SiF_6 to react with the silicon surface but the rate is reduced. At low HF concentrations, a solid phase film is formed on the silicon surface and inhibits etching [26]. The layer has been identified as K_2SiF_6. It has been reported that SiF_6 is an intermediate product on the silicon surface. This may react with protons or potassium ions. In the former case, a soluble product, H_2SiF_6, is produced, but in the latter the K_2SiF_6 film is formed. This is not soluble in the etching solution but was found [26] to be completely dissolved by pure 48 % HF. At intermediate concentrations etch depth has been demonstrated to be linear with time under stable conditions [26]. The etch rate is typically in the region 0.4 $\mu m min^{-1}$ and a highly polished surface results [27].

The reaction is thought to proceed by a two step mechanism [26]:

(i) The oxidation of silicon by the injection of holes, produced by the reaction of MnO_4^- with H^+:

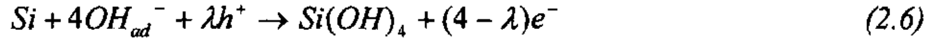


$$MnO_4^- + 8H^+ \rightarrow Mn^{2+} + 4H_2O + 5h^+ \qquad (2.5)$$

This is followed by:

(ii) The dissolution of the oxidised silicon surface by HF, for which different mechanisms exist for high and low HF concentrations:

low concentration



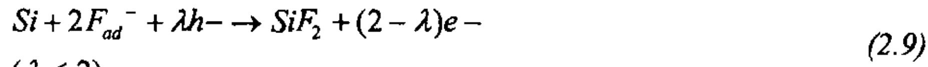
$$Si + 4OH_{ad}^- + \lambda h^+ \rightarrow Si(OH)_4 + (4-\lambda)e^- \qquad (2.6)$$

$(\lambda \leq 4)$

$$Si(OH)_4 \rightarrow SiO_2 + 2H_2O \qquad (2.7)$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \qquad (2.8)$$

high concentration



$$Si + 2F_{ad}^- + \lambda h- \rightarrow SiF_2 + (2-\lambda)e- \quad (\lambda \leq 2) \qquad (2.9)$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2 \qquad (2.10)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \qquad (2.11)$$

ad = adsorbed state, h^+ = hole, e^- = electron

A graph of etch depth versus time is given in figure 2.8. The etch rate is reported to show a maximum for a $KMnO_4$ concentration of 0.05M [26]. At increased concentrations the rate decreases gradually. At a concentration of ~ 0.12M, a negative rate is recorded representing deposition of the solid phase film [26]. Equation (2.5) demonstrates an increase in hole concentration with increasing $KMnO_4$ concentration. This explains the initial rise in etch rates with $KMnO_4$ concentration.

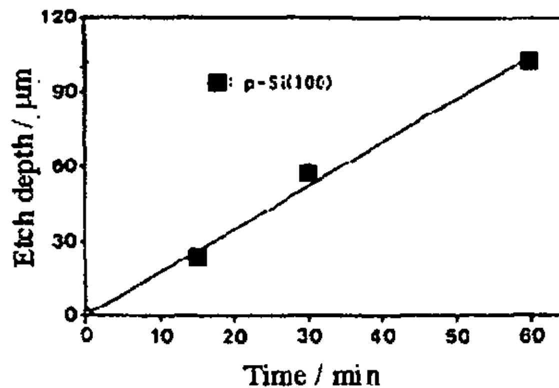


Figure 2.8 The silicon etching behaviour of $KMnO_4$ [26]

As discussed above, the $KMnO_4$ causes accelerated K_2SiF_6 formation on the silicon surface [26]. At low HF concentrations this formation exceeds the dissolution rate of K_2SiF_6 in HF. However, as the HF concentration increases, H_2SiF_6 removal can be maintained. The etch rates have been shown to be unaffected by the addition of F^- [26].

Under conditions of increasing agitation, up to 800 rpm, the etch rate increases, it then saturates and remains constant. An Arrhenius relationship is seen between etch rate and temperature, as shown in figure 2.9, from which an activation energy of 6.8 K-calg-mol^{-1} has been determined [26] for the etchant composition 12M HF, 0.05M $KMnO_4$, H_2O at 800 rpm on (100) silicon.

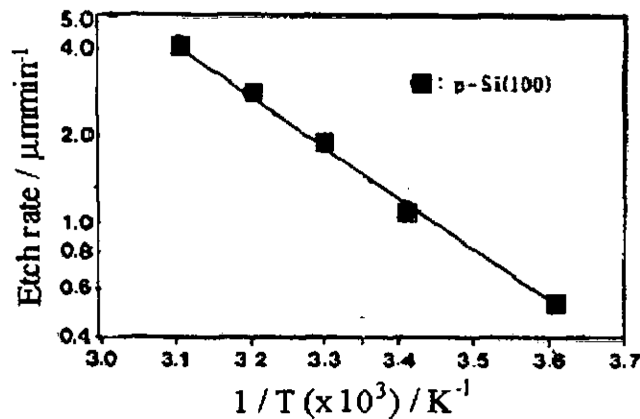


Figure 2.9 The temperature dependence of $KMnO_4$ silicon etching [26]

The drawbacks with etching silicon in this solution are etch rates which are typically only 1/3 of those with HNO_3, HF, HAc and a build-up of reaction by-product which becomes important in large batch processes [26].

2.3.1.2 SILICON DIOXIDE ETCHING

Silicon dioxide is commonly etched by its conversion into soluble salts or complexes by a reaction with dilute hydrogen fluoride (HF) [28]. HF dissolves silicon dioxide by domain etching, where by many pits are created in the oxide by the acid. These increase in size, overlap and combine as etching progresses. The HF is often diluted to

slow the etch rate and buffered with ammonium fluoride (NH_4F) [29] to avoid depletion of fluorine. This also ensures consistent etching and reduces photoresist attack. This etchant has been reported as being used in numerous ratios. Low HF concentrations are commonly used for processing small dimensions, since overetching to ensure complete material removal will cause less undercut.

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (2.12)$$

The reaction kinetics are related to the concentration of HF and HF_2 ions. The latter is commonly 4 - 5 times the HF concentration. The relative concentration of these ions affects the pH of the etch solution. The pH of a typical etchant composition is 3. HF and BHF (buffered HF) have poor wetting on silicon which can present difficulties for etchant penetration into deep holes. This can be aided by the addition of a surfactant. In general film oxides etch faster than bulk and faster still if there are effects such as built-in stress, stoichiometry irregularities or radiation damage [30]. Layers can be densified by annealing which will result in a fall in etch rate. A dry thermal oxide will etch slower than a wet grown layer since it has a closer packed structure [31]. Where the thermally grown oxide is undoped, the etch rate is uniform through its entire thickness. For implanted oxide this is not the case. Phosphosilicate glass (PSG) or borosilicate glass (BSG) also etch in HF and BHF with a rate which increases with dopant concentration [31].

2.3.2 DRY ETCHING

2.3.2.1 HISTORY AND EQUIPMENT

In dry etching a plasma is used to remove unmasked material layers, a high degree of anisotropy can be achieved [13]. Material is removed by its chemical reaction with a gaseous etchant and/or by physical bombardment. This technique, adapted from photoresist plasma removal methods in the late 1960's, was initially abandoned due to the presence of tin residuals which resulted in severe device degradation [32]. With the emergence of n-type metal-oxide semiconductor transistor (NMOS) and DRAM technologies in the early 1970's, the techniques were resurrected and by 1976 dry

etching was regularly used [14]. There are several types of dry etching processes which are summarised below.

2.3.2.2 METHODS OF DRY ETCHING

In a plasma etcher, the plasma is confined between two close, parallel plate electrodes, one of which is RF driven and the other grounded [6]. A number of wafers can be placed on the grounded electrode. Molecular halogen gases are used for etching at high pressure (0.1 to 10 Torr), and low plasma potential (< 20 V).

Reactive ion etching (also called reactive sputter etching, ion assisted chemical etching and chemical assisted sputtering) uses ion bombardment to achieve anisotropic etching of small dimensions [32]. The system is effectively an electrical circuit and chemical reactor operating interactively. The wafers are placed on an RF driven electrode (cathode) which is capacitively coupled to a high frequency (13.56 MHz) supply. The other electrode is grounded and includes the chamber walls [33] which gives a high anode : cathode ratio. This, combined with the low operating pressures (0.5 - 100.0 mT), produces high plasma potentials (200 - 500 V) resulting in high energy ion bombardment [32]. Processing is initiated by the formation of a glow discharge plasma between the two electrodes, constituting a gaseous etching environment of charged species containing positive and negative ions, electrons, radicals and neutrals. The radicals and neutrals react chemically with the wafer to produce volatile species. The positive ions are accelerated and bombard the wafer. Their energy is dependent on the dc bias voltage across the plasma sheath (dark space) in the inter-electrode space [32]. This bombardment results in volatilisation and accelerates material removal. Due to the asymmetric electrode configuration, a small negative bias develops between the anode and plasma, leading to preferential positive ion bombardment of the cathode with minimal sputtering of the anode [32]. Single wafer etchers meet stringent process demands and can be automated to reduce operator handling e.g. microprocessor control and endpoint detection. These often use high power and pressure to achieve faster etching but some process control is sacrificed. An auxiliary substrate heater maybe incorporated into the etcher design. Hexode style etchers allow more wafers to be etched simultaneously compared with the planar design described above and preferential cathode bombardment is

pronounced [34], reactor structures are shown in figure 2.10. Alternatively, hybrid reactors combine several single wafer etchers in one machine to allow particular chambers to be dedicated to specific chemistries. A molecular gas is used and operating parameters can be adjusted to provide good control over selectivity, uniformity and anisotropy [13]. Isotropy exists when chemical etching predominates, which generally occurs at high pressure (> 100 mT) or low power. Optimum etching conditions are typically high flow rate, low (< 100 mT) pressures and low power to prevent damage. This may reduce rate and throughput, but maximises selectivity and dimension control. Sidewall bowing may sometimes occur due to reflection of bombarding species from the edges of the mask. Passivating films formed during etching can be removed from the surface by ion bombardment but remain on the sidewalls. This prevents undercut, resulting in vertical profiles [13]. Demands for higher linewidth control have encouraged the use of chlorine based chemistries, but with this comes severe resist stability and residue problems.

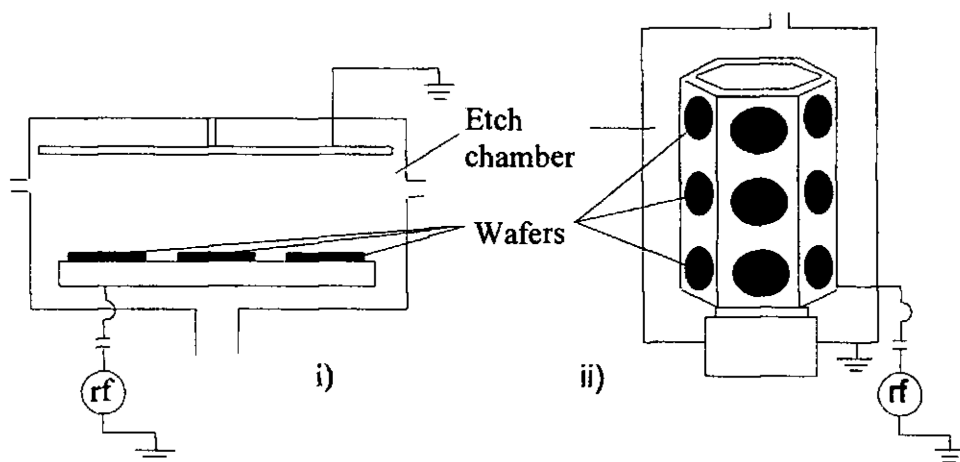


Figure 2.10 i) Planar Electrode Configuration ii) Hexode Configuration For Reactive Ion Etching (RIE) [35]

Sputter etching systems use high energy (≥ 500 eV) noble gas ions e.g. Ar^+ to etch wafers on the powered electrode [6]. The ions are accelerated normal to the wafer in an applied field by momentum transfer. Atoms near the substrate surface become volatile and are removed. Typical operating pressures are 0.01 to 0.1 Torr. This produces high anisotropy but poor selectivity [6].

In reactive ion beam etching (RIBE) fluoro-carbon reactive gases are used. Ions produced from electron/gas collisions in the plasma within a discharge chamber are extracted and accelerated onto the wafer by an electrostatic lens. The high ion energies (600 - 1200 V) and densities are separately controlled and gas pressures are low (< 2 mT) to prevent beam decollimation by scattering. This apparatus uses a cold cathode or heated filament source. Radiation damage can sometimes be problematic [7].

2.3.2.3 CHEMISTRY OF PLASMAS

When inert plasma species are used, the wafer is bombarded by the positive ions and subjected to fluxes of other charged and neutral particles [35]. In reactive gases, e.g. chlorine or fluorine, the chemistry is more complex. For example with CF_4 gas, collisions lead to the formation of saturated ($CF^{\bullet}_3$) and unsaturated ($CF^{\bullet}_2$) radicals, molecular (CF_3^+) and atomic ions (F^-) and the reaction with the substrate yields free atoms (F), while molecular interactions result in polymer products [35]. Wafer surfaces have sites for the adsorption of some of these species. A chemical reaction takes place and the products are subsequently desorbed due to volatility and/or ion bombardment.

Most halocarbon gases etch under conditions at the limit of polymer formation which can result in trapped back scattered metal contaminants. Surface damage and charge trapping can also occur. These problems can be reduced or eliminated by post etch anneals, appropriate etch sequences or backside gettering [35].

2.3.2.4 RIE PROCESS PARAMETERS

The key characteristics of RIE, such as rates, selectivity, resolution, profile and uniformity, can be controlled by several parameters. The individual effects of these parameters on the microscopic attributes, e.g. particle energy, gas phase chemistry, surface chemistry and electrical factors, are difficult to assess since their interactions are complex [35]. The effects of various parameters have been reviewed by Gorowitz [35] and are summarised below

The etch rate is dependent on the rate of generation and consumption of active species and the rate of removal of reaction products. At low flow rates, there is an inadequate supply of etch species, resulting in low etch rates. Etch rates increase rapidly with increasing flow rate, up to a maximum. Rates then decrease, despite a continued increase in flow, due to decreased residence times for the etching species, i.e. the active species are pumped from the system before they have time to react. The ratio of effluent : input gas flow is referred to as the utilisation factor. This factor is related to surface area, meaning that etch rates show an area dependence, known as the 'loading effect' where [13]:

$$R = \frac{G}{n}\left\{\frac{\tau k}{1+\left(\frac{\tau k A}{V}\right)}\right\} \qquad (2.13)$$

G = Generation rate per unit volume and time.

R = Etch rate.

n = Number of atoms per unit volume of layer being etched.

τ = Recombination rate.

k = Reaction rate constant.

A = Surface area to be etched.

V = Volume of plasma.

The loading effect is particularly relevant where different numbers of wafers are input in batch reactors or there are differences in the exposed area across a single sample causing local etch rate variation, underetching can also result [13].

Etch rates generally increase monotonically with applied power since this affects the electron energy distribution which, via collisions, affects the generation of active species [35]. Increased power can compensate for decreased residence times in conditions of high flow, but can result in photoresist degradation, increased loading effects, etch non-uniformity, substrate heating and bombardment damage which subsequently affects anisotropy, selectivity and etch rates [35].

As the pressure increases in an RIE system, residence time and collision frequency also increase, but mean electron energy decreases and, since the latter determines the rate of active species generation, etch rates decrease [35]. At high pressure, the flux ratio of atomic : ionic species increases which enhances the chemical component of etching, reducing anisotropy [35].

Since wafer temperature affects reaction and product formation rates, the reaction rate exhibits a temperature dependence, despite the fact that a significant amount of the activation energy is provided by ion bombardment [35]. Typical chamber temperatures are 40 °C with the wafer carrying electrode typically partially thermally isolated from the chamber by an independent heat exchanger system. At higher temperatures the chemical and therefore isotropic aspects of the etching are enhanced. However, for an unsupported wafer, RF power and reaction heats can produce typical temperature rises of 100 – 200 °C in a 75 mm diameter wafer [35]. The thermal stability of the resist and the ability to cool the wafer surface are therefore important process considerations.

The electrodes, particularly the cathode, need not be inert but their chemical interaction will affect such parameters as etch rate, uniformity and loading. Stainless steel or other metal electrodes can slow rates and cause heavy metal contamination or form localised masks. Teflon, carbon and silicon cathodes stimulate the release of fluorine which reduces carbon build up in the chamber. During etching the electrodes and chamber walls can become coated with chemically inert films of involatile halides, oxides or even polymer reaction products. Ion bombardment may produce sputtering, redeposition and undetected changes in the coatings which then affect etching characteristics. A dependence on mask material is also experienced.

Chamber geometry also influences etching. A large electrode spacing increases etch rates and uniformity. Different etch gases of course have different effects. CF_4 etching leads to a CF polymer film which inhibits etching, SF_6 etching causes deposition of an SF_2 film with a lesser but similar effect, while NF_3 results in no film deposition. The etched profile has also been shown to exhibit a dependence on excitation frequency [36].

2.3.2.5 SILICON ETCHING

Mono and poly crystalline silicon can be etched using fluorine-based etchants e.g. CF_4, CH_3F, CF_4/O_2, SF_6, C_2F_6/O_2 and NF_3. These mainly produce the volatile products of SiF_2 and SiF_4 [13]. Oxygen addition (1 - 10 %) to some fluorocarbons increases the silicon etch rate [36]. Using CF_4 as an example, the oxygen is thought to react with CF_n^+ to form CO or CO_2, releasing the fluoride ions to react with silicon. However, this can result in excessive undercutting [35]. Anisotropy can be achieved by decreasing the fluorine atom flux or increasing the ion energy, but the silicon : silicon dioxide selectivity is reduced. For example, SF_6, combined with a fluorine atom reducing electrode material, etches silicon anisotropically [35]. The addition of nitrogen to SF_6 enhances the photoresist etch rate but the silicon etch rate is increased much more [37].

Ion bombardment increases the silicon etch rate by the continuous volatilisation of fluorinated silicon, thereby exposing bare silicon to the fluorine atoms [35]. Without this effect, a moderately stable, fluorinated silicon layer would form on the surface. Ion bombardment is also thought to damage the silicon surface which allows the reactive species to etch these sites more readily [35].

For anisotropic, selective RIE of silicon, chlorine or bromine based gases can also be used [38]. With the addition of argon, helium or nitrogen, non-reactive ion bombardment is increased. After etching single crystal silicon in CCl_4, CCl_4/N_2 or CCl_4/O_2, pyramidal structures more than 1 μm deep are sometimes seen in unmasked areas [35]. This is thought to be due to deposition of polymeric residues or stacking faults in the silicon lattice acting as local masks. With gas compositions such as Cl_2, HCl, BCl_3/O_2, C_2F_6/Cl_2, ClF_3/Cl_2, CCl_3F, and CCl_2F_2/O_2, the pyramidal formations do not occur and etched features with vertical sidewalls are obtained. Bromine containing etchants include $CBrF_3$ and $CBrF_3/O_2$. Oxygen in the latter composition prevents dark rough silicon finishes due to the non-volatile products, and increases silicon : silicon dioxide selectivity [35].

With gases containing carbon, chlorine and fluorine, it is considered that since the carbon-fluorine bond is stronger than the carbon-chlorine bond, chlorine dominates the etching behaviour. Following etching, in some cases, there is a region of heavy

lattice damage roughly 100 Å deep. This can be considered as a region of amorphous silicon with a high void density and behaves differently from the bulk material [39].

2.3.2.6 SILICON DIOXIDE ETCHING

High selectivity over silicon is a frequent requirement of silicon dioxide etches [35]. Anisotropic, selective etching of SiO_2 or Si_3N_4 in CHF_3, CF_4 and C_2F_6 can be achieved at low pressure due to polymer formation [40]. Saturated fluorocarbons are common etches but with < 40 % hydrogen, the CF_4/H or C/F ratio is high, polymer formation dominates and silicon dioxide etch rate drops to an unacceptably low level [35]. Other etchants that control polymer formation are CHF_3/CO_2 and CHF_3/NH_3. When etching with CF_4, low pressure and exposure to ion bombardment lead to the inhibition of polymerisation. Polymerisation is affected by the H_2 level which reduces the F present. Fluorocarbons undergo sputter assisted reactions with the oxide lattice leading to the formation of volatiles e.g. CO, CO_2 and COF_2, which allows material removal to continue [35]. Where fluorocarbon species contact silicon or resist, there is no oxygen to react and etch rates are generally drastically reduced [35]. CHF_3 or CF_4/H_2 can achieve a silicon : silicon dioxide etch rate ratio of up to 1 : 30. SiO_2 and Si etch rates both increase with the addition of H_2 depending on the pressure, residence time and electrode material [35]. The addition of oxygen increases the F present and the etch rate is reduced [41]. When etching with CHF_3, the etch rates increase with power density for most materials but most dramatically with SiO_2 [42]. This can be used to enhance material selectivity. Often conditions providing high oxide : resist selectivity do not provide a high silicon dioxide : silicon selectivity and so a two step process is required [35].

2.3.3 COMPARISON OF WET AND DRY ETCHING

Both wet and dry etching techniques meet some of the criteria given at the beginning of section 2.2, but neither meets all. Wet etching offers the benefits of uniformity, economy and low temperature/energy environments. However, it presents handling and disposal problems, can cause suspended structures to stick to the substrate and is invariably isotropic [13]. It is for these reasons which have become more crucial with

the drive to smaller dimensions, that dry etching methods were developed, and are now widely used in fabrication. However, radiation damage, poor uniformity across the wafer and repeatability between subsequent wafers can be problematic [13]. High variation in etch characteristics can also be experienced from machine to machine. For microstructure fabrication, dry etching can be important to avoid the effects of stiction. In addition to environmental benefits, plasma etching offers high throughput.

The key advantages of reactive ion etching are the ability to etch features with high precision, selectivity and minimal loss of critical dimensions from a variety of materials. This can facilitate the production of specialised geometries, based on the controlled erosion of overlying materials causing deliberate changes in surface topography. Occasionally a deep dry etch is followed by a short wet etch to reduce contamination and radiation damage. The essential benefits of dry etching are lost in this last step, e.g. the ability to pattern accurately and anisotropically. However, stress and cracking at the sharp 90° corners from dry, and particularly reactive ion etching, can cause problems if the corners are not rounded by a wet etch [35].

2.3.4 ALTERNATIVE TECHNIQUES

Lift-off is a patterning alternative to etching which can be used to form images without etching. For lift-off, a material layer is deposited on a previously patterned resist which is then removed in a solvent. The solvent dissolves the resist. Where the material was on it, this is also removed [13]. In the windows of the original photoresist layer, the deposited material is directly on the structural layer below, where it remains unaffected by the solvent as shown in figure 2.11. Disadvantages of lift-off are round topped profiles where shadowing has occurred, temperature limitations to below 200 - 300 ^{o}C, low repeatability and poor process control [7]. Ultimately, control of minimum dimensions is dependent on the ability to deposit material into resist openings. For lift-off, the top edge of an image should extend beyond the remainder of the layer. This allows solvent access to the photoresist sidewalls after layer deposition on top of the resist. Solvent treatment (e.g. chlorobenzene) and multilayer resists can be used to control the resist profile for lift-off [13]. In research and small scale production, lift-off can prove the only practical way to fabricate structures.

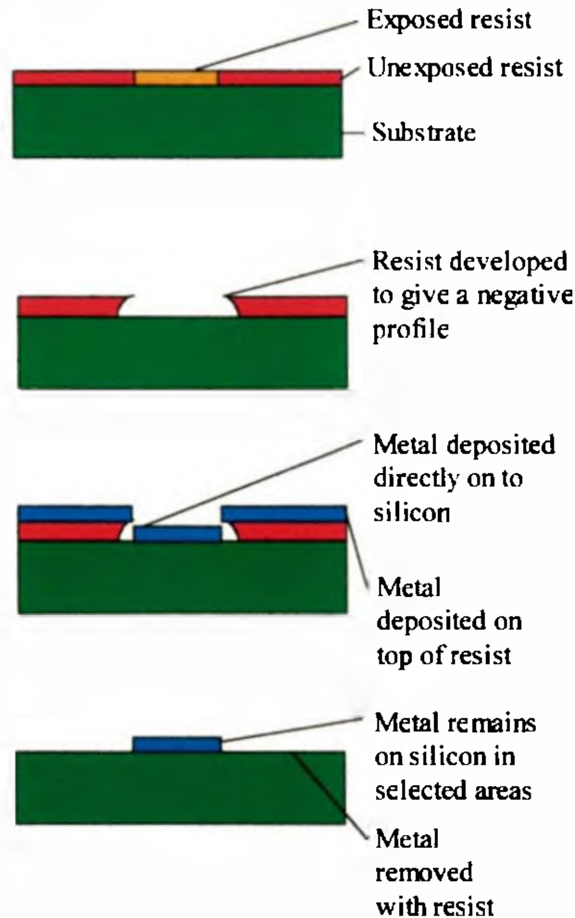


Figure 2.11 Lift-off Process Sequence

LIGA (Lithographie, Galvanoformung, Abformung) is a specialised patterning technique which combines x-ray lithography, electroplating and micromoulding for the direct fabrication of structures with large vertical aspect ratios, typically 100 µm or more in depth [43]. Resist features are electroplated to give an accurate negative micro replica which, after curing, is either used itself or as a mould for polymer, plastic or ceramic structure formation [43]. However, LIGA is expensive as a synchrotron is required to generate the high energy collimated photons to enable complete exposure of the thick photoresist. Only a few such facilities exist worldwide. SLIGA (sacrificial LIGA) combines the above technique with sacrificial layers to allow the fabrication of suspended elements such as gears [43].

2.4 METALLISATION

Devices are of no practical use until connected to the outside world for power supply and communication purposes. This requires electrical contacts, so that voltages can be applied across the device and currents drawn from it. Contact pads and metal interconnects are usually deposited on the top surface of a device, with choice of metal dependent on the application [44]. There are several factors to consider in metallisation such as; metal/semiconductor adhesion, etch selectivity, ease of wire bonding and material degradation during high current or temperature operation [13]. Low resistance ohmic contacts are generally required, which exhibit straight line IV characteristics over the current and voltage operating range of the device [13]. The contacts must only transfer current to and from the semiconductor and should not play an active role in the device operation, for example by current injection [13]. Contact resistance can be controlled by degenerate doping of the semiconductor-metal interface region. Ohmic contacts are typically formed by a two step process. Initially a heavily doped region ($> 10^{19}$ cm^{-3}) is formed on which the metal contact is deposited. This allows a wide choice of material systems [13]. Device contacts and interconnections may be provided by single or multiple metal systems [7]. Multilayer contacts are clearly more complex and expensive than single layer contacts and are therefore reserved for situations where the latter perform badly. An alternative is the use of multilevel contacts which are typically 2 - 4 material layers deep. This type of contact provides design flexibility by giving more surface area for connection, but complexity and the need for planarisation are increased. The technology relies on the ability to deposit and pattern, at low temperature, high quality insulating layers between the metals. Temperature cycling should be withstood while maintaining electrical integrity and connection to terminals should be easily achieved. The physical and chemical characteristics of a metallised contact are intimately related to the performance of the final device.

Difficulties can arise from:

(i) Thermally induced chemical reactions at the metal/semiconductor (or metal/metal interfaces in multi-metal systems) can ultimately cause device failure. An example of this is 'purple plague' which can occur in aluminium/gold systems. Also at high temperatures metals can react and lose their definition by decomposition or mechanical failure [44].

(ii) Interdiffusion at boundary regions, in which metal atoms diffuse into the semiconductor and semiconductor atoms into the metal. This phenomenon is enhanced by high temperatures and power.

(iii) Electromigration, where metal is transported under the influence of current flow. This results in void formation at one end of a metal interconnect with globule build-up at the other, resulting in open circuit and short circuit conditions respectively. This problem has been exaggerated by the very high current densities present in metal conductors caused by continually reducing device dimensions [13].

The problems of electromigration can be reduced by using a metal with a large diffusion and activation energy, for example gold. At the same current density and temperature, the mean time to failure (MTTF) for gold is typically 23 - 40 times that of aluminium. However, due to the poor adhesion of gold to silicon, an intermediate layer such as Cr, Ta or Ti is required [13]. For this purpose, spin-on glasses, e.g. polyimide, CVD layers with high conformation and reflowed sputtered layers have been used. This type of contact is very complex and is used only in specialised cases. A review of various metallisation schemes has been carried out by Murarka [44] and is summarised below.

2.4.1 TYPES OF METALLISATION

2.4.1.1 POLYSILICON

The properties of deposited polysilicon films and process induced changes to them are highly dependent on the deposition method. Ion implanted polysilicon is generally used to achieve good linewidth control despite its instability at high temperatures due to a needle like grain structure.

2.4.1.2 TUNGSTEN AND MOLYBDENUM

These have a low thermal expansion coefficient and resistivity and are definable in a variety of etchants. A common application is in multimetal systems and as gate metals

in MOS devices. Refractory metals (and their silicides) are sometimes employed to improve the reliability and performance of aluminium. These avoid reflectivity and electron mobility concerns. They can be evaporated, sputtered or deposited by CVD methods. However, adhesion to silicon, polysilicon and silicon dioxide is poor without an intermediate layer or the use of sputter embedding. These metals are unstable during oxidation and their high melting point results in low diffusivity and small grain size. Annealing or deposition of overlayers can control this. Tungsten applications are widened by the ability to selectively deposit it, allowing its use for metallic plugging [45].

2.4.1.3 COPPER

For copper, the use of adhesion promoters, increased energy in deposition or surface pretreatment is essential. Copper displays low resistivity, heat of formation and reactivity, high diffusivity and deep levels in silicon resulting in lifetime degradation. Concerns include dielectric compatibility in adhesion, diffusion, etching, deposition, contamination and electromigration.

2.4.1.4 SILICIDES

All silicides operate at higher temperatures than aluminium but can be restricted by the eutectic temperature. Silicides are normally formed by the deposition of a refractory metal onto poly or monocrystalline silicon, followed by sintering and removal of unreacted metal. If aluminium is then deposited, a clean interface with no spiking results. However, trace levels of water and oxygen must be rigorously avoided in silicide formation, which is therefore normally conducted under vacuum conditions. Alternatively, films may be co-deposited by evaporation, sputtering, or CVD. For a given silicide, sputtered films have a 50 - 100 % higher resistivity than sintered films due to higher electron mobility resulting from larger crystals. $CoSi_2$ offers the lowest resistivity, is thermodynamically stable and not affected by processing conditions below 900 °C. However, it consumes much silicon in formation. PtSi and Pd_2Si consume minimal silicon in formation but have poor high temperature stability. WSi_2, $MoSi_2$ and $TaSi_2$ have become popular for small devices. They provide high

temperature and oxidation stability. WSi_2 and $TiSi_2$ are preferred silicides as they can be co-sputtered. A typical multilayer contact is formed by the sputtering of Ti followed by W and Al, with a subsequent nitrogen anneal. Other silicides, e.g. $TiSi_2$, offer lower chemical resistance which gives reliability concerns.

2.4.1.5 CHROMIUM

Cr (and Ti) have low barrier height and so form ohmic contacts with moderately doped silicon. Adhesion to insulator surfaces is good and a common use is in multimetal systems with gold. Chromium is normally E-beam evaporated and can be readily etched, following removal of a thin passivating oxide film.

2.4.1.6 PLATINUM AND PALLADIUM

These are commonly used to form shallow junctions for Shottky barriers and ohmic contacts. Palladium avoids the water free deposition complexities of silicides, is easily deposited and readily etched in a number of common solutions. Etching of platinum can be carried out in dilute aqua regia (3HCl : $1HNO_3$ by volume).

2.4.1.7 SILVER

Silver is commonly used with titanium in multilayer systems, for Schottky devices. It is etched in basic or acidic solutions. Silver, however suffers from migration problems.

2.4.1.8 GOLD

Gold is ductile, weldable, readily deposited by vacuum evaporation and patterned in aqua regia or $KI/I/H_2O$ which are compatible with a photoresist mask, or cyanide based etchants. The resistivity of thin film layers is almost equal to that of bulk. Gold is used in multilayer connections with chromium, titanium or tantalum. These form

intermetallic compounds on subsequent high temperature processing. This inert metal can tolerate high current density and temperature without being subject to corrosion or electromigration. However, its inert nature inhibits adhesion by chemical means, precluding its single layer use and lifetime degradation can result from the use of gold.

2.4.1.9 ALUMINIUM

Aluminium, alone and as an alloy (e.g. with copper) is used extensively for device metallisation due to its low resistivity (2.7 x 10^{-8} ohmm^{-1} and 3.5 x 10^{-8} ohmm^{-1} respectively), good adhesion to silicon, silicon dioxide and silicon nitride and ease of deposition [6]. Aluminium ohmic device contact formation is a simple, repeatable, reliable, low cost technology [13]. Aluminium is compatible with gold which is commonly used in wire bonding for package connection and can be readily deposited and etched.

Aluminium/silicon mixtures exhibit eutectic characteristics, i.e. when mixed, the melting point of the mixture is below that of either metal alone, this restricts its use. Spike formation can be a particular problem with aluminium contacts on silicon [6]. Where aluminium is in contact with silicon it will dissolve into the silicon at the interface during the high temperature annealing step. The amount dissolved is dependent on the solid solubility of the materials. The volume of silicon consumed by aluminium can be calculated by equation (2.14) [6]:

$$Volume\ of\ silicon = 2\sqrt{dt}(HZ)S\left[\frac{\rho Al}{\rho Si}\right] \qquad (2.14)$$

d = diffusion coefficient for silicon in deposited aluminium films
t = anneal time
H = silicon height
Z = silicon width
S = solid solubility of silicon in aluminium at the anneal temperature
ρ = density

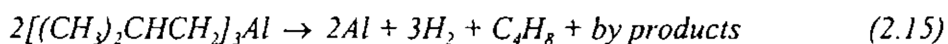
Due to the tendancy for spiking and electromigration in addition to its low melting point (660 °C), aluminium is limited to applications with post processing temperatures below 450 °C [44]. A current density above ~ 109 Am^{-2} in aluminium used alone is sufficient to promote electromigration. This effect is dependent on the metal deposition method, linewidth and crystal structure. It can be reduced by the addition of ~ 0.5 wt% of copper, dielectric encapsulation or film deposition in an oxygen atmosphere. An addition of 4 wt% of copper can raise the mean time to failure (MTTF) by a factor of 10, but corrosion and dry etching considerations limit the maximum addition to 2 wt%. A further disadvantage with aluminium is its electronegative nature which makes it prone to corrosion despite its natural oxide protection. It is also soft and therefore easily physically damaged. These drawbacks can be addressed by chip coverage in Phosphosilicate glass (PSG) or silicon nitride, with windows to access the bond pads improving yield and reliability.

Typically, mixtures containing 1 wt% of silicon are used depending on the maximum process temperature. Single layer ohmic contacts are formed by heating aluminium after deposition to a temperature just below its eutectic temperature. Since the aluminium only truly contacts the substrate at discrete points, these are under considerable pressure resulting in melting below the eutectic temperature. Melting causes bonding at a number of localised points which allows stress relieving plastic flow of the aluminium and a lower resistance than if the full area were in intimate contact. In practice however, instead of uniform dissolution, the aluminium penetrates the silicon deeply at a few points forming spikes. This spike formation due to differential transport of material in the semiconductor is known as the Kirkendall effect [13]. The spikes are pyramidal on (001) silicon and appear as characteristic rectangular etch pits in the semiconductor surface which are most prevalent in regions of high stress, e.g. at the edges of windows. The effect can be minimised by co-evaporation of the silicon and aluminium to satisfy the solid solubility requirement or by deposition of the aluminium on a layer of polysilicon or barrier metal e.g. TiN (which is stable under anneal conditions of 550 °C for 30 mins). This forms a low contact resistance and the silicon does not react with the aluminium

The solid solubility of aluminium is such that during contact formation the silicon freezes out epitaxially as an extension of the semiconductor substrate, followed by a region of polycrystalline aluminium/silicon alloy and finally pure aluminium metal.

The nett result is a highly doped p^+ region formed in the silicon with connection made to the pure aluminium via an alloy layer. The aluminium and p^+ silicon form a tunnelling Schottky junction with dissolution of the trace oxides, precluding the need for the extensive cleaning procedures normally associated with junction formation [44]. In the Al / n^+-Si system the initial resistivity is high but decreases with heat treatment as does contact resistance [44]. Provided that temperatures are limited to below 200 °C, no spikes are formed. On a silicon dioxide surface, the insulating native oxide layer is reduced and Al_2O_3 formed, resulting in low resistance and strong bonding. On silicon nitride, the mechanism is less clear but it may again be due to the formation of a thin surface oxide [13]. In multilayer metal contact systems, if the first layer is aluminium, sputtering maybe required to remove the native oxide (Al_2O_3) to allow the subsequent layer to adhere properly [13].

Common techniques for aluminium deposition are: evaporation, sputtering and chemical vapour deposition. Aluminium can be evaporated [13] with low contamination under conditions of low pressure, at a typical rate of 6000 Åmin^{-1}, and, if the substrate is heated to 300 °C, step coverage is promoted [13]. Sputtering increases step coverage and so is preferred for undulating surfaces [13]. The deposition rate is typically 1 μmmin^{-1}. Aluminium also can be CVD deposited by the pyrolysis of an aluminium alkyl such as triisobutyl alcohol which decomposes to aluminium hydride and isobutylene at 260 °C in the following reaction [6]:



$$2[(CH_3)_2CHCH_2]_3Al \rightarrow 2Al + 3H_2 + C_4H_8 + by\,products \qquad (2.15)$$

The catalyst $TiCl_4$ vapour is generally included prior to deposition and heating in silane is used for the alloying step. The resulting layer has a conductivity 90 % that of bulk and excellent coverage. Aluminium can be deposited by LPCVD (low pressure chemical vapour deposition) and subsequently alloyed with the silicon in the same equipment, resulting in high throughput and good film properties such as electron migration resistance, step coverage and film smoothness [7].

Once deposited, aluminium can be easily patterned to form the required contact pads and interconnects. Wet etching of aluminium can be carried out using a mixture of H_3PO_4 and HNO_3 with or without CH_3COOH (or less commonly in $K_2Br_4O_7$, KOH or $K_3Fe(CN)_6$) [44]. Lift-off is also sometimes used for aluminium definition. In reactive

ion etching of aluminium, hygroscopic residues may form which draw moisture from the environment. This corrodes patterned metals and forms by-products. Aluminium can be dry etched using BCl_3 and CCl_4 without corrosion or attack on other layers [13].

2.5 DIFFUSION AND ION IMPLANTATION

The electrical characteristics of silicon can be altered in a controlled manner by the introduction of impurity atoms or dopants into the crystal lattice [6]. This is a key technique in semiconductor processing and is generally achieved by either diffusion or ion implantation [6]. The requirements of doping are, in common with most other process steps, high throughput, uniformity and dose control with low process temperature and contamination levels along with compatibility with standard processing materials.

To compare the two techniques, ion implantation tends to result in sharper doping profiles with lower levels of contamination and good control over a wide range of doses [13]. It is considered most suitable for smaller geometries and local area doping. Several separate implant steps with different parameters (e.g. ion energy, substrate temperature) can be combined, allowing the production of dopant profiles which are unobtainable by diffusion methods. The low temperature of this process ensures existing dopant profiles are not altered and allows greater variety in masking material e.g. photoresist can be used without cross linking occurring [13]. The lateral penetration with implantation is lower than for diffusion allowing higher dimensional control of structures. Disadvantages of ion implantation are, high energy and high beam currents which can cause damage and the need for sophisticated, expensive equipment [6].

2.5.1 DIFFUSION

The diffusivities of common dopants are less in silicon dioxide than silicon. An oxide layer can therefore be used as a mask usually ~ 1 μm thick. At the mask edges some lateral diffusion occurs. The most

common silicon dopant is boron which results in p-type material, arsenic and phosphorus are used as n-type dopants. These three elements are all highly soluble in silicon, typically > $5x10^{20}$ cm^{-3}. The typical carrier concentration (n) in silicon is $5x10^{18}$ cm^{-3} at 1000 °C [6]. If the dopant concentration is < n the region is said to be intrinsic if it is > n, then it is extrinsic. An abrupt doping profile is a normal requirement.

When boron is used in silicon it acts as a donor, causing vacancy diffusion with a coefficient that varies linearly with dopant concentration [13]. Boron has a diffusivity of 10^{-12} cm^{-2} at 1200 °C and high solid solubility. The misfit factor is 0.254, consequently large amounts of boron held in the silicon lattice result in strain induced defects and considerable crystal damage. This sets the practical upper limit for doping as 5 x 10^{19} atomscm^{-3} from the reaction [13]:

$$2B_2O_3 + 3Si \Leftrightarrow 4B + 3SiO_2 \qquad (2.16)$$

Phosphorous has a diffusivity comparable to Boron, but a lower misfit factor of 0.068 [13]. However, the practical limit of phosphorus doping is an active carrier concentration of 3 x 10^{20} atomscm^{-1}.

In diffusion, the impurity atoms are thermally distributed. Rates are temperature dependent and increasing temperature allows atoms to penetrate the wafer surface faster. An inert gas containing the dopant is passed over the cleaned wafer held in a quartz boat in a open furnace, typically with a 10 - 100 cm flat zone held within 0.5 °C of the deposition temperature in the range 600 - 1200 °C [13]. An alternative closed tube furnace can be used for low contamination diffusion but the tube must be broken for sample removal. The radial thermal gradients can cause dislocation and slip faults which can be minimised by loading and withdrawing the wafers at a slow rate of ~ 10 cmmin^{-1} [13]. Alternatively the temperature can be ramped once the wafers are in place with appropriate adjustment of diffusion times.

Liquid, solid, gas or planar sources are used to introduce the dopant into the system [13]. For solid (powder) types, oxygen or nitrogen flow increases uniformity. For liquid, e.g. trimethylborate, a carrier gas is bubbled through the liquid source in a chamber resulting in a saturated vapour. The process is easily initiated and terminated.

Gas, e.g. diborane (diluted with argon) is easy to handle but suffers from high toxicity, chemical instability, low concentration and poor uniformity across a batch and a wafer. Common solid sources are BN, As_2O_3 and P_2O_5, liquid sources are BBr_3, $AsCl_3$ and $POCl_3$ and gas sources are B_2H_6, AsH_3 and PH_3. These are reduced at the surface in a reaction such as [6]:

$$2As_2O_3 + 3Si \rightarrow 4As + 3SiO_2 \qquad (2.17)$$

Planar sources are held in solid form by a binder, as a wafer sized disc, impurity levels for a wide range of heavy metals are < 1 ppm. These discs are stacked with each acting as a source for the adjacent two wafers, as shown in figure 2.12. A carrier gas is often used to control transport and prevent back diffusion. The planar sources such as BN are typically preoxidised at 750 - 1100 °C for 30 minutes [13]. The limitations of this technique are the rate of dopant transfer and high sensitivity to traces of oxygen and water which results in the formation of a surface layer of boric acid. After appropriate planar source preparation to freshen the surface, doping wafer uniformity of 2 %, wafer to wafer uniformity of 3 % and run to run uniformity of 4 % can be achieved [13]. The use of halogenic dopant compounds, e.g. BBr_3, reduces heavy metal contamination and is therefore ideally implemented towards the end of a device processing sequence. Other means of achieving predeposition are spin-on sources such as organosilane compounds spun 5000 Å thick, which achieve good uniformity but poor control and LPCVD which introduces an extra step but avoids the need for uniform transport and allows selective doping [13].

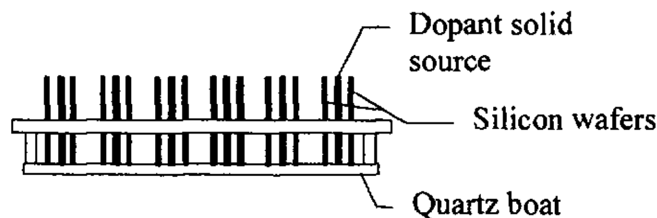


Figure 2.12 Diffusion with solid disc sources

Diffusion may occur under conditions of constant surface concentration, where the vapour source maintains a constant dopant concentration at the surface, or by constant total dopant diffusion, where a fixed amount of dopant is deposited on the surface and

then diffused. A two step process is common where predeposition involves the formation of a diffused layer under constant surface concentration conditions followed by the drive in or redistribution step under constant total dopant conditions in the diffusion furnace with an oxygen ambient [13]. The solid solubility determines how hot a wafer should be to achieve the required level of doping. Time is also a factor. For short diffusion times, there is high dopant concentration near the surface but this falls off rapidly. At longer times the dopant concentration below the surface is increased, resulting in a flatter profile [13]. The dopant concentration gradient causes the atoms to diffuse away from regions of high concentration. The concentration profile resulting from diffusion is a gradual one with the concentration decreasing monotonically from the surface in a distribution dependent upon temperature and diffusion time as described by Fick's equation [13]:

$$\frac{d\,C(x,t)}{dt} = D\frac{d^2}{dx^2}C(x,t) \qquad (2.18)$$

C = concentration at a distance x into the wafer and time t

D is a temperature dependent diffusion coefficient

Diffusion proceeds by the atomic movement of dopants in the crystal lattice via vacancies or interstitials [13]. Vacancy diffusion occurs due to the finite probability that a host atom will gain enough energy to leave its lattice site and become an interstitial itself, creating a vacancy. The neighbouring impurity then migrates to the vacancy. Interstitial diffusion is where an interstitial atom moves without occupying a lattice site. Atoms smaller than the host often move by this means. Group 1, 8 and transition metal elements generally diffuse by interstitial movement. Doped layers are typically evaluated by isotope tracing, junction depth, sheet resistance, CV reverse bias examination of a junction capacitance or secondary ion mass spectroscopy (SIMS) [6].

2.5.2 ION IMPLANTATION

During ion implantation the dopant species is introduced by a high energy ion beam and accelerated at high energy, depending on the depth of implant required. The

projected range for boron ions in silicon is ~ 3 $\mu mMeV^{-1}$. BF_3 is commonly used as a boron implant source. Collisions of electrons and neutral atoms produce ionised dopant atoms which pass through a mass separating analyser to an acceleration tube and on to the substrate. Ionisation is typically achieved by electrons supplied from a hot or cold cathode, an electronic discharge or an RF discharge. Ions incident on the substrate lose energy by collision with electrons and/or nuclei in the substrate before finally coming to rest. Boron, which is of low mass, mainly experiences electron stopping.

Typical ion implantation energies are in the range 30 - 300 keV with ion doses of 10^{11} - 10^{16} $ionscm^{-2}$ [6]. Collisions with atoms in the perfect crystal lattice can result in the creation of regions of amorphous material. The higher the ion dose the greater the resultant lattice disorder. This damage degrades carrier mobility and lifetime, and necessitates annealing to remove it [13]. During annealing, dopant reactivation occurs. However, significant dopant movement can occur in the anneal step which may alter the intended dopant profile. In general, heavy ions result in a small volume of considerable damage while light ions cause a large volume of slight damage. Typically, the peak ion damage region is closer to the surface that the ion concentration maximum. Isolated defects are harder to anneal out then heavily damaged regions where the damage/semiconductor interface gradually moves toward the surface during the anneal step [13]. A crude method for detecting severe damage is a reduction in surface reflectivity, giving the surface a milky appearance. Annealing is achieved in a furnace or with lasers at a temperature below the melting point allowing crystal regrowth along original crystal planes to rebuild the lattice. Annealing conditions are material and device specific but annealing achieves only partial recovery of parameters such as lifetime and mobility. Generally at 400 °C, cluster disorders are removed with a 20 - 30 % recovery of electrical properties and at 550 - 600 °C epitaxial regrowth occurs for boron and 900 - 1000 °C anneal temperatures lead to full activation [13]. Laser anneals reduce contamination, wafer warpage, lateral diffusion and dopant activation but limits process sequencing. Solid or liquid phase epitaxy can be carried out with IR lasers, cold processing with a pulsed laser keeps the substrate at ambient temperature and the dopants are frozen into place in the lattice. Rapid thermal annealing is also an alternative. This reduces dopant redistribution and takes just 10 seconds at 1000 °C using switched incoherent heat sources and point supports [13]. The implanted layer typically has a uniformity of

< 1 - 2 % and a reproducibility of 0.5 - 1 % from wafer to wafer [7]. The beam is often scanned and/or rotated to further increase uniformity and minimise process temperature. High temperature resists and wafer cooling during implantation can increase implant quality, typically allowing 1000 W power to be applied with a dose of 10^{15} ioncm^{-3} without the wafer temperature exceeding 105 °C [7]. Preimplantation of an inert ion may be used to make an amorphous layer to allow close control of dopant profiles and full dopant activation at low temperatures. For deep implantations a series of implants at varying ion energies and doses can be used. Implantation is carried out in order of decreasing temperature, to form a flat dopant profile.

Greater control is possible in implantation than with diffusion although shallow implants of light ions are difficult to achieve with precision [6]. The beam current is a function of ion source material, ion extraction method and machine design. A dopant concentration which peaks inside the semiconductor with a profile determined by the ion mass and implanted ion energy is produced. This can be further adjusted by the acceleration potential. This profile is typically Gaussian in form along the axis of beam incidence [13]. However, with boron, the profile is assymetric with the highest concentration region toward the surface. In addition to dopant implantation there are other applications of ion implantation in semiconductor processing such as dielectric formation.

2.6 OXIDATION

Silicon dioxide displays high stability and has excellent thermal and electrical insulation properties making it one of the most important materials in semiconductor devices. It has a resistivity of 10^{12} ohmcm and thermal conductivity of 1.4×10^{-2} Wcm^{-1} K^{-1} [46].

Silicon dioxide can be deposited readily by a number of techniques alone or with dopants [46]. The growth parameters for silicon dioxide are affected by the orientation of the silicon substrate. For example the <111> plane has the highest growth rate [13]. Amorphous or fused silicon dioxide have lower densities than the crystalline form (tetrahedral) which makes them more receptive to dopants [6]. Due to silicon dioxide's ability to flow at low temperature it is also used in planarising applications.

Silicon dioxide growth occurs naturally on silicon. A 10 – 20 Å thick silicon dioxide layer typically forms under conditions of room temperature and pressure [13]. Both temperature and pressure can be used to accelerate the growth rate in deliberate oxidation. Thermal oxidation can be conducted in a long quartz tube in an oxygen environment. The temperature is held at 900 - 1200 °C and the wafers are positioned within a central 'flat zone' with particularly high temperature control [13].

During the dry oxidation process, oxygen is passed over the wafer in a furnace at 950 - 1250 °C ($\pm$0.5 °C). The resulting silicon dioxide layer has a high uniformity and predictability of final layer thickness is good. A dry oxide of 1 μm thickness would be expected to grow in about 2.5 hours. For steam silicon dioxide growth, oxygen or nitrogen is used as a carrier gas which flows through a water bubbler at constant temperature at less than 100 °C [13]. The steam is created either by flash techniques, in which water flows onto a heated surface and steam flashes off from it laden with gas and passes into the furnace, or by torch methods in which the combustion of oxygen and hydrogen are used to produce water vapour. Steam growth is faster than the dry process and a film thickness of ~ 1 μm grows in ~ 1.5 hours [6]. The resultant oxide differs in structure and properties.

Regardless of the oxide growth method used, the mechanisms are similar, the oxygen dissociates, simultaneously reacting with silicon. The oxidation process begins at the surface, consuming atoms and then progressively, as the layer is formed, uses silicon atoms from deeper within the crystal, while oxygen diffuses through the growing oxide layer [13]. The rate of oxidation is limited by the reaction rate at the interface and the diffusion of new species through the already formed film. As the layer thickens the growth rate becomes non-linear due to the necessity to diffuse through an increasingly thick layer of oxide. A general rule for silicon dioxide growth is that it is 2.27 times the thickness of silicon consumed [13].

Since the compressive stress of a silicon dioxide layer can be as high as 1 GPa, and cannot be eliminated by annealing, it is most commonly used as a sacrificial rather than structural layer in microstructure fabrication. Thermal growth results in silicon dioxide of excellent quality but large stress due to volume changes which can result in mechanical warping. This is because silicon dioxide formation increases a given

silicon volume by as much as 45 % [46]. This, together with the slow growth rates, is prohibitive to thick film production by thermal growth. Other drawbacks of thermal oxidation are the probability of particle contamination from the wafer loading and unloading processes (this can be reduced by automatic loading) and the high temperature redistribution of impurity ions. Silicon dioxide can be grown by thermal oxidation for a wide variety of applications e.g. dielectric isolation or barrier layers. With small dimensions, lateral diffusion becomes a critical parameter for retaining device performance and conserving wafer area [6].

The thickness of grown or deposited silicon dioxide layers is commonly measured either by ellipsometry, which recognises changes in the polarisation state of reflected light, or by an optical interference fringe method, which relies on the interference of light waves returning from two interfaces, the air/silicon dioxide and the silicon dioxide/silicon interfaces [13].

Silicon nitride is used in some applications in place of silicon dioxide. Silicon nitride is highly durable, displays good thickness control and low dopant diffusion. The film can be deposited by LPCVD at approximately 750 °C or plasma enhanced chemical vapour deposition (PECVD), at around 300 °C [6].

2.7 FILM DEPOSITION

Film deposition techniques are of great importance in semiconductor processing, being used to form layers of many materials for a multitude of applications [13]. Thin films are the 'building blocks' of many device fabrication techniques and a baseline for surface micromachining with devices constructed from successive deposition and patterning of thin solid films (0.1 - 5 μm) [46]. Some of the most important film deposition techniques used in micromachining are briefly described in the following sections. Particular attention is given to sputtering, the technique which was investigated during the course of this project. The essential requirements of deposited films are listed below [13]:

(i) high uniformity

(ii) good step coverage

(iii) high material purity

(iv) good adhesion

(v) the ability to be deposited to a required thickness

(vi) controlled stress

The deposition technique must also provide good rates for sufficient throughput, economic viability, operator safety and a small equipment footprint.

Layers can be deposited by physical methods e.g. sputtering and evaporation or chemical means e.g. chemical vapour deposition [13]. Other methods of film formation include electrochemical deposition, screen printing - common in hybrid electronics and spin casting of materials such as inorganic glasses [46]. Epitaxy is the growth of single crystal semiconductor layers upon a single crystal semiconductor substrate [6].

The final deposited film thickness can be confirmed with cross sectional SEM or Fourier transform infrared analysis (FTIR).

2.7.1 EVAPORATION

To deposit a layer by evaporation, the source material is heated in a high vacuum causing it to evaporate, the vapourised atoms and molecules are then deposited onto a wafer [13]. The equipment consists of a vacuum chamber, a substrate holder - which may be rotating, a crucible containing the material to be deposited and a shutter [46]. The benefits of deposition by evaporation are high material purity and equipment simplicity but it is difficult to control deposition parameters such as rate, grain size and composition. Adhesion and step coverage may be poor and there is often x-ray damage. A wide variety of metals: platinum, niobium, molybdenum, tungsten, titanium and tantalum can be deposited by evaporation. There are three heating mechanisms utilised in evaporation: resistive, inductive and electron beam as shown in figure 2.13.

Resistive heating is simple, inexpensive and wafers do not incur radiation damage. However, it is restricted to low melting point materials, short runs which results in thin layers and filament contamination [6]. Inductive heating achieves high deposition

rates while avoiding radiation effects but requires complex equipment and suffers also from crucible contamination risks [6]. Electron beam beating provides high deposition rates and allows the co-deposition of several materials in a controlled manner but does result in ionising radiation damage to wafers. A magnetic field is used to deflect the beam, screening impurities out [6]. During electron beam evaporation, high energy electrons strike a target made of the required deposition material. The electron energy is converted into heat which causes local melting and evaporation around the incident site of the beam [13]. The result is a region of high purity material inside the source.

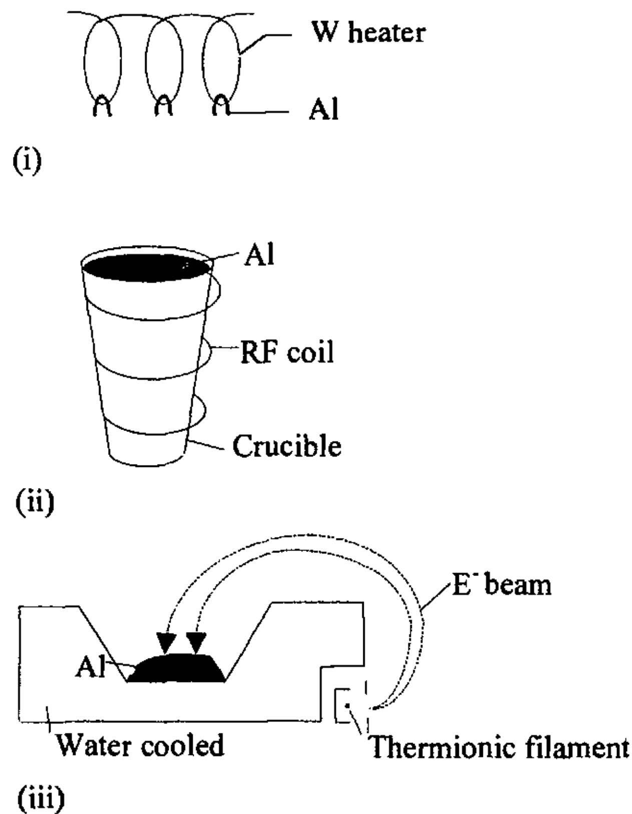


Figure 2.13 Heating systems in evaporation (i) Refractory wire coils, (ii) Inductive arrangement, (iii) E-beam evaporation [6]

Evaporation methods also allow the deposition of epitaxial films in a process known as Molecular Beam Epitaxy (MBE). This is an ultra high vacuum (10^{-10} T) evaporation process for the growth of very thin films, the environment is ultra clean to minimise defects and contamination, and controlled doping can be incorporated [6]. In this method an atomic or molecular beam of the film elements is generated from thermally heated crucibles containing the deposition material. These then condense on the

heated surface of a wafer forming an epitaxial layer. Substrates are placed face down to reduce contamination and rotated to improve uniformity, beam shape is controlled by an aperture between the crucible and substrate [7]. Several crucibles can be used with their temperatures computer controlled to achieve the desired film composition, real time monitoring of the film and growth environment can also be conducted [7].

2.7.2 SPUTTERING

Sputtering is a versatile method of material deposition and was the technique employed for aluminium deposition in this project. Sputter deposition can overcome many of the problems exhibited by evaporation methods, allowing improved step coverage at lower temperatures with less substrate damage [13]. The system includes a vacuum chamber, a metal target, a sample holder and a high voltage dc or RF power supply [46]. The chamber shape can be designed to optimise the number of ionising events [6]. Sputtering takes place in vacuum conditions (10^{-2} T) [13] with an inert gas (e.g. argon) which is ionised in an electric field produced by the application of a high voltage (2 - 6 kV) to form a plasma or slow discharge. Once the plasma is ignited, energetic ions are accelerated through the potential gradient. Positive ions are directed toward a cathode target material which they bombard with sufficient kinetic energy to remove its atoms by the transfer of momentum [13]. Atoms near the surface of the target become volatile and are transported as vapour to the substrate. The result is a continuous flux which condenses on the wafer. The energy and velocity of the atoms are reduced by numerous collisions. Increasing the pressure reduces the reflection of atoms from the substrate, increasing the deposition rate [13]. The different energies of incident ions define specific reactions at the target as described by table 2.1, which results in a cosine distribution of expelled atoms with a velocity range of $3 - 7 \times 10^5$ $cmsec^{-1}$. The minimum energy required to initiate sputtering is approximately equal to the heat of sublimation of the source. To minimise the energy required to eject target atoms, the process uses an ion energy within the range for which sputter yields of one atom per ion result [6].

Atoms from the source and impurity species condense on the wafer as a result of electrically attractive forces and attach to the surface by chemisorption and physisorption to form a complete film, atom by atom. Progressive film growth is

ensured by the naturally decreasing free energy of this system of molecular species. During sputtering the substrate undergoes mechanical motion so that all of the substrate is exposed to the same average number of sputtered atoms [6]. Sputtering provides good control of film properties such as grain structure, film stress, step coverage uniformity and alloy composition. The high energy of sputtering leads to high surface bonding. Sputtering is well suited to the deposition of multilevel contacts. In this case backscattering can be used to clean the chamber and wafer surface between each material deposition [13]. Stress and other mechanical properties of sputtered films are dependent on sputtering conditions. In addition, trapping of inert gases can lead to anomalies in the film characteristics [46]. Sputtering is commonly used for aluminium and its alloys, refractory metal silicides, gold, titanium/tungsten, tungsten, molybdenum, silicon dioxide and silicon. However, sputtering can also be used in conjunction with alternative materials, including organic and inorganic compounds, and several materials can be sputtered in controlled atomic ratios [46].

Energy	**Reaction**
2 eV	Physisorption
4 - 10 eV	Surface sputtering
10 - 5000 eV	Range of monolayer sputtering
10 - 20 keV	Ions driven into lattice structure

Table 2.1 Reactions at the sputter target

Radio frequency (RF) and magnetron sputtering are two common deposition methods. A typical radio frequency sputtering system consists of electrodes of alternating electric polarity to sustain continued expulsion of electrons from insulator surfaces. In one cycle of an RF waveform, enough electrons are emitted to sustain the required anode/cathode potential [13]. In magnetron sputtering, a magnetic field is used to concentrate stray electrons around a target resulting in a high current density of 10 - 100 $mAcm^{-2}$ see figure 2.14). This ensures that a large fraction of the sputtered atoms are ejected toward and deposited on the substrate (which need not be an electrode). Particles leaving the magnetic field toward the wafer cause ionising collisions instead of releasing redundant heat [13]. This provides high deposition

rates. A magnetron operates at a voltage below that of a typical electron beam source, leading to less penetrating radiation [6]. Backside wafer heating can be used to allow precise control of the wafer temperature.

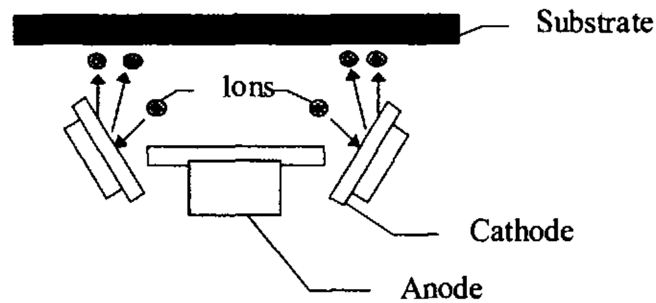


Figure 2.14 Typical magnetron arrangement [6]

2.7.3 CHEMICAL VAPOUR DEPOSITION (CVD)

In CVD, one or several gaseous species undergo pyrolysis (thermal molecular breakdown into components). Some of the resulting species contact the wafer surface where they undergo a vapour/gas phase chemical reaction, nucleate and grow to form a solid film [7]. A CVD reactor consists of a heated quartz tube, sample holder, pump and gas injectors [46]. Film growth is controlled by mass transport and is reaction limited which results in good film uniformity. CVD can be used to deposit polysilicon, silicon dioxide and metals as well as superconducting and magnetic layers [46].

The basic equipment is realised in several different designs. A hot wall reactor is similar to a silicon dioxide growth furnace with three heater zones sustaining high temperature (300 - 1000 °C) within a quartz tube [7]. The wafers are placed in a holder perpendicular to the gas flow. Batch processing allows high throughput (up to 200 wafers/run) and good film uniformity can be achieved although actual deposition rates are low, contamination can build up and flammable, toxic gases are generally involved [7]. A continuous CVD system is a conveyor on which wafers travel through a convection heated reaction chamber containing the reaction gases [7]. The parallel plate design is similar to a plasma etcher. Wafers are placed on a bottom (graphite or aluminium) electrode plate and the gas flows radially. An applied RF field initiates a

glow discharge at temperatures of 100 - 500 °C. Disadvantages of this system are low throughput and build up of contamination [7].

A specific form of CVD is epitaxial growth where a monocrystalline film is grown on a crystalline substrate. The layers fuse to form an extension of the substrate. CVD epitaxial growth is used widely in the formation of diaphragms [46]. Epitaxial films can be grown from solid, liquid or gas phase sources 0.1 - 100 μm thick with accurate doping levels [13]. There are two process requirements for silicon epitaxial growth [13]:

(i) Wafers should be tilted 2 - 4 ° off axis to expose the maximum number of crystal edges allowing matching to the existing lattice structure.

(ii) The wafer surface must have sufficient nucleation sites, which can be formed by 0.2 - 1 μm deep HCl etching which also removes any crystal defects.

The whole process takes less than one hour but parameters must be optimised to prevent misorientations or pattern shift. Lowering the pressure or changing reactant gas provide some degree of control over these factors. In batch CVD equipment, epitaxial silicon can be grown at temperatures from 900 - 1300 °C [13]. As with standard CVD, epitaxy suffers from the transport of reaction by-products to the surface together with the required chemical species which may affect film quality. In situ, highly controlled doping can be achieved by adding hydrides to the gas stream, or the reactant gas can be diluted with hydrogen [13].

Low pressure chemical vapour deposition (LPCVD) gives high film quality and controllable mechanical characteristics including low stress (following an anneal step). It also displays good step coverage, low cost and the wafer packing density is high. Maximum mass transfer rate can be optimised by increasing the reactant partial pressure, mean free path and reactant concentration in the gas stream. As a general rule, an LPCVD film etch rate increases with decreasing deposition temperature. Certain LPCVD techniques use UV light to decompose the reactants allowing a lower process temperature [6]. The UV photons have an energy which is below the gas ionisation energy to avoid charged particle device degradation. UV LPCVD also gives excellent step coverage, low mechanical thermally induced stress and low defect density [7].

Plasma enhanced chemical vapour deposition (PECVD) uses a plasma to decompose reactant gases so initiating the reaction [46]. The apparatus consists of a vacuum chamber, pump, two electrodes, gas inlet and RF source [46]. The chamber is evacuated to ~ 5 x 10^{-5} Pa and gas delivered at a few mT pressure. The plasma is struck resulting in many ionised species, some of which deposit on the substrate to form a solid film [46]. System cleanliness is of utmost importance. This is a faster and lower temperature process than standard CVD and allows more substrate versatility [46]. Stoichiometric control is difficult to achieve as trapped by-products are often incorporated in the films and these increase stress. Silicon dioxide and organic films e.g. polytetrafluoroethylene (PTFE), hexamethyldisilazane (HMDS) and resist are often deposited on non-planar substrates by tbis method [46].

2.7.4 PLATING

The plating of metals from solution is simple and inexpensive but produces poor film purity, thickness control and surface topography. In electrolytic techniques the wafer surface acts as the cathode and the metal to be deposited the anode. Plating occurs by the attraction of metal ions through an aqueous solution of salts by the electric field between anode and cathode. The deposition rate is controlled by the current density [45].

2.8 CONTAMINATION

Ensuring low contamination levels is paramount in semiconductor processing. The mechanical and electrical performance of a device is inherently affected by contamination [13]. Contamination may be organic, inorganic or metallic in nature and range from monomolecular films to particles from 0.1 - 0.5 μm in size, i.e. large enough to affect feature dimensions during photolithography [7]. Particle contamination results from operators, storage boxes, metal corrosion, equipment surfaces, handling tools, mechanical devices, cassettes, wafer friction, resist, chemical vapours, and scrubber brushes. Contamination may also be in the form of unwanted impurities, as-grown or from solutions, gases, air or glassware. In every stage of device fabrication, impurities can be incorporated inadvertently. This can be

minimised by the use of semiconductor grade chemicals and a high quality clean room [13]. The degree of contamination from processing is dependent on process time and temperature. During processing, efforts should be made to minimise contamination. Samples should always be handled with tweezers, vacuum wands and gloved hands. Contamination from diffusion is particularly common in open tube furnace systems. The quartz should be cleaned on installation and regularly during service [13]. Sensitivity to contamination can be so high that a monolayer of sodium can invert the surface of a 1 ohm silicon device [7]. Devices can often cost up to ten times their true price to accommodate the failures resulting from defects. Therefore on line examination is generally carried out. Various procedures can be used to control the problem of contamination and more sophisticated methods of analysis are continually being developed. Contamination can be detected for example by a surfscan which locates particles, fingerprints, haze, scratches, epispikes, cracks, pits, protrusions, slips and other surface abnormalities [7]. This method has micron scale resolution and a fast rate. Wafers are sorted into good and bad batches by comparison with the predicted angle of reflection of its laser beam.

Organic absorption can occur during wafer storage and handling. Organic films may result from resist or solvent residue, wax, fatty acid fingerprints, oils, lubricants, detergents and coolants [7]. These bond by weak electrostatic bonding or strong polar bonding which results in a hydrophobic surface detectable by atomisation or cold plate condensation [7]. Photoresist veiling and scumming can be readily detected by observing surface wetability after dipping [7]. Multiple internal reflection IR spectral studies have shown that a decrease in hydride coverage occurs over several weeks of clean room storage, but the fine structure (vibration modes) is destroyed due to surface oxidation after just a few days [47]. Hydrocarbons build up from the cleanroom air, reaching equilibrium after 5 - 6 hours. H_2 annealed or HF treated surfaces are less susceptible to this contamination. Hydrophilic wafers, i.e. those with a native oxide covering, demonstrate a higher uptake of organic contaminants than hydrophobic, i.e. those wafers which have been HF dipped [47]. In microstructure photolithography particularly, defects should be minimised, as this step forms the baseline for all subsequent processing. In all but one of the common resist removal processes tested [7], some residual remained. Plasma ashing was found to remove completely positive resist, while an ammonium hydrogen peroxide clean after gross removal left no negative resist. Spin coating can highlight contamination problems, a

seemingly perfect resist film can exhibit lifting, poor geometric control or undercutting due to an intermediate layer of water or other contaminant [7]. The brittleness of positive resist makes this type of contamination common, and wet removal tends to leave residues [7]. Alternatively plasma techniques can be used. These are often used for a short de-scum after developing to avoid veiling [7]. Time of flight secondary ion mass spectroscopy (TOFSIMS) and mass spectroscopy (MS), unlike multiple internal reflection infrared spectroscopy (MIR), can actually identify the chemical nature of contaminants.

Inorganic contamination e.g. Na, K, Ca ions and Au, Cu and Fe atoms arise from storage containers, process equipment, airborne salts and particles, corrosion, filtration and fumes [7]. These can bond very strongly by van der Waals forces, hydrogen or covalent bonding, depending for example on the ionisation of the wafer surface and humidity. Metal contamination results also in electrical characteristic degradation in fabricated devices. Inorganic ions are more difficult to remove than organic [7], such that after HCl cleaning enough sodium can remain to cause inversion. Fluoride can be desorbed by a 3 minute rinse in hot water and chlorine by 2 minutes in water at room temperature [7]. Metal contaminants can best be cleaned in a hydrochloric acid/hydrogen peroxide or sulphuric acid/hydrogen peroxide mixes. Gold and copper can be removed by placing in heated hydrogen peroxide while iron can be removed by a 60 second 30 % HCl dip [7]. Water contamination is also problematic in lithographic processing [7], tending to form a barrier between the resist and substrate which can be removed by absorption, chemical conversion to ammonia by HMDS or dehydration by in-line heating chucks, IR, conduction or microwave sources [7]. Detection of inorganic contaminants can be carried out with SEM, transmission electron microscopy (TEM), atomic absorption spectroscopy (AAS), x-ray analysis (XRA) or spark emission spectroscopy (SPS), but methods for their removal are not very effective [7]. Iron, sodium and potassium contamination due to skin salts resulting from touching of wafers can lead ultimately to surface leakage failure of devices. Diffusion, oxidation and deposition steps can all drive metal ions into the matrix, making cleaning prior to these steps essential [7]. Total reflectance x-ray fluorescence can be used for detection although this is only sensitive to some metals. A greater range of metals can be detected by infrared. The technique is combined with vapour pressure decomposition using synchrotron radiation or

polysilicon encapsulation. Secondary ion mass spectroscopy (SIMS) can also be used and is suitable for sample sizes which are smaller than whole wafers.

Almost all chemicals exhibit one or more deep impurity levels in silicon, detrimentally affecting the electrical characteristics [13]. Deep impurities can be deliberately channelled away from active regions in a process called damage gettering which involves heat treatment, sandblasting or abrading of the back surface. This provides a ready supply of vacancies which acts as a sink for deep impurities, but can also produce high interfacial stress. Copper, iron and gold are important deep impurities as they diffuse rapidly through the lattice and have large solid solubilities. Copper and iron can be frozen out in cooling, leaving by a process of diffusion or being removed by doped oxide growth. Any remaining atoms condense around dislocations [13].

Wafer contamination can be minimised by good cleaning procedures. Typical methods are solvent rinsing, vapour degreasing and ultrasonic cold cleaning [13]. Wafer scrubbing is also a well established technique for particulate removal. Equipment may combine mechanical brush scrubbing where a meniscus of water and detergent rather than the brush are in intimate substrate contact with high pressure, 4000 psi jet cleaning together with wafer spinning and constant rinsing [7]. The brush rotates in opposition to the wafer to create lateral force while actuators ensure the application of constant pressure to remove particles from etched topographies. Brushless jet spray cleaning is most appropriate for hydrophilic surfaces. The nozzle should be close to the wafer and moveable across its entire area with multiple angles and constant pressure achieved by real time control. The disadvantage of high pressure spray cleaning is the damage caused to delicate structures, while both methods can suffer from static electricity build up [7]. Chemical cleaning can also be used to remove contamination such as sodium and potassium which cannot be removed by scrubbing. This method also removes the photoresist memory on reworked wafers. In comparison of cleaning equipment, it is noteworthy that sprays reduce the volume of chemicals required by 50 % compared with baths [45]. The RCA chemical cleaning procedure detailed in table 2.2 overleaf is effective with most contaminants currently recognised [48].

Clean	Composition	Action
1	1:1:5 to 1:2:7 of NH_4OH:H_2O_2:H_2O	H_2O_2 oxidises organic contaminants, while NH_4OH removes heavy metals by the formation of amino complexes.
2	1:1:6 to 1:2:8 of HCl:H_2O_2:H_2O	Aluminium, magnesium and light alkali ions are removed and replating of the substrate with contamination is prevented.

Table 2.2 RCA clean sequence [7]

Ultrasonic cleaning is highly effective and reliable, resulting in no scratching or etching [7]. It also minimises the volume of waste chemical. However, use of ultrasonic is incompatible with some microstructures as it results in the breakage of delicate features. This method relies on the activation energy of bubbles generated by sonic waves to dislodge particles as the bubbles collapse. The water is usually held at 65 °C and contains a detergent or non-ionic surfactant in low concentration so as not to impede the ultrasonic action [7]. Wafer movement increases efficiency and promotes energy generation from several directions allowing uniformity even with stepped surfaces. A subsequent wash cycle maintains the contamination in suspension and a dry in filtered nitrogen then removes the residual water [7].

Rinsing is best conducted by moving the substrate through a series of progressively cleaner water baths held at a temperature between 35 and 90 °C [45]. This is called cascade or overflow rinsing. To remove water without further contamination, heated, filtered nitrogen or centrifugal spinning are most appropriate. These can be performed in batch mode in a controlled environment. Solvents and air used for drying are themselves sources of contamination and evaporation tends to leave suspended particles on the wafer surface [7].

2.9 PACKAGING

Bonding is the connection, by fine wires, of device metal pads to package terminal

posts. Gold bonds readily to aluminium and gold pads by thermo compression bonding. 99.999 % pure gold wires are drawn from a spool and fed through a capillary, a sphere is formed on the wire end which is aligned with the pad and lowered [13]. Contact is enforced for a few seconds until a weld is formed. This results in some plastic flow to form a flattened spherical join. The capillary is then raised which draws wire from the spool to form a lead. The procedure is repeated with the opposite end of the lead over the terminal post followed by cutting of the wire near the substrate join. To assist the bonding process, high temperature 280 °C can be used or lower temperature of 100 - 200 °C in conjunction with ultrasonics. A disadvantage of this technique is the wire 'tail' which results. This can break off and move freely within the package with the possibility of causing device failure. Stitch bonding is an alternative procedure which avoids this [13].

Packaging is one of the most common problem areas with sensors, the primary issues concerning sensor packaging are discussed by Sze [46] and are summarised below. It affects quality, cost and lifetime and must therefore be considered right from the initial device design stage. Each sensor demands different requirements from its package, since it needs to allow transfer of the variable for measurement but protection from harmful environments. For example for devices to be used in the body, the package should protect the sensor from the environment and the environment from the sensor material i.e. avoiding toxic reaction products.

On-chip circuitry or multiplexing of sensors can relieve packaging and encapsulation requirements, improving yield and lifetime by reducing the number of failure points, namely leads and bonds. For multiple sensor systems, the number of outputs can be limiting [46]. Integrating a sensor can considerably increase the device cost but when the increased reliability, reduction in component count and their assembly and ease of packaging are taken into account, costs are normally comparable [46].

For electrical protection, packaging considerations are electrostatic shielding, moisture protection, interface adhesion, interface stress and corrosion. Moisture is a major cause of device failure. When it infiltrates a package it condenses on the components causing leakage currents with the ultimate consequence of electrical and mechanical breakdown.

In selecting package material, adhesion to the substrate is also vital. If voids occur, diffused water vapour will condense and electrolytic currents develop resulting in package damage and partial lift off. To enable good adhesion, surfaces should be fully cleaned to remove organic contaminants and particulates. A vacuum bake out prior to bonding is recommended and adhesion may also be promoted by various chemical agents or plasma treatments. Interfacial stress, due to a dimensional mismatch between the package and substrate resulting from swelling, shrinkage or temperature changes should be minimised. This can be achieved by using an intermediate layer of low elastic modulus material, e.g. silicone rubber, to allow strain relief.

Metals can be welded to ceramic or glass to form hermetic packages by resistive, E-beam or laser methods with a provision for electrical feed through. These are a barrier to moisture and ions. Where only short term use is anticipated, this expense is spared and polymeric encapsulants are used, sometimes with additives to change their properties. These are cheap and applied at low temperature. An additional layer of titanium, silicon nitride or carbon may be used to provide increased moisture protection. Titanium is light weight and corrosion resistant due to a low temperature protective oxide which forms. This makes titanium (and tantalum) popular, particularly for biomedical device packaging. For mechanical protection the considerations are rigidity, weight, size, surface roughness and shape for convenient operation, in addition to a structure which allows repair or replacement of disposable components. In semiconductor devices, light and heat shielding must also exist to avoid errors during operation. For a comparison of the capabilities of several common packaging materials see reference [46].

The total cost of a sensor is dictated mainly by the testing, calibration and packaging steps. Wafer level, hybrid and multichip modules are all packaging options. With high component density, 3D packaging is becoming increasingly necessary with support pillars, lead columns, and signal processing platforms.

2.10 SUMMARY

In order to design and fabricate pressure sensors effectively, a full understanding of the conventional technologies used in silicon processing was necessary. To allow this,

a literature review of lithography, etch, metallisation, doping, oxidation and film deposition technologies has been carried out and is summarised in this chapter. The importance of contamination and the constraints of sensor packaging have been acknowledged by the inclusion of a review of these topics. This enabled the correct choices to be made to proceed with fabrication using the most appropriate methods to achieve each stage of the process. In some cases, standard processes required adaptation for the particular needs of this application, with an awareness of the limitations of these deviations.

With the background to processing techniques provided by this chapter, the sensing structure can now be designed. The design must meet both production and performance requirements as discussed in the following chapter.

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CHAPTER 3: SIMOX PRESSURE SENSOR THEORY

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3.0 INTRODUCTION

Having surveyed the available technologies for fabricating the pressure sensor in chapter 2, this chapter addresses the design aspects of the novel structure developed during this work. The factors which determine the type, and design of sensor are briefly outlined. The basic operation of the capacitive pressure sensor is also described. A section on the sensor design introduces the criteria which must be satisfied by the sensor and describes how this has been achieved by the chosen design. An analysis of the diaphragm dimensions and design required to achieve the required performance is given and the expected performance and operational limits are calculated.

3.1 SENSOR TYPE

Pressure sensors have been the subject of considerable research and comprise 40 % of the total sensors market. However, there remains a gap in this market for small, low cost, high performance sensors for medical applications [1, 2]. This chapter describes the design of a pressure sensor for this purpose

A capacitive sensing method was selected for this sensor because of the characteristic high pressure sensitivity combined with low temperature sensitivity exhibited by this sensing method. The main alternative is piezoresistive pressure sensors where the diaphragm acts as a stress amplifier. However, these typically suffer from high temperature sensitivity resulting from a temperature dependent coefficient of piezoresistivity. Furthermore, Blasquez *et. al.* [2] have demonstrated by calculation that the pressure sensitivity of capacitive pressure sensors is always greater than that of piezoresistive sensors.

A monocrystalline silicon diaphragm was chosen for the sensor for its excellent mechanical properties which offer the benefits of low hysteresis, good stability and high mechanical strength. Polycrystalline silicon is the most commonly used alternative diaphragm material but this is affected by grain boundaries and internal stress which can result in hysteresis, non-linearity, fatigue and fracture problems. Where other diaphragm materials are used a mismatch in thermal expansion coefficient between the diaphragm and substrate can result in serious inaccuracies. In designs where pyrex bonding is used to provide a substrate, outgassing can result in errors. SOI was chosen as a starting material for the sensor developed in this work to allow the monocrystalline diaphragm to be fabricated using one sided standard IC compatible processing with a low number of masking steps. This provides the opportunity for future electronic integration. SIMOX was selected over alternative SOI substrates for the maturity of manufacturing technology, high material quality and well defined layer thicknesses. The Middlesex University Microelectronics Centre has a strong background in silicon-on-insulator technologies.

The diaphragm dimensions are discussed in detail in section 3.3; these are primarily determined by the characteristic dimensions of the SIMOX substrate which are effectively fixed, in combination with the pressure range of interest. For implantable

medical sensors, the pressure of interest ranges from around 10 mmHg (1.3 kPa) for intra-ocular [3] applications to around 500 mmHg (66.66 kPa) for cardiovascular applications [4, 5].

The above section is intended to summarize the main reasons for the selected sensing method and design of the device presented in this work. A detailed market evaluation, material analysis and comparison of sensing methods are included elsewhere in this thesis.

3.2 SENSOR OPERATION

The capacitive pressure sensor developed in this work was fabricated from SIMOX. This consists of an array of 2500 monocrystalline silicon diaphragms connected in parallel. Figure 3.1 shows a simple schematic of part of the device. Under an applied pressure, each diaphragm deflects causing the separation between the diaphragm and the substrate to decrease, resulting in an increased capacitance between the two plates. Insulation between the two capacitor plates is provided by the buried oxide layer. The use of an array increases the values of the undeflected and sensing capacitance, easing measurement and reducing the importance of stray capacitances. This also introduces a degree of tolerance to diaphragm redundancy. The small plate separation determined by the thickness of the SIMOX buried oxide layer provides overpressure protection to prevent diaphragm rupture, increases device sensitivity and reduces stray capacitance effects [6]. When the applied pressure is sufficient to result in a deflection (w) which is equal to the plate separation (d), then the diaphragm is in contact with the substrate. Under this condition the SIMOX structure could be used to function as an array of pressure switches (in the absence of an insulating layer).

In sensor fabrication the buried oxide is removed by lateral etching under the diaphragm to form the cavity. The buried oxide is accessed via a small, 3 – 5 μm etch hole in the diaphragm. This is subsequently sealed by a spin deposited photoresist plug which remains only in the region of the etch hole.

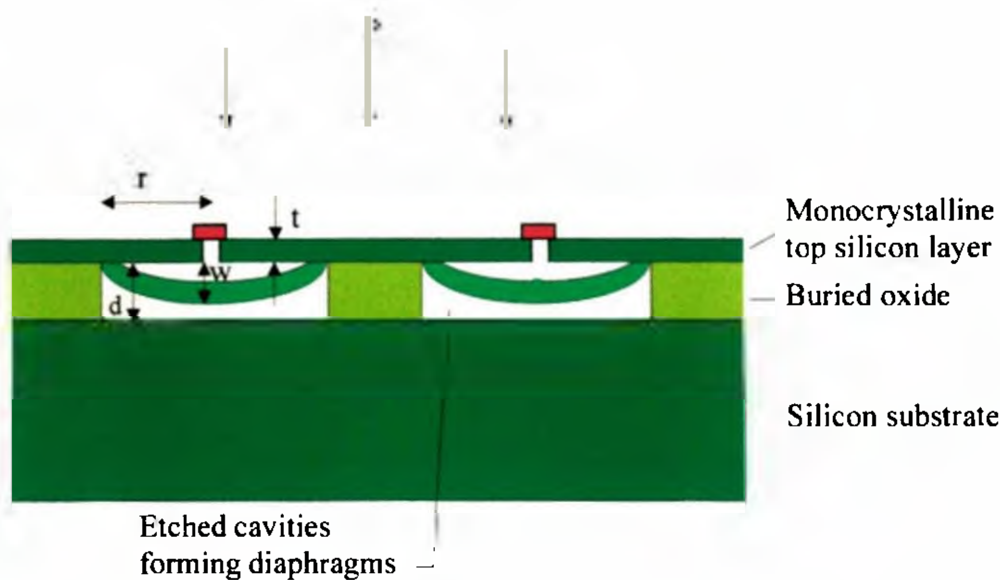

Figure 3.1 Schematic showing part of the SIMOX pressure sensor.

3.3 SENSOR DESIGN

Having established the appropriate type and material for the required sensor performance, the physical design must also be optimised. Typically a capacitive pressure sensor is designed to meet several criteria. These have been discussed by Mastrangelo [7] and the most important are:

(i) The sensor capacitance must be greater than a specified, measurable value.

(ii) The sensor must respond to the required pressure range and be capable of withstanding reasonable overpressure.

(iii) The electrostatic pull in voltage must be greater than the applied voltage.

The SIMOX material effectively fixes the vertical diaphragm dimensions which are conventional variables in sensor design, these are:

diaphragm thickness (t) = 0.2 μm

cavity depth/plate separation (d) = 0.4 μm

These parameters are controlled by the depth and width of the implanted oxide of the SIMOX substrate which are highly repeatable. This in turn, limits the possible diaphragm area resulting in a much smaller device than is considered typical. However scaling investigations have indicated that these typical dimensions can be further reduced [2]. More usual diaphragm dimensions are:

diaphragm thickness (t) = 1 to several 10's of μm

cavity depth/plate separation (d) $\geq 1\ \mu m$

Diaphragm areas are typically several square millimetres.

The wet, isotropic etch chosen to form the basis of the fabrication procedure, predetermined that the sensor would be circular (or oval – depending on the shape of the etch window). It is important to note that the circular diaphragms are a result of the isotropic etch as opposed to a photolithographic process, they are therefore 'perfect' circles. Circular diaphragms typically offer the benefits of higher rupture pressures and resonant frequencies compared with square designs [8, 9]. However, the latter typically show increased pressure sensitivity (rectangular diaphragms show lower pressure sensitivity than square [10]). Square diaphragms are more commonly used in pressure sensors than circular, therefore in the following sections the theoretical performance of square diaphragms will be briefly discussed to allow comparison of the two designs. In the following discussions two simplifications to the structure have been made:

(i) Isotropy of the elastic properties of the diaphragm material has been assumed.

(ii) The diaphragm has been treated as a complete circular diaphragm formed entirely of monocrystalline silicon, disregarding the central hole and plug.

Precise modeling of the plugged, anisotropic diaphragm would require computational modelling and is outside the scope of this thesis which is intended simply to provide performance estimates. For an analysis of the impact of these features the reader is referred to Timoshenko [11].

3.3.1 DIAPHRAGM DEFLECTION

The pressure-deflection characteristic is critical in sensor design. It is dependent on the diaphragm geometry, material, clamping mechanism and the size of the deflection [11]. The load has been assumed as symmetric about the axis perpendicular to the diaphragm through the centre. The deflection surface will then also be symmetric such that all points on the diaphragm, equidistant from its centre will have equal deflection. The sensor studied in this thesis can be described as a circular, elastic plate, clamped around the edges with a small deflection. In order for a diaphragm to be described by small deflection theory, its deflection must be less than or equal to half the diaphragm

thickness. In this case bending alone is considered and any diaphragm stretching can be neglected. Further assumptions and corrections for small deflection theory are given in Timoshenko [11]. Under these conditions the maximum deflection of a circular diaphragm which occurs at its centre, as a function of the applied pressure is given by equation (3.1) [2].

$$w = \frac{P(2r)^4}{85Dt^3} \qquad (3.1)$$

where

$$D = \frac{E}{(1-\upsilon^2)}$$

E = Youngs modulus (taken as 190×10^9 Nm^{-2})
υ = Poissons ratio (taken as 0.3)
other symbols are as defined in figure 3.1

Equation (3.1) illustrates that the deflection of a diaphragm under applied pressure is most strongly dependent on the diaphragm area, as deflection is proportional to the fourth power of the radius. Therefore the larger the radius, the larger the deflection. There is also a strong inverse dependence on the diaphragm thickness, the thinner the diaphragm the more it will deflect for a particular pressure. There is also a dependence on material parameters arising from Young's modulus which describes material stiffness and Poissons ratio which describes elasticity. This deflection is 3/8 of the deflection of a uniformly loaded bridge with a width of unity and length equal to the diaphragm diameter [11]. In deflection a diaphragm has two elements of energy. These are the strain energy due to bending and the potential energy of the load distributed over the surface.

Using the SIMOX material fixed dimensions of diaphragm thickness and cavity height together with a value of 66.66 kPa for the maximum applied pressure the expression for the deflection of a circular SIMOX diaphragm as a function of radius is:

$$w = 4.695 \times 10^{11}(2r)^4 \qquad (3.2)$$

This expression (3.2) has been plotted for a range of diaphragm diameters in figure

3.2. The solid line demonstrates the dependence of the maximum deflection on the diaphragm size for the circular design described above.

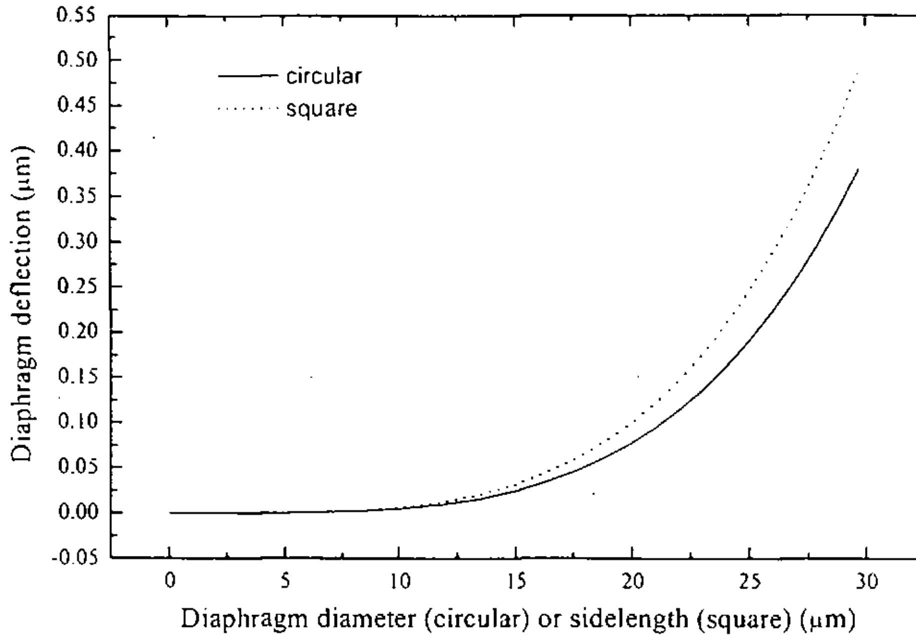

Figure 3.2 Graph showing deflection under applied pressure versus diameter for circular (solid line) and square (dotted line) diaphragms

Considering the above graph and the fabrication techniques to be used, a suitable diaphragm diameter of 17 μm was selected for the working, pressure sensor design. Using equation (3.2), the deflection of such a diaphragm at a maximum applied pressure of 66.66 kPa has been calculated as 0.0392 μm. This is 9.8 % of the maximum available deflection before the diaphragm contacts the substrate. This represents a versatility in design which will allow this structure to be suitable for use in alternative applications where the sensor is required to measure larger pressures.

The pressure-deflection characteristic for a square, elastic plate, clamped around the edges is given by small deflection theory [2].

$$w = \frac{Pa^4}{66Dt^3} \qquad (3.3)$$

where
a = diaphragm side length
other symbols are as previously defined

Equation (3.3) shows a similar dependence of square diaphragm deflection to the fourth power of the side length and inverse third power of the thickness. Therefore as with circular designs, the largest deflections will occur for large thin plates. There is also a dependence on the material properties. The relationship in equation (3.3) is described by the dotted line in figure 3.2. The curves show that the square diaphragms have a slightly higher sensitivity to pressure than the circular diaphragms. The difference in the absolute deflections of the two designs becomes larger with increasing diaphragm dimensions. For a square diaphragm of sidelength 17 μm, comparable in terms of all other parameters with a circular diaphragm of diameter 17 μm, the deflection under maximum applied pressure is 0.0505 μm. At this dimension the difference in the deflection of the square and circular diaphragms is small.

Each of the parameters in equation (3.1) has a variance resulting from process variations, preset tolerances or other manufacturing systematic errors. These contribute to an overall error in the deflection. It is therefore desirable to design a sensor which has low process variation to minimise the error in deflection and hence capacitance. Mastrangelo *et. al.* [7] have analysed the effect of process variations and systematic errors on the uncertainty in the deflection of capacitive sensor diaphragms. It is generally assumed that individual contributions to the total error are uncorrelated and the total error in deflection (ξw) is given by equation (3.4) [7].

$$\xi w \approx \left[16\left(\frac{\Delta(2r)}{(2r)}\right)^2 + 9\left(\frac{\Delta t}{t}\right)^2 + \left(\frac{\Delta d}{d}\right)^2 + \left(\frac{\Delta E}{E}\right)^2 \right]^{1/2} \qquad (3.4)$$

Equation (3.4) incorporates errors arising from both material properties and device dimensions. However, the variance in Young's modulus can be considered negligible due to the use of high purity, monocrystalline diaphragm material [7]. Variation in both the diaphragm thickness and cavity depth are small since these parameters are accurately controlled by the SIMOX material. For example, the variation in thickness

of the top silicon layer of a SIMOX wafer is typically ± 0.015 %. Therefore, as noted by Mastrangelo *et. al.* [7], the largest contribution to the error in diaphragm deflection arises from uncertainty in the diaphragm radius. In the current work, this is determined by the accuracy to which the underetch process can be carried out. An upper bound of ± 0.5 μm can be placed on the error in underetched dimensions, however, this value reflects the limitation in the microscope system used to measure the underetched cavities. The actual dimensional variation resulting from underetching using good temperature and time control, is expected to be considerably smaller. The variations discussed above would yield a maximum error in diaphragm deflection of around 12 %. This is reasonably low and results from a combination of SIMOX starting material, which incorporates well defined material thicknesses, and the well controlled, repeatable etch process developed in this work. As noted above, this value is likely to be a considerable overestimate of the true error in deflection, reflecting the limitation of the measuring system.

3.3.2 DIAPHRAGM CAPACITANCE

For the parallel plate capacitor model of the sensor, the capacitance of a single diaphragm is given by equation (3.5).

$$C = \frac{A\varepsilon_r\varepsilon_0}{d} \qquad (3.5)$$

where $\varepsilon_r = \dfrac{\varepsilon}{\varepsilon_0}$

A = Area of diaphragm
ε_0 = Permittivity of freespace
ε_r = Relative permittivity
ε = Permittivity of material between capacitor plates

For a circular capacitor plate of radius r, this can be expressed as:

$$C = \frac{\varepsilon\pi r^2}{d} \qquad (3.6)$$

Equation (3.6) demonstrates a squared dependence on the radius of the diaphragm and an inverse dependence on the capacitor plate separation. In application to the described pressure sensor, under no applied pressure the separation has been assumed as equal to the cavity height or the gap between the diaphragm and substrate. In operation with the diaphragm deflected by the application of applied pressure the separation (d) is equal to the initial cavity height minus the diaphragm deflection calculated from equation (3.1). Therefore it can be seen that the larger the diaphragm radius, the larger the deflection and therefore the larger the capacitance change will be. Under an applied pressure during measurement, the area of the diaphragm will not significantly change. Therefore the change in capacitance depends only on the diaphragm deflection. Taking as ε (for air) as approximately equal to ε_o in equation (3.6) the single diaphragm capacitance under conditions of no deflection (C_o) can be calculated as 5.02×10^{-15} F (5.02 fF). Under the maximum calculated deflection due to an applied pressure of 66.66 kPa, the capacitance can be calculated from equation (3.6) as 5.568×10^{-15} F. Hence the maximum change in capacitance under the maximum applied pressure is 0.548×10^{-15} F.

The small change in capacitance of 0.548×10^{-15} F calculated above is increased to a measurable value by the linking of many single pressure sensing diaphragms into an array. For an array of diaphragms connected in parallel, the output capacitance is described by equation (3.7).

$$C_\Sigma = C_1 + C_2 + C_3 + \ldots\ldots + C_n \qquad (3.7)$$

Where the number of single diaphragms in the array is 2500, the total base capacitance, C_o would be expected to be in the region of 12.55×10^{-12} F. The maximum change in capacitance for full applied pressure would then be of the order of 1.37×10^{-12} F. This capacitance change for the pressure sensing matrix can be expressed as a pressure sensitivity of ~ 0.02 pFkPa^{-1}. This sensitivity is considered measurable both for device testing and operation and is high compared with typical capacitance to pressure sensitivity values reported for similar devices such as 0.0008 pFkPa^{-1} [12]. This high sensitivity is a direct result of the small plate separation which is a consequence of the thin buried oxide layer. It is important to note that for the sensor described here the use of SIMOX allows for the integration of on chip circuitry for signal amplification if required. This can be readily achieved with

isolation of the electronics from the substrate provided by the buried silicon dioxide insulating layer. This is less true of many of the reported capacitive sensors which are fabricated on alternative substrates [13].

For comparison, a square diaphragm with a side length of 17 μm would show a slightly larger base capacitance C_0 of 6.39 fF, i.e. a total of ~16 pF for an array of 2500 such diaphragms. The higher value is due to the slightly larger area of the 17 μm sidelength square diaphragm compared to the 17 μm diameter circular diaphragm. For pressure sensing the important parameter is the change in capacitance obtained for a given change in pressure. For deflections of a plate, which are small compared to its thickness pure bending can be assumed [11], in this case the area of the plate remains constant. Therefore the difference in the change in capacitance under applied pressure between a square and circular diaphragm is entirely due to deflection of the plate. Figure 3.2 shows that deflection is slightly larger for the square diaphragm compared to the circular diaphragm. For an array of 2500 devices this results in a capacitance change for an applied pressure of 66.66 kPa of ~ 2.3 pF for the square design compared to ~1.4 pF for the circular design. However, if the 17 μm circular plate is compared to a square design of the same area (i.e sidelength ~ 15 μm) then the calculations indicate that the circular array could be expected to show a marginally larger capacitance change of 1.4 pF (circular) compared to 1.1 pF (square). Finally, it should be noted that the values quoted for the capacitance changes are likely to be slightly over-estimated since they are based on the maximum, central deflection of the diaphragm, not the mean. Given the assumptions which have already been made the simple treatment is sufficient for the illustrative purposes being considered here.

Modelling of square membranes has been carried out by Kovacs *et. al.* [8]; this showed that the sensitivity of a diaphragm can be increased by adjusting the design. Examples of this are shown in figure 3.3 where (a) the clamped area of a diaphragm is reduced and (b) 'slots' are cut in the diaphragm [8]. It is expected that similar adjustments could be employed with circular diaphragms to increase the pressure sensitivity. However in the case of the SIMOX diaphragm the sensitivity is considered sufficient for measurement, making these measures unnecessary.

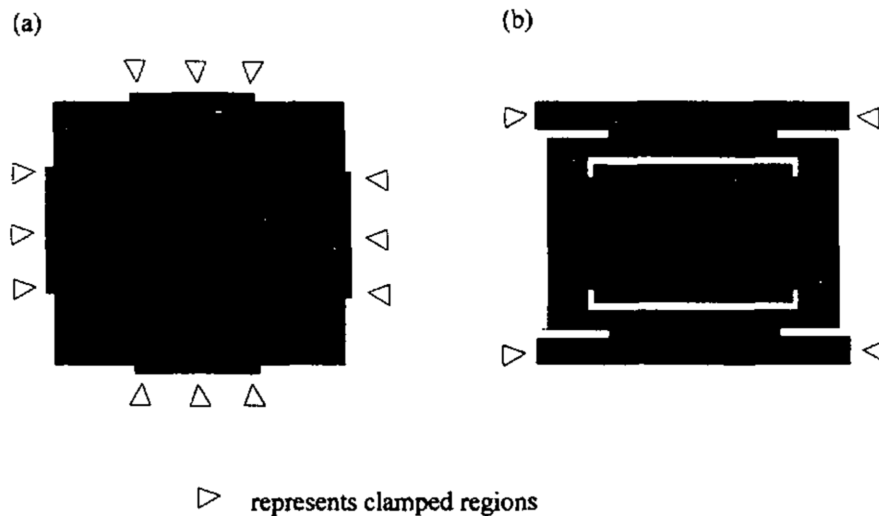

Figure 3.3 Examples of diaphragm designs which are reported to exhibit higher pressure sensitivity than a standard square, fully supported diaphragm [8].

The relationship between capacitance and plate separation described in equation (3.5) is inherently non-linear. However, the degree of non-linearity of a sensor's capacitive response to pressure can also be affected by the diaphragm design. In some cases response non-linearity can be reduced to less than 1 % [14]. For example, either strengthening the centre of the diaphragm or weakening its edges has the effect of stiffening the diaphragm and maintaining a higher degree of parrallelity between the capacitor plates than is gained for the standard structure. Corrugations in the edge of the diaphragm can increase the effective diaphragm length resulting in reduced diaphragm stretching which will also increase linearity. Contact of the diaphragm centre with the substrate has also been shown to cause the diaphragm to behave with increasing stiffness and therefore linearity. These effects can be used alone or in combination to increase the linearity of the sensor characteristics [14].

3.3.3 DIAPHRAGM STRESS

Stress is a critical parameter in the design of diaphragm pressure sensors. Stress can be internal due to the material or external due to the deflection under applied pressure. The level of stress depends upon several factors such as the diaphragm dimensions, material properties and the size of the applied pressure. If a stress is positive, it is of a

compressive nature. Where the yield stress or elastic strain limit is exceeded, the diaphragm will begin to display plastic deformation which means it will not return to its original dimensions when the stress is reduced. Under these conditions irreversible diaphragm buckling and/or long term shifts in the mechanical properties can result. Where the material rupture stress is exceeded the diaphragm undergoes permanent destruction [15]. At temperatures below 600 °C single crystal silicon exhibits no plastic flow, but, under tensile loading, fractures at 6 GPa. At temperatures above 600 °C, plastic deformation occurs for tensile loading above the yield stress. As temperature is further increased, the yield stress decreases as a result of higher dislocation mobility. The magnitude of the yield stress of silicon is also dependent upon the rate at which the material being strained [16].

Internal stress in a diaphragm can result from a mismatch in thermal expansion coefficients, grain growth and deposition processes. In general the internal stress in the plane of the diaphragm is much greater than the stress in the direction of the film thickness [17]. The internal, in plane strain, ε_i, is related to the in plane stress, σ_i, through the material properties of Young's modulus (E) and Poissons ratio (ν) by equation (3.8) [17].

$$\varepsilon_i = \frac{\sigma_i(1-\upsilon)}{E} \qquad (3.8)$$

It can be seen that a high stress corresponds to a high strain. The internal stress of a diaphragm or thin film can vary through its thickness resulting in an internal moment per unit width, M_i. If such a diaphragm or film is released it will curl with a radius given by R in equation (3.9) [17].

$$R = \frac{Et^3}{12M_i} \qquad (3.9)$$

Equation (3.9) indicates that the release curl will not only depend inversely on the internal moment but is also dependent on Young's modulus and highly dependent on the film thickness.

Where a diaphragm is of a square design joined to the substrate along all four sides, it will buckle due to internal strain if the diaphragm side length exceeds a critical value of a_{cr} given by equation (3.10) [17].

$$a_{cr} = \frac{2\pi t}{\left[9(1+\upsilon)\varepsilon_i\right]} \qquad (3.10)$$

Hence the critical side length to avoid buckling is dependent on the material properties and the film thickness. In the case of the SIMOX pressure sensor the diaphragm is formed from a single crystal layer which originated as part of the substrate. It would therefore be expected to have a low internal stress. There may be some level of internal stress resulting from the oxygen implantation process; however, annealing is used in SIMOX manufacture to relieve this [18]. Therefore the critical size to which a SIMOX diaphragm can be made without the occurrence of buckling is expected to be large compared with diaphragms made from many alternative materials.

Within the region of elastic behaviour, the external stress in a diaphragm can be calculated using mechanical plate theory [19]. For a circular plate, the degree of deformation determines the size and location of the maximum stress. When a circular diaphragm undergoes large deflection, the stress is at a maximum in the centre and is described by equation (3.11) [19].

$$\sigma_{max} = 0.423\sqrt[3]{\frac{EP^2r^2}{t^2}} \qquad (3.11)$$

The circular SIMOX pressure sensor diaphragm, however, displays a small deflection; in this case the stress will be at a maximum at the edge and is described by equation (3.12) [19].

$$\sigma_{max} = 0.75\frac{\mathrm{Pr}^2}{t^2} \qquad (3.12)$$

Equation (3.12) shows a dependence of the maximum stress not only on the applied pressure but the ratio of dimensions; radius squared to thickness squared. For a large deflection of the diaphragm described by equation (3.11), there is also a dependence

on the Young's modulus, but the dependence on all variables is to the power of one third, reducing their influence (compared with the case of small deflections). Substitution of the dimensional parameters of the SIMOX pressure sensor diaphragm into equation (3.12) allows us to calculate the maximum stress. Under application of the maximum pressure of 66.66 kPa, the maximum stress at the edges of the diaphragm has been calculated as ~ 90 MPa. This is well below the yield or fracture stress of monocrystalline silicon which is ~ 0.6 Gpa, and indicates that in routine operation the stress in the diaphragm will not be sufficient to cause the silicon to fracture.

For a deflected square diaphragm, the maximum stress is at the mid-point of the four sides and is described by equation (3.13) [2].

$$\sigma_{max} = \left(\frac{5}{16}\right)P\frac{a^2}{t^2} \qquad (3.13)$$

For a square plate with the SIMOX determined vertical dimensions and a 17 x 17 μm area, the maximum stress under a maximum applied pressure of 66.66 kPa, can be calculated as ~150 MPa. It can be seen that this is substantially higher than the maximum stress of 90 MPa calculated above, which a comparable circular diaphragm would be subjected to under application of the same pressure.

If the fracture stress of silicon is used in equation (3.12) together with a pressure of 66.66 kPa, we can calculate a radius r. This will be the minimum radius which will result in diaphragm fracture under maximum applied pressure. At any radius less than this value the diaphragm would remain operational up to and including the maximum applied pressure. This maximum radius has been calculated from equation (3.12) as approximately 22 μm. Since the diaphragm radius used here was 8.5 μm (diameter = 17 μm), this demonstrates that there is sufficient latitude in the design to allow adjustments to lateral diaphragm dimensions to extend the basic design to alternative applications without risking the operational integrity of the device.

Diaphragm strain can be reduced by thermal annealing and diaphragm design. For devices to display low stress their diaphragm area should be minimized [19].

Supporting beams can also be designed to reduce diaphragm stress by allowing lateral motion as shown in figure 3.4 [15].

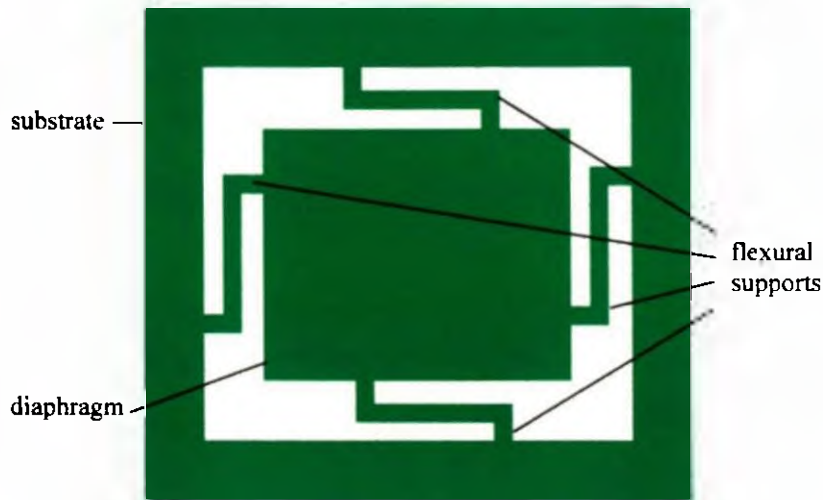

Figure 3.4 Diaphragm with flexural supports for stress relief

In this arrangement, the fraction of strain released by the use of flexural supports, α is given by equation (3.14) [15]

$$\alpha = 1 - \frac{Fn^2}{\varepsilon a E t} \qquad (3.14)$$

where

F = applied force

n = number of supports

εa = unreleased strain

Since the above calculations have shown that the SIMOX sensor will not suffer from a level of stress likely to cause fracture, it was not considered necessary to use flexural diaphragm supports.

The method of diaphragm support is another factor which affects the performance of a diaphragm. For clamped edge diaphragms, such as the modelled SIMOX design, the deflection is one quarter that of a diaphragm with hinged edges but the maximum stress at the diaphragm edge is 0.6 the value for a hinged diaphragm [20]. This means

that the SIMOX pressure sensor will display a lower change in capacitance for unit pressure compared with a hinged diaphragm but will withstand higher pressures before device failure.

3.3.4 IMPULSE RESPONSE

The transient response of capacitive pressure sensors under impulse pressures has been studied by other researchers [10]. Underdamped square diaphragms were modelled and the results have suggested that the capacitive response is primarily determined by the fundamental mode of vibration. Modes 00, 01 and 02 of a typical square diaphragm are shown in figure 3.5.

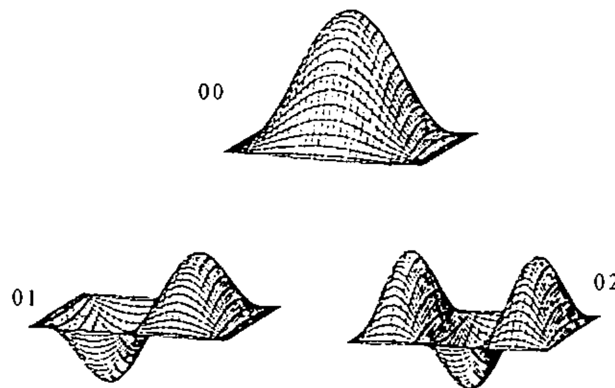

Figure 3.5 Modes of vibration of a diaphragm

The 01 (and all odd modes) display an anti-symmetry which means the positive and negative deflected regions cancel and the net contribution to the response is zero. The 02 (and all even modes) have positive and negative deflection areas which partially compensate each other to result in only a small contribution to the response. Hence the 00 or fundamental mode in which deflection is in one direction only forms the major contribution to the sensor response. Similar behaviour would be expected for a circular diaphragm such as the design fabricated in the current study.

The time t_{ss} for the response of a diaphragm to settle to ± x % of the steady-state is given by equation (3.15) [10].

$$\frac{\left[\cos(\Omega_d t_{ss} - \vartheta)\right]\exp(-\beta t_{ss})}{\cos\vartheta} = \pm\frac{x}{100} \qquad (3.15)$$

where

Ω_d = damped angular frequency of vibration

β = damping factor

$\sin\vartheta = \frac{\beta}{\Omega_{00}}$

Ω_{00} = fundamental angular frequency of vibration

Low settling and overshoot times are desirable for diaphragms in sensing applications. Simulations have shown that, by comparison with many other materials, silicon exhibits the best results in terms of highest pressure sensitivity, with smallest settling times and overshoot values.

3.3.5 TRAPPED AIR EFFECTS

For the sensor described in this work, the cavity is sealed by a spin deposited photoresist film following one sided etching. In this case the cavity will remain filled with air which exerts an internal force on the diaphragm. This opposes the applied pressure and hence changes the diaphragm deflection for a given applied pressure. At a constant temperature and no applied pressure, the pressure loading across the diaphragm, Q, due to trapped air is given by equation (3.16) [21].

$$Q = P_{atm} - \frac{P_1 V_1}{V_1 - \Delta V} \qquad (3.16)$$

where

P_{atm} = atmospheric pressure
P_1 = unknown internal cavity pressure
V_1 = internal cavity volume
ΔV = change in internal cavity volume

The net pressure on the diaphragm will be the resultant of the internal and external pressures. If the internal pressure is lower than atmospheric then the diaphragm will deform downwards and the combination of atmospheric pressure and internal pressure will be additive. If the internal pressure is higher than atmospheric then the diaphragm will deform upwards and the combination will be subtractive. For a circular diaphragm, the diaphragm displacement due to internal gas is assumed to be small compared with the diaphragm radius and to have a spherical mode which has been confirmed by Huff *et. al.* [21] using interferometry. They have shown that the change in internal cavity volume is given by:

$$\Delta V = \frac{1}{6}\pi w\left(3r^2 + w^2\right) = \frac{\pi r^2 w}{2} \qquad (3.17)$$

Substituting equations (3.1) and (3.17) into equation (3.16) allows the unknown internal pressure to be expressed as:

$$P_1 = \frac{d - \left(\frac{w}{2}\right)}{d}\left(P_{atm} - \frac{5.3Et^3 w}{r^4\left(1 - \upsilon^2\right)}\right) \qquad (3.18)$$

Expression (3.18) can be used in cases where the deflection of the diaphragm due to trapped gas can be measured to allow the internal gas pressure to be calculated. In an examination of the internal gas pressure of a large cavity (diameter of 12 mm) by Huff [21], the diaphragm deformation was measured and an average residual gas pressure of 0.79 atm. was calculated. This is lower than atmospheric pressure indicating a reduced pressure within the cavity and downward deflection of the diaphragm. This reduced pressure was thought to be due to the oxygen in the trapped air in the cavity reacting with the sidewalls during a high temperature bonding operation. The diaphragm deformation was confirmed as being due to internal pressure, as opposed to

buckling under residual stress (common in bonded structures), by flattening of the diaphragm upon the drilling of small holes through it [19]. In the case of the SIMOX sensor, it would be expected that an internal pressure more similar to atmospheric pressure would be retained within the cavity since the structure is not exposed to high temperatures during manufacture.

The gas trapped within a cavity will expand and contract in response to changes in the ambient temperature. A change in air volume within the cavity may result in further pressure loading of the diaphragm and an adjustment to any diaphragm deformation. The differential pressure across the diaphragm, due to cavity volume expansion arising from heating effects is given in equation (3.19) [19].

$$Q = \frac{T_2 P_1 V_1}{T_1 (V_1 + \Delta V)} - P_{atm} \tag{3.19}$$

where T_1 is the initial temperature and T_2 is the final temperature of the cavity and all other parameters are as previously defined. By combining expressions (3.19) and (3.12), the stress which the diaphragm is subjected to as a result of internal gas expansion can be evaluated and compared with the yield stress for single crystal silicon to determine whether the temperature induced expansion will cause plastic behaviour or breakage of the diaphragm.

In Huff's work [19], plastic behaviour is reported as occurring in this situation at temperatures in the region of 800 - 850 °C. These temperatures are an order of magnitude higher than temperatures which the SIMOX sensor would be deliberately subjected to and therefore it is reasonable to assume that plastic deformation of the diaphragm due to internal gas expansion resulting from increased temperatures is not a concern for the SIMOX pressure sensor. It is interesting to note that the plastic deformation of diaphragms by deliberate exposure of the trapped air to high temperatures has been designed into the fabrication process of pressure switches [21]. As the deformed structure is cooled the pressure inside the cavity decreases and the shell redeforms due to the external pressure loading.

3.3.6 ELECTROSTATIC EFFECTS

When a voltage is applied across capacitor plates, such as in a pressure sensor structure, an associated electrostatic field is generated. This field can result in an electrostatic deflection in addition to the deflection due to applied pressure. The presence of an electrostatic force can result in systematic error in the measured pressure and ultimately device failure [2]. This becomes particularly important with increasing applied voltage and decreasing applied pressure. The pressure, P_E, resulting from the electrostatic field due to an applied voltage, V, is described by equation (3.20) [2].

$$P_E = \frac{\varepsilon_o V^2}{2(d-w)^2} \qquad (3.20)$$

where

ε_o = permittivity of free space

other parameters are as previously defined

Equation (3.20) clearly shows that an increase in applied voltage will result in an increase in the electrostatic pressure with an inverse dependence on the square of the diaphragm to substrate separation. There is no dependence on any other structure geometry. The pull in voltage is defined as the voltage which provides sufficient electrostatic force between the capacitor plates to cause diaphragm collapse. The pull in voltage for a square diaphragm can be described by equation (3.21) [7].

$$V_p = \frac{64}{7}\sqrt{\frac{Et^3 d^3}{5\left(1-\upsilon^2\right)a^4 \varepsilon_o}} \qquad (3.21)$$

This shows that the pull in voltage is dependent on the material properties and geometric parameters with the diaphragm side length having the greatest effect. The larger the diaphragm side, the smaller the pull in voltage is. For a diaphragm of side 17 μm, fabricated from SIMOX, the pull in voltage can be calculated from equation (3.21) as around 50 V. A similar value would be expected for a circular diaphragm, of radius 17 μm. This is in excess of the voltages which would be used in the capacitance measurements to be made on the SIMOX sensor (typically 10 V) indicating that no

electrostatic force related problems would be anticipated for the discussed device under standard operational conditions.

3.3.7 RESONANT BEHAVIOUR

Pressure sensors can alternatively be operated in a resonant mode, this is often used to increase the sensitivity of the device and also simplifies the provision of measurement circuitry, since frequency can easily and accurately be determined by digital means. The fundamental resonant mode, f_{00}, of a circular diaphragm is given by [22]:

$$f_{00} = \frac{2.56t}{\pi r^2}\left[\frac{E}{3\rho(1-\nu^2)}\right] \qquad (3.22)$$

where the symbols are as previously defined.

Clearly the diaphragm resonant frequency is dependent on material properties such as Young's modulus and density together with the diaphragm dimensions such as thickness and most fundamentally the diaphragm area. For a circular SIMOX diaphragm of diameter 17 μm a resonant frequency of approximately 12.3 MHz can be calculated using equation (3.22). A similar expression can be used for the case of a square diaphragm, differing in the value of the constants [23], this yields a value of ~10.3 MHz for a square diaphragm of sidelength 17 μm. These values are high for mechanical resonant structures which is primarily due to the small size of the SIMOX diaphragm. The performance of silicon resonant pressure sensors has been reviewed in some depth by Bryzek [24].

3.4 SUMMARY

This chapter has addressed the design aspects of the proposed, novel pressure sensor and the reasons for the choice of sensing method, materials and sensor structure have been outlined. A description of the operation of the sensor has been given and the basic relationships which are fundamental to pressure sensor operation have been discussed. Calculations have been made for the sensor in order to estimate the

optimum dimensions and assess the expected performance. From this a 'final' device design has been proposed and it has been concluded that this would yield a functional pressure sensor. This includes the provision of sufficient deflection to cause a measurable change in capacitance without exceeding a level of stress which would damage the device. A high overpressure tolerance without fracture is expected and the output linearity may be increased by taking advantage of substrate contact. Any temperature dependence resulting from expansion of air trapped in the cavity is likely to be minimal. In summary, the theoretical aspects considered here have confirmed the predicted high performance discussed in chapter 1.

Square diaphragms are the most commonly reported structures therefore the discussion has included a comparison of the behaviour of both circular and square diaphragms. This has indicated that the circular design has some benefits over the square structure such as decreased stress under applied pressure.

Having reviewed the available technology in chapter 2 and designed a sensor structure in chapter 3, the work carried out to develop a suitable fabrication process is described in chapter 4.

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CHAPTER 4: PROCEDURES USED FOR PRESSURE SENSOR FABRICATION

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4.0 INTRODUCTION

The design of a SIMOX pressure sensor has been developed in chapter 3. This chapter discusses the actual device fabrication and reports on optimisation of the processes involved. The development of novel processes, alongside adaptations of traditional methods which were reviewed in chapter 2, was necessary to fabricate the SIMOX pressure sensor. These techniques are not available in the literature. The chapter describes the processes used for each fabrication step, giving the motivation for that choice and an indication of the success of its implementation. Where experimental surveys were conducted to determine appropriate fabrication methods, an outline of procedures and results are provided. Particular emphasis is given to novel but IC-compatible procedures, specific to SOI based processing. These include the development of an effective anti-stiction rinse cycle, highly controlled underetching of the sacrificial oxide, cavity sealing, specialised post-production metallisation and small sample alignment methods. None of these are standard techniques commonly described in published sources.

The processes are detailed in the order in which they are implemented in the pressure sensor fabrication sequence. The first process step described is photolithography

followed by silicon etching and then silicon dioxide etching. The latter two sections include an outline of surveys conducted to determine optimum etch systems. Details of post etch rinses are then provided, followed by an overview of the metallisation techniques used along with an outline of the experimental study. This was carried out to establish a means of combining metallisation with the lengthy silicon dioxide etch step necessary. The procedures used for sealing etch windows to form a closed cavity are then discussed.

4.1 PROCESS OUTLINE

The process sequence for pressure sensor fabrication from SIMOX was evolved through experimental analysis of each step of the device formation with considerations at each stage for compatibility of the previous and subsequent steps. In order to fabricate the final design of the pressure sensor, which consists of a matrix of interconnected pressure-sensitive diaphragms, and other microstructures from SIMOX material, the process sequence listed below was used. The highlighted steps are those which use novel techniques, the sequence is also shown in the diagram in figure 4.1 (overleaf).

(i) Cleaning of SIMOX starting material.

(ii) Photolithography for silicon window definition.

(iii) Anisotropic etching of windows in top silicon layer, selective to stop at silicon/silicon dioxide interface.

(iv) Removal of image forming photoresist.

(v) Silicon dioxide isotropic etching, selective over silicon, to form cavity under the silicon overlayer with the top silicon acting as a mask. Time control is used to produce the required diaphragm diameter.

(vi) Anti-stiction rinse sequence.

(vii) Aluminium deposition.

(viii) Aluminium photolithography.

(ix) Aluminium etching and sintering.

(x) Removal of image forming photoresist.

(xi) Photolithographic plugging of etch windows.

(xii) Packaging.

(i) Cleaned SIMOX substrate

(ii) Photolithography for silicon

(iii) Silicon

(iv) Photoresist

v) Silicon dioxide undercut

vi) Anti-stiction rinses

(vii) Aluminium

(viii) Photolithography for aluminium

(ix) Aluminium etching

(x) Photoresist removal

(xi) Cavity Sealing

(xii) Packaging

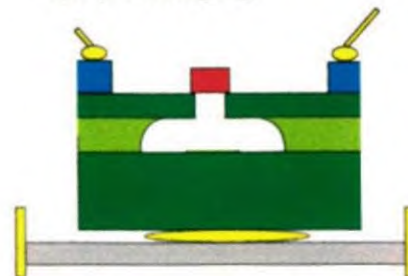

Figure 4.1 The pressure sensor fabrication process sequence

4.2 PHOTOLITHOGRAPHY

4.2.1 PHOTOLITHOGRAPHY PROCEDURES

Prior to processing, all SIMOX and standard silicon samples were cleaned for 15 minutes in a solution of approximately one volume part hydrogen peroxide and 3 volume parts sulphuric acid, rinsed in a de-ionised water (DI) weir and then dipped in a 5 % HF aqueous solution to remove any native oxide. In addition, if considered necessary, the samples were degreased in an acetone, isopropyl alcohol and de-ionised water rinse sequence.

Photolithography was then carried out for silicon etching to define the circular windows. This began with a one hour oven dehydration bake at 150 °C, followed by vapour priming to promote photoresist adhesion in electronic grade hexamethyldisilazane (HMDS) for 20 minutes. Shipley 1813 positive photoresist was then applied, dispensed from a pipette to cover approximately two thirds of the area of the sample being held on a vacuum chuck of a manual spinner. The sample was then accelerated to a constant spin speed of 5000 rpm for 40 seconds to give a uniform resist coating. A soft bake at 105 °C was carried out for 1 minute on a vacuum hotplate to expel solvents from the resist coat. The resist thickness after softbake was measured as 1.2 μm on the Tencor alpha step. UV exposure of the photoresist was achieved with a Cobilt contact aligner using the appropriate mask plate. For bulk silicon samples an exposure time of 17 seconds was used. For SIMOX samples an 18 second exposure time was found to be appropriate and for aluminium covered samples a 16 second exposure time was used.

Development was carried out in 150 ml of positive developer with 100 ml of water, using agitation of the sample within a developer bath for a time of between one and two minutes. The end point was determined by microscope observation of the features following rinsing in DI and drying in a nitrogen stream. Where dry etching techniques were to follow a 120 °C, 20 minute hotplate hard bake was carried out. Subsequent to etching, the patterned resist was removed either by soaking in acetone or barrel etching in an oxygen plasma. Alternatively, in some cases, (see section 4.7.3), Shipley photoresist, PREDA-914-EZ was used. For this the process modifications were a 15 minute HMDS vapour prime and a 1 minute hotplate soft bake at 125 °C. The post

softbake resist thickness was measured on the alpha-step as 1.31 μm. The exposure remained at 18 seconds and immersion development in Microposit 351 developer took approximately 1.5 minutes for full development.

A negative Shipley photoresist was also used for metallisation trials (see section 4.7.3). Wafer conditioning for this was at 200 °C for 1 hour. Adhesion promoter was spun on to the wafer followed by the photoresist. A spin speed of 5000 rpm was used for the photoresist to obtain a coat thickness of approximately 0.6 μm, measured on the alpha step. Soft baking was carried out at 80 °C for 10 minutes. The development procedure was 50 seconds in Selectiplast N2 followed by 15 seconds in MOS Selectipure n-butyl acetate. Hard baking was carried out at 170 °C for 30 minutes.

4.2.2 MASK DESIGN

Three different mask sets were used in this project. The designs for these were drawn using Autocad software. Two emulsion masks allowed feasibility assessment and a third chrome type facilitated final device manufacture. The transformation from design into an emulsion mask was carried out in-house using a flat-bed plotter, photoreduction and step and repeat printing. The chrome sensor array mask was manufactured elsewhere by electron beam direct writing.

4.2.2.1 MASK FOR UNDERETCHING SURVEY.

In order to survey various silicon dioxide etchants, an emulsion mask containing opaque squares of two different side lengths was used. This allowed assessment of the degree of underetch and modification to feature geometry during etching.

4.2.2.2 MASK FOR THE FABRICATION OF SINGLE SENSING STRUCTURES

An emulsion mask set was prepared comprising a separate mask for each of the material layers used for pressure sensor fabrication:

(i) Silicon access window opening.

(ii) Metal contact definition.

The mask set incorporated a number of examples of isolated single pressure sensor structures of different dimensions. These were intended to establish experimentally the feasibility of the fabrication techniques. Test structures were included to demonstrate the etching characteristics, such as the effect of reducing the window size and the minimum window size limit for successful underetching. Multi-window diaphragm, bridge and cantilever structures were also included.

4.2.2.3 MASK FOR THE FABRICATION OF AN INTERCONNECTED ARRAY OF PRESSURE SENSORS.

A chrome mask set was designed to define matrices of 2500 electrically interconnected diaphragms. Each matrix incorporated sensors with either 3 μm or 5 μm diameter access windows. A positive and negative mask, identical in design were prepared. The negative of the access window mask was used to define the plugs for the cavity sealing process step. By having two window sizes, the opportunity to use plugs slightly larger than the windows was available if necessary. Several isolated structures with individual contact pads were also included. These masks had different designs on each quarter. The small size of the structures meant that approximately 15 matrices could still be incorporated within just one quarter of the mask. Three of these quarters were patterned to define the material layers of the structure. This was feasible since the substrates used were never larger than one quarter full size. The fourth quarter contained designs for the silicon etching of some alternative structures such as resonators [1], released rings, bridges [2], cantilevers, and emitter tips to be fabricated as a demonstration of the applicability of the novel technology to wider fields of microengineering, sensing and actuating.

4.2.3 METHOD FOR EXPOSURE OF SMALL SAMPLES

The mask aligner used for exposure is designed to hold 3 inch diameter wafers by vacuum. However, the SOI experiments were conducted on small pieces of SIMOX,

typically 1 x 0.5 cm to 2 x 1.5 cm, (originating from 4 inch wafers). These were held in place by double-sided sticky plastic tape (as used for wafer sawing). Although the first mask exposure appeared adequate using this technique, on subsequent masks misalignment became apparent. These effects were considered to be due to the small sample size causing warping of the mask plate (figure 4.2).

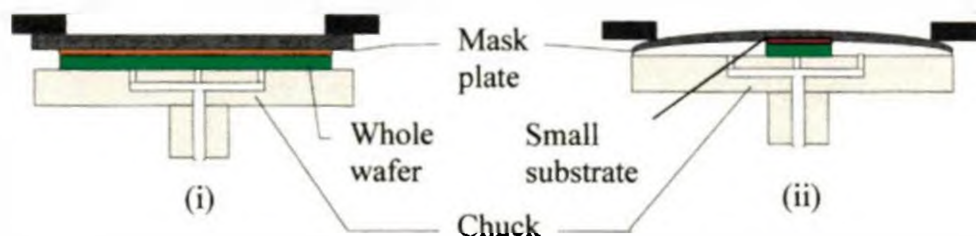

Figure 4.2 Small samples in mask alignment

To address this problem, a four inch silicon wafer of similar thickness to the SIMOX (0.54 mm) was sawed into pieces and placed around the sample as shown in figure 4.3. For ease of use, the assembly was fixed on to a standard 3 inch silicon wafer. For exposure the sample was simply waxed into position with a lower temperature wax than used for the surrounding standard silicon pieces. The sample was then aligned, exposed, removed by heating and developed individually while the wafer and waxed 4 inch pieces were stored for future use. The wax was then removed from the back of the SIMOX sample by heating. This proved successful and full alignment was achieved routinely.

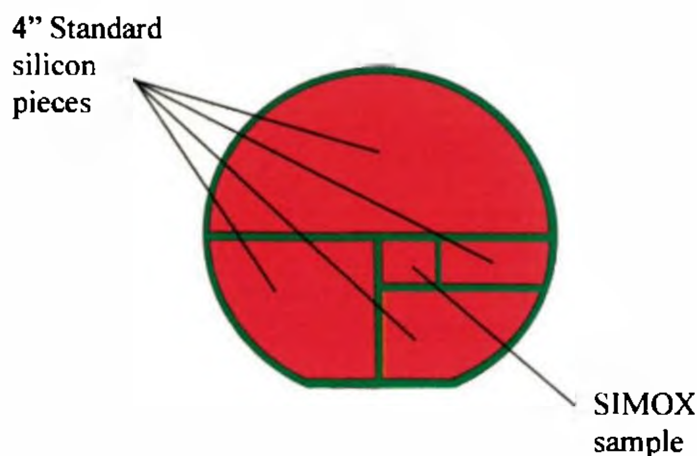

Figure 4.3 Mounting of a SIMOX sample for alignment and exposure.

4.3 SILICON ETCHING

This etching transfers the arrays of holes in the photoresist mask defined in the previous step, to holes in the silicon with corresponding dimensions. For the fabrication of pressure sensitive diaphragms, circular windows, 3 or 5 μm in diameter were required to be etched in the top silicon layer of the SOI material in order to expose the buried silicon dioxide. This step requires etching of the monocrystalline silicon with high selectivity with respect to the photoresist mask.

Appropriate etching could be achieved by wet or dry techniques and each method was experimentally tested with suitable etch compositions. This allowed comparison of the two techniques to determine the optimum system for microstructure fabrication from SIMOX with regard to structure profile, repeatability, linearity, process control and mask capabilities. These investigations initially used standard silicon wafers prior to testing on more expensive SIMOX wafers. This allowed a further comparison of data for the two materials, and the determination of the etch rates for SIMOX top silicon, which are not commonly reported and differ slightly from those of bulk silicon. Following silicon etching, rinsing in de-ionised water and drying in nitrogen, the image forming photoresist was removed. The etched steps were measured using a Tencor Alpha-step 200 surface profiler, with the mean of several readings from across the sample being used for rate determination.

4.3.1 WET SILICON ETCH SURVEY

A series of experiments was conducted using two wet silicon etchants, one based on KOH and the other on $KMnO_4$. The likely benefits of these, over dry methods include high selectivity (i.e. ability to etch the substrate compared to the mask) and high etch uniformity [3]. The experiments were carried out using a hotplate for temperature control. The results from each solution were compared to determine the most appropriate wet etchant for use.

Although HF based silicon etchants are more commonly used, they are largely isotropic and a high degree of control cannot be achieved [4]. Hydrazine and ethylene diamine provide anisotropic etching above a threshold temperature of approximately

40 °C which is indicated by the formation of small bubbles on the silicon surface as a result of hydrogen gas expulsion. The etching mechanism is by the formation of hydrous silica and its subsequent dissolution by the formation of a complex [5]. However, these solutions require high temperatures and hydrazine is very sensitive to residual water in the system. In addition, both are hazardous to the operator [6]. These etchants display high sensitivity to doping which can be used as an etch stop mechanism [7].

4.3.1.1 POTASSIUM HYDROXIDE SOLUTION (KOH)

KOH, used either with water or in a number of other compositions e.g. with IPA [5], produces a crystallographic-dependent etchant displaying high rates of attack on (100) planes which can be 600 times faster than on (111) planes [8].

In the subsequent section (100) silicon etching, in KOH with water is reported and compared to similar reports. A potassium hydroxide (KOH) solution, with a composition of 66 g KOH in 100 cm^3 of water, was tested for the required silicon etching, as the etch rate is appropriate for the removal of small depths and the high temperature sensitivity allows additional fine tuning of the rate. Furthermore, SIMOX silicon etching has been reported using KOH [9, 10], with a selectivity over the buried silicon dioxide of nearly 200:1 [11] which would allow a precise etch stop mechanism. A highly linear etch rate was expected at constant temperature as commonly reported in literature [12]. A photoresist mask could be used for etching [5]. In order to establish a suitable system for device etching, silicon samples were etched in the KOH solution at 7 different temperatures. A graph of etch rate in microns per minute versus the reciprocal temperature in °C is shown in figure 4.4. This plot takes the form of an Arrhenius relationship as has been described by Seidel [13]. The scatter of points is quite high, which is most likely to be due to poor temperature control of the hotplate arrangement used, thought to be in the region of ±3 °C, possibly combined with poor solution mixing. The gradient of this plot (which represents the rate of change of the log of the etch rate with temperature) is 0.95 for the 39.8 wt% solution tested. This compares with 2.06 in the work of Seidel [13] using a 42 wt% aqueous KOH solution this implies that the higher concentration solution displays a higher temperature dependence.

A temperature of 50 °C combined with slight agitation was selected as the most appropriate condition for pressure sensor fabrication since it resulted in a moderate etch rate. With this system, an etch rate of 0.47 μmmin^{-1} or 28.2 μmhour^{-1} was observed for standard silicon. This compares well with published rates of 21 μmhour^{-1} for a 45 wt% solution at 70 °C [14]. The conditions most similar to our etchant system are achieved by Siedel, etching in 42 wt% solution at a temperature of 50 °C and in this case the etch rate is considerably lower at 9 μmhour^{-1} [13]. However, 50 °C etching carried out with a lower concentration (20 wt%) is recorded as etching at a higher rate of 12 μmmin^{-1} [15]. This author also reports [15] raised temperature etching at 72 °C in 39 wt% solution resulting in an etch rate of 43 μmhour^{-1} [15]. In this case the rate is considerably higher than in Kung's high temperature work [16]. No reason is given in Seidel's papers [13, 15] for the inconsistencies within his and between his and other published work. However, direct comparisons are made difficult by the non-identical parameter sets of each piece of research. The sensitivity of this etch system to changes in % KOH is estimated in Seidel's work as approximately 10 μmhour^{-1} difference in etch rate for 10 wt% KOH concentration change (within the range 30 < wt% KOH < 60). Furthermore, figure 4.4 clearly demonstrates the importance of temperature on this etchant system.

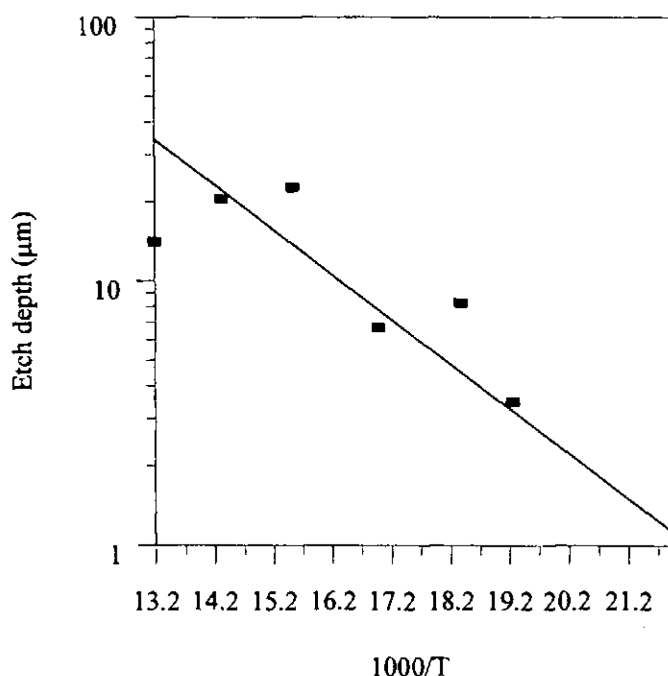

Figure 4.4 Etch Depth as a Function of Temperature for aqueous KOH Etching of Silicon.

Seidel also describes a reduction in etch rate for a particular system with the addition of propanol. This is supported by a comparison of the high temperature work carried out by other researchers. Etching carried out in a 20 wt% aqueous solution at 80 °C etched silicon at a rate of 86 $\mu mhour^{-1}$, whereas Bean's key work describes the same system but with the addition of n-propanol, giving a rate of 60 $\mu mhour^{-1}$ [5].

4.3.1.2 POTASSIUM PERMANGANATE SOLUTION ($KMNO_4$).

Alternative wet silicon etchants are based on oxidising agents such as Br_2, I_2 and potassium permanganate ($KMnO_4$) [7, 17]. A potassium permanganate solution with a composition of 0.6 g $KMnO_4$, 280 ml H_2O and 20 ml (48 wt%) HF was tested for silicon etching. The rapid but linear etch rate allowed high throughput and selectivity over both silicon dioxide and positive photoresist. This made it appropriate for use in the silicon etch step of the SIMOX sensor fabrication. Etching was carried out at 25.5 °C (±0.5 °C) with slight agitation. Based on an expected etch rate of 0.32 $\mu mmin^{-1}$ [18], a range of etch times around that required to remove 0.2 μm, i.e. the SIMOX top silicon layer thickness, was tested on standard silicon. Having obtained repeatable, well-controlled etching at a rate of 0.34 $\mu mmin^{-1}$ with standard silicon, SIMOX etching was then carried out. The graph in figure 4.5 displays the results. Etch depth in microns is plotted versus etch time in seconds for standard silicon and SIMOX material. A linear relationship between etch depth and time was obtained in agreement with other work conducted in this field [17]. The degree of scatter is low indicating high repeatability and process control. From the gradients, an etch rate of 0.40 $\mu mmin^{-1}$ was determined for SIMOX silicon etching. The silicon etch rate was found to increase dramatically to 0.86 $\mu mmin^{-1}$ for moderately boron doped bulk silicon (2.06E17 cm^{-3}). At 20 - 25 °C this etchant system has been described as etching p-type material slower than n-type [17]. The selectivity of this etch over silicon dioxide is not expected to be high due to the inclusion of hydrofluoric acid in the composition but was not measured since an etch stop was not required in this case where time controlled etching was being used. Any slight over etch would not be a major concern as the next process step is a silicon dioxide etch using the same mask features.

The standard silicon rate correlates roughly with the etch rate values reported by Nahm [17], when the higher etch temperature and lower $KMnO_4$ concentration of our

composition are taken into account. With a solution of 12M HF, 0.05M $KMnO_4$, H_2O etching conducted at 20 °C was reported to proceed at a rate of approximately 1.75 $\mu mmin^{-1}$ on (100) silicon. A temperature increase of 5.5 °C is described as increasing the etch rate of silicon in this etchant composition by as much as 0.6 $\mu mmin^{-1}$. There is also strong, but non-linear, dependence on the concentrations of both $KMnO_4$ and HF. Much higher rates have been determined, with the optimum composition with regard to the resultant surface quality, reported as 3.5 g $KMnO_4$, 100 ml aqueous HF solution, 10 ml H_2O. This etched at a rate of 4.4 $\mu mmin^{-1}$, producing highly polished surfaces [16], but is a much more concentrated solution than that used in our work. 7 g $KMnO_4$ with aqueous HF solution but no additional water was reported to display inconsistent etching with limited solution stability. A lower rate of 0.4 $\mu mmin^{-1}$, resulting from a solution of 2 parts HF : 1 part of 0.038 M $KMnO_4$ by volume is also detailed. This corresponds more closely to our solution composition excepting the absence of water.

4.3.2 DRY SILICON ETCHING SURVEY.

Dry etching has the potential to achieve better anisotropic etching than wet techniques and for production purposes can be more easily automated [3]. Reactive ion etching (RIE) in particular is a high precision anisotropic technique which gives minimal loss of critical dimensions. For these reasons, reactive ion etching was investigated for the silicon etch step of the SIMOX sensor production. A literature survey was carried out to determine the appropriate gases and process parameters, followed by experiments to characterise and optimise the chosen system. For RIE, the specific combination of parameters is of great importance in the control of material etch rates and selectivity [7]. For example, both silicon and silicon dioxide can be etched in CHF_3, but, by adjusting chamber conditions each can be removed selectively over the other. A positive photoresist (Shipley S - 1813) mask was used and although a high silicon/photoresist selectivity was achieved, the mask etch rate can never be zero due to the finite removal rate by physical sputtering. However, selectivities as high as 80 : 1 and 75 : 1 have been reported for silicon etching with both silicon dioxide [8] and photoresist masks [19] respectively.

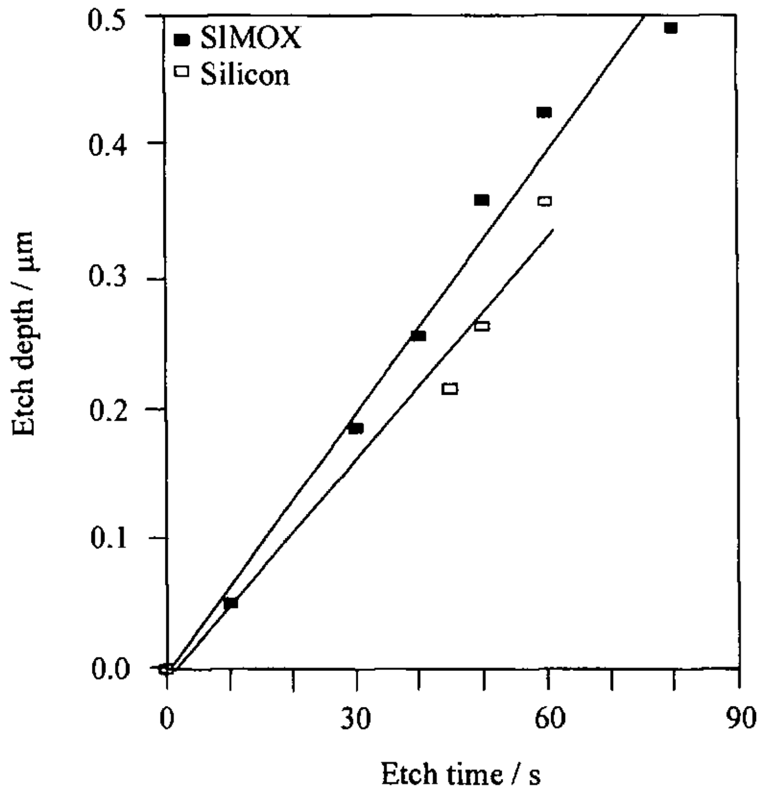

Figure 4.5 Etch rate calibration graph for $KMnO_4$ etchant.

4.3.2.1 TRIFLUOROMETHANE (CHF_3).

CHF_3 etches silicon by the production of highly volatile SiF_4 [7]. Anisotropic, selective etching can be achieved at low pressure where the gas forms positive ions in the electric field [4]. Although selectivity can be adjusted by the addition of oxygen, this was not possible with the Electrotech Plasmafab 340 reactive ion etcher being used. Etching was reported using the parameters below with resultant etch rates of 1130 Åmin^{-1} for silicon and 3 Åmin^{-1} for silicon dioxide, giving a silicon/silicon dioxide selectivity of 300:1 [20], using standard silicon, not SIMOX.

- Gas composition: 60 % CHF_3 10 % Ar
- Power: 50 W
- Base Pressure: 30 mT
- Chamber Pressure: 56 mT

Several combinations of these parameters were tested experimentally on standard silicon using the reactive ion etcher as detailed below in table 4.1:

Experiment number	Gas composition		Forward Power (W)	Etch Time (mins.)
	% CHF_3	% Ar		
(i)	20	-	107	30
(ii)	40	-	75	30
(iii)	40	-	50	30
(iv)	60	5	50	45
(v)	60	10	50	45
(vi)	60	10	75	45

Table 4.1 Reactive ion etch systems tested for bulk silicon etching

The results were examined using optical and scanning electron microscopy. From this, the system given in (v) was selected as the optimum system, producing features with smooth surfaces and well defined edges. Etching with (i) resulted in rough surfaces and uneven edges, while (ii) and (iv) gave moderately improved edge profiles compared with (i) but uneven surfaces. (iii) led to features with smooth surfaces but poor edge definition. The results of (iv) were similar to (iii) but the edges were slightly better defined.

Etch rate analysis for system (v) was initially conducted on small samples (~1.5 cm^2) of standard silicon. This gave a rate of 3.16 $nmmin^{-1}$. Etching was then repeated with quarter wafers of standard silicon and the rate was reduced to 2.05 $nmmin^{-1}$. The etch depth versus time for both sample types is plotted in figure 4.6. These results gave an estimate of the change in etch rate with sample surface area due to the loading effect (see section 2.3.2.4) to allow SIMOX characterisation to be carried out on small samples. It was expected that the etch rate for the top silicon layer in SOI would be different from that for bulk silicon [21]. The SIMOX silicon etch rate on small samples (~1.5 cm^2) was measured as 4.58 $nmmin^{-1}$, (the gradient of the etch depth/time plot, in figure 4.6). The silicon loading effect shown by the two plots in figure 4.6 was then applied to this SOI rate using the ratio of gradients to estimate an

etch rate of 2.98 $nm min^{-1}$ for silicon etching of 1/4 wafer size SIMOX samples for sensor fabrication. This procedure can be justified from consideration of the equation which describes the loading effect [7]:

$$R = \frac{G}{n} \left\{ \frac{\tau k}{1 + \left(\frac{\tau k A}{V} \right)} \right\} \qquad (4.1)$$

where

G = Generation rate per unit volume and time.

R = Etch rate.

n = Number of atoms per unit volume of layer being etched.

τ = Recombination rate.

k = Reaction rate constant.

A = Surface area to be etched.

V = Volume of plasma.

For both the bulk silicon samples, every value in the equation will be the same with the exception of the area. Therefore the ratio of etch rates will reflect only the difference in exposed area. When SIMOX silicon is etched, again the only difference between the two samples is the area, which differs in the same ratio as the two silicon samples. Although the value of K for example may be different in this case to that of bulk silicon, it will be the same for each SIMOX sample meaning that the same ratio of etch rates can be assumed for 1.5 cm^2 and quarter wafer sample sizes.

4.3.2.2 SULPHUR HEXAFLUORIDE (SF_6).

SF_6 is an inorganic halide which can be used for reactive ion etching of silicon or silicon dioxide, producing passivating sulphur halides [7] to achieve anisotropy. By careful selection of the operating parameters used with this molecular gas, good control over selectivity and anisotropy can be achieved. SF_6 was tested on standard

silicon with the conditions below, reported for the etching of SIMOX silicon with selectivity over silicon dioxide and photoresist [21, 22].

- Gas composition: 10 % SF_6
- Power: 50 W
- Base Pressure: 33 mT
- Chamber Pressure: 43 mT

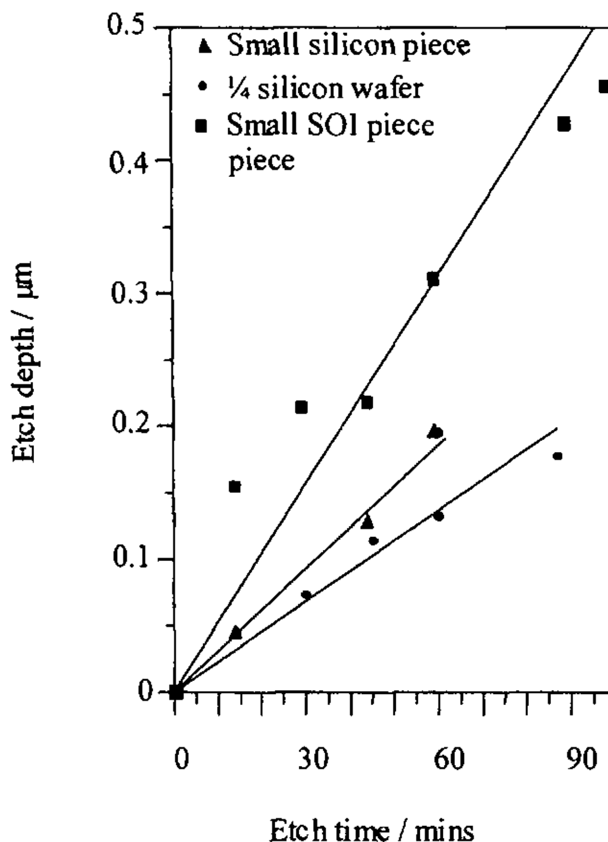

Figure 4.6 Experimental results indicating loading effect for CHF_3 etching.

Samples were etched for different times, corresponding to the predicted time to etch 0.2 μm. Following photoresist removal, feature height measurements were made across each sample using a Tencor Alphastep. From these, a mean feature height was determined which is plotted for each sample in figure 4.7. This gives an etch rate of 0.018 $\mu m min^{-1}$. Similar etch rate assessments were carried out on small SOI samples. These gave an etch rate of 0.005 $\mu m min^{-1}$, relating to an etch time of 40 minutes to

achieve complete etching through the top silicon layer. The main problem experienced with SF_6 etching was the slow etch rate and a lack of repeatability. Subsequent etching conducted using apparently identical conditions gave a completely different etch rate, this remained the case even after chamber cleaning. The reason for this is not fully understood but could be due to unstable chamber conditions induced by the use of SF_6.

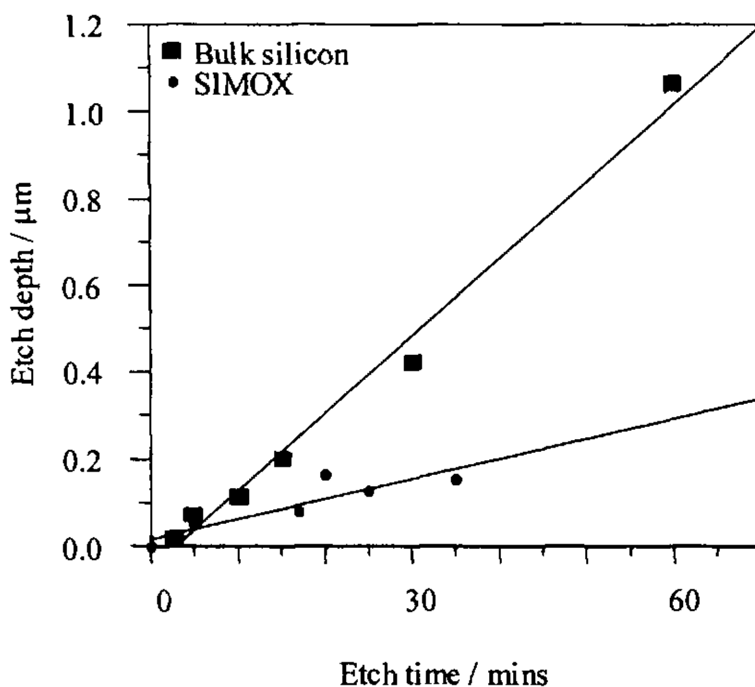

Figure 4.7 Etch rate analysis for SF_6 dry etching of silicon.

4.3.3 SUMMARY OF WET AND DRY ETCH SURVEYS

Dry etching using SF_6 resulted in problems with the run-to-run repeatability. Therefore, CHF_3 was considered the most appropriate dry etchant conventionally available. CHF_3, used in conjunction with the conditions described above, displayed linear, repeatable etching at a rate of 4.58 $nmmin^{-1}$ on small SIMOX samples. Potassium permanganate was selected as the most suitable wet etchant, primarily due to the ease of masking with photoresist, and the high linearity in the etch rate compared with KOH. On comparison of wet and dry etching methods, the wet etch, potassium permanganate was favoured for its faster etch rate (approximately 60 times faster than the CHF_3 system), allowing high throughput yet controlled etching.

Furthermore, surface damage can result from RIE making resist removal difficult. The $KMnO_4$ composition, described earlier in this chapter, combined with appropriate processing parameters, is well suited to the shallow depth of the top silicon layer. The experiments carried out demonstrated a high degree of linearity and repeatability allowing accurate determination of process etch times, to allow effective time control of the etching (figure 4.6). This system was therefore selected for use in pressure sensor fabrication.

4.4 SILICON DIOXIDE ETCHING

The areas of buried silicon dioxide exposed by the silicon etching are subsequently etched to leave the surrounding top silicon areas suspended as shown in figure 4.8. Vertical and lateral etching are required for this step to remove a section of the buried silicon dioxide layer below the top silicon, via the 3 or 5 μm etch window. To achieve this, a highly isotropic etchant was necessary which etches uniformly in all directions. This should also display a high selectivity over silicon to retain both the thin top silicon layer (which also acts as a mask), and the substrate surface. This would result in the formation of a cavity below a thin, flexible, suspended diaphragm which is free to deflect in response to an applied pressure.

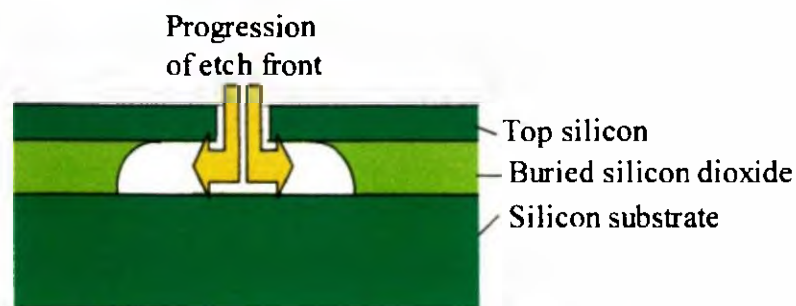

Figure 4.8 Illustration of Silicon dioxide underetching

4.4.1 WET SILICON DIOXIDE ETCHING

An extensive literature and experimental survey of wet silicon dioxide etching was conducted to establish an appropriate system for the cavity formation step. This allowed a comparison of parameters such as etch rates and undercut profiles. The amorphous nature of silicon dioxide films allows isotropic etching, facilitating undercutting to form a cavity. However, since silicon dioxide undercut is more often considered a nuisance than it is utilised, it is not well characterised in the literature [4]. The study conducted in this work used various compositions of buffered HF. This is the most commonly used isotropic silicon dioxide etchant [23, 24, 25] and has also been reported for the removal of buried oxide layers in SIMOX [26].

Four buffered, hydrogen fluoride based, silicon dioxide etchants of different compositions (listed below), reported as demonstrating isotropic behaviour, were tested experimentally. VLSI grade 48 % HF and VLSI grade 40 % NH_4F were used in all experiments. Low HF concentration compositions were selected to maximise the degree of process control achievable to allow time controlled etching in sensor fabrication. High selectivity is required to retain the top silicon layer intact during the undercut step of sensor fabrication.

- A: 10:1 2.18 M BHF

  10:1, 10 volume parts water, 1 volume part 2.18 M Buffered HF [27]
- B: BHF

  113 g 40 % NH_4F, 28 ml 48 % HF and 170 ml water [8]
- C: 10:1 BHF

  10 parts 40 % NH_4F, 1 part 48 % HF by volume [28]
- D: 7:1 BHF

  7 parts 40 % NH_4F, 1 part 48 % HF by volume [29]

Composition D is reported to produce no measurable polysilicon attack [29]. In initial etchant trials, no temperature control was used. For device fabrication the experimental set up presented in figure 4.9 was used. Several methods of agitation can be implemented. In this case, thermal convection was used as this is reported as producing greater lateral etching than other methods [4]. Here agitation is caused by

thermal gradients and chemical potential difference (resulting from the etching process) causing motion within the solution.

Initial characterisation of the four buffered hydrofluoric acid solutions was carried out using the mask detailed in 4.1.2.1. Negative photoresist was used, on a thermally oxidised bulk silicon wafer. The resist was intended to mimic the role of the top SIMOX silicon. The etch solutions, once mixed, were allowed to stand for approximately one hour prior to use, in order to reach equilibrium. The six etch times used to etch samples in each solution were based around the times necessary to laterally etch a distance of 4 μm based on published underetch rates. The measurements of undercut in all cases, suffer from large errors, due to the inaccuracy in the undercut measurement (±0.25 μm) using the cursors on the video screen of the microscope system used.

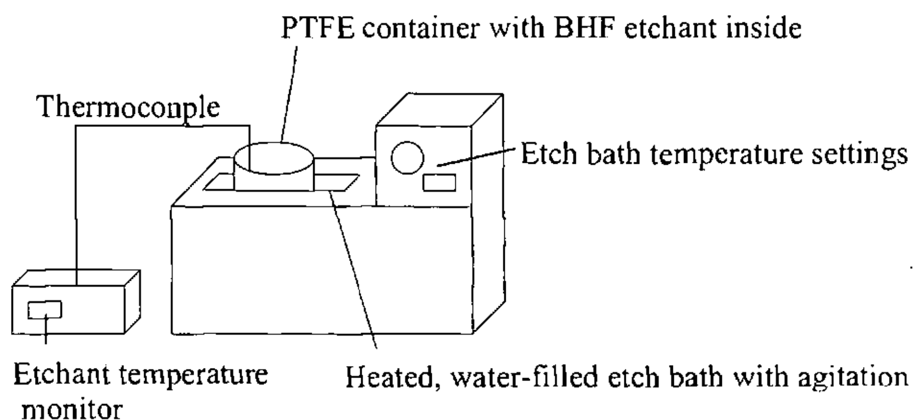

Figure 4.9 Experimental Arrangement.

4.4.1.1 LATERAL ETCHING OF BULK SILICON

Structures underetched in each of the four test etchants were observed with an optical microscope and the undercut measured using the calibrated cursors. The oxide boundary (etch front) was visible through the photoresist in these tests. Due to the thin nature of the top silicon layer in the SIMOX material - at 200 nm, the etch front was

also visible through this silicon in sensor fabrication. The mean of measurements made on ten diffcrent features was calculated and plotted with respect to time, for each etchant (see figures 4.10(i) to (iv)). The undercut distance was later confirmed by examination of the etched features following photoresist removal. Lincar fits have been made to allow etchant comparison, since each data set approximated a linear trace. However, in some cases an initial delay in etching is seen possibly due to downward etching occurring before thc sidewalls are exposed for the onset of lateral etching.

The gradient, which gives the underetch rate, effectively determines the degree of process control which is achievable. Etchant A gave a very fast rate of 1.54 μmmin^{-1} for lateral etching but high scatter suggested low repeatability, making time control inaccurate. Etchant B displayed a moderate etch rate of 0.5 μmmin^{-1} with moderate scatter indicating that precise etching could not be achieved with this composition. Etchant C displayed a slow etch rate of 0.28 μmmin^{-1}, with low scatter. Etchant D demonstrated a moderate etch rate of 0.97 μmmin^{-1} with low scatter indicating a high consistency of etching. The graph for etchant D suggests high etch controllability with a sufficiently fast rate to allow feasible etch times to be used for pressure sensor fabrication. Photographs of features etched in each solution are presented in figure 4.11. The coloured fringes indicate differences in oxide thickness, as a result of undercutting. The perimeter area of thc cavity has a profile consisting of many different oxide thickness, resulting in multicoloured fringes. Close fringes indicate a steep undercut profile.

Features etched in A showed only minimal undercut even at long etch times and lost shape definition with rounding of the corners occurring at longer etch times. Etchant B structures displayed uneven undercutting both over individual structures and across the wafer area. Etchant C had considerably distorted the square features into diamonds. Features produced with etchant D (Figure 4.11), however, displayed high undercut uniformity in individual structures and across the wafer indicated by well-defined, even fringes around each structure. No signs of distortion of the shape defined by the mask was detectable.

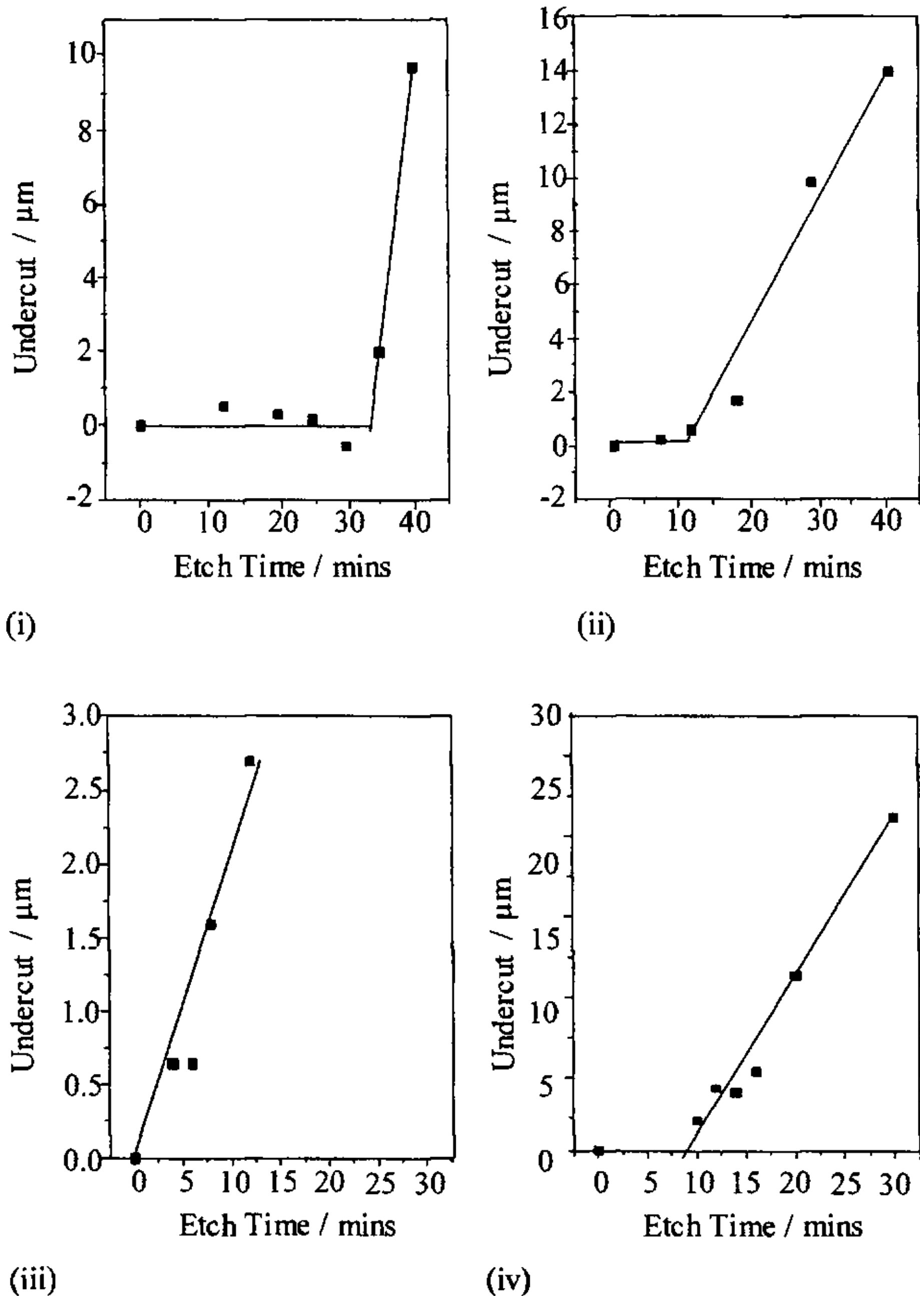

Figure 4.10 Lateral etch distance versus time for etchants A, B, C and D, figures (i), (ii), (iii), (iv) respectively

The microscope observation of the samples showed conclusively that, for the lateral silicon dioxide etching during pressure sensor fabrication, of the four compositions tested, solution D (7 : 1, 40 % NH_4F : 48 % HF by volume) would be the most appropriate for use.

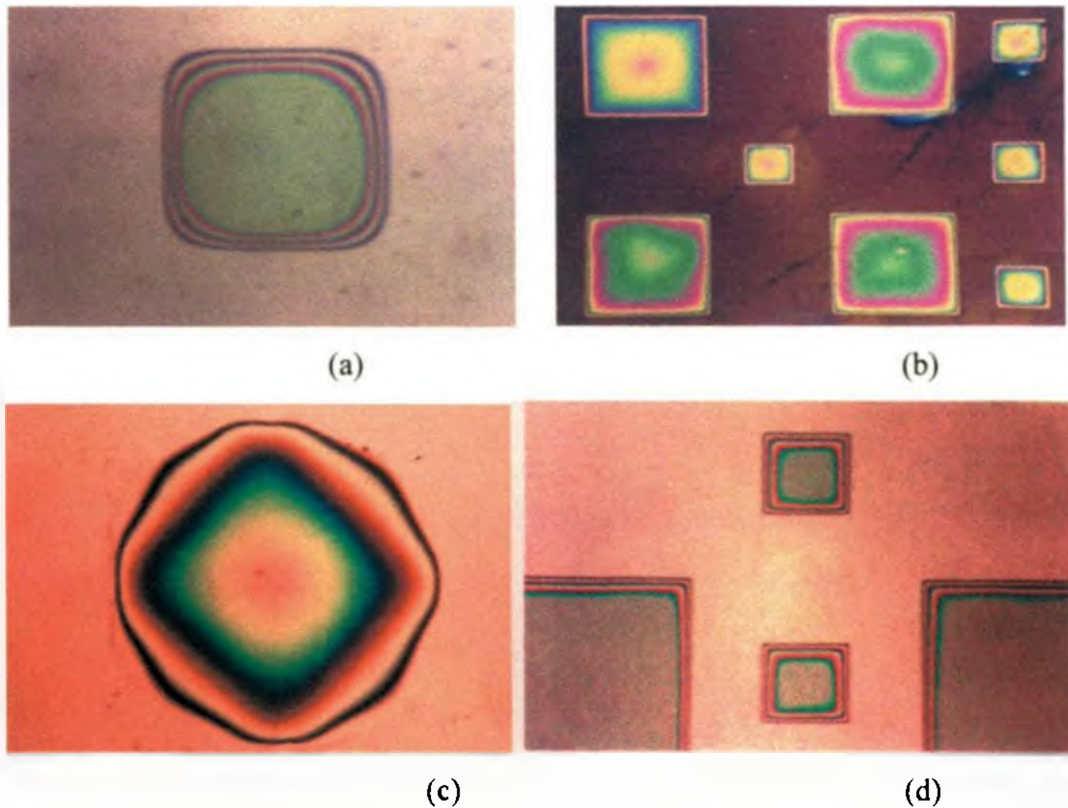

Figure 4.11 Optical Microscope Photographs Showing Results of Silicon Dioxide Etching with Etch Compositions: (a) A, (b) B, (c) C and (d) D.

Prior to SIMOX etching, undercutting experiments were then repeated using the selected etchant D, on thermally oxidised bulk silicon with a photoresist mask. Temperature control and a mask similar to that required for sensor etching (predominantly masked areas with small etch windows opened) were used. In this case a reduced etch rate (compared to that seen in initial experiments) of 0.16 $\mu mmin^{-1}$ was determined at 30±0.5 °C. This may be due either to increased temperature control or increased diffusion limitation effects (or a combination of these effects).

4.4.1.2 LATERAL ETCHING OF SIMOX

Further work was then undertaken to characterise and optimise the undercut step of structure fabrication using SIMOX with the chosen etchant composition. In this case, the top silicon layer acts as a mask and no photoresist is necessary. Again the etchant temperature was controlled to 30 ±0.5 °C and a mask with only small etch windows was used. From microscope measurements of the undercut, an initial linear interpretation of the lateral etching rate for the buffered hydrogen fluoride solution was established as approximately 0.13 $\mu mmin^{-1}$ for the buried oxide of SIMOX

material. A graph of undercut distance versus etch time is shown in figure 4.12. The minimal deviation of individual points from the best fit line confirms the expected high accuracy of this process seen in the initial trials.

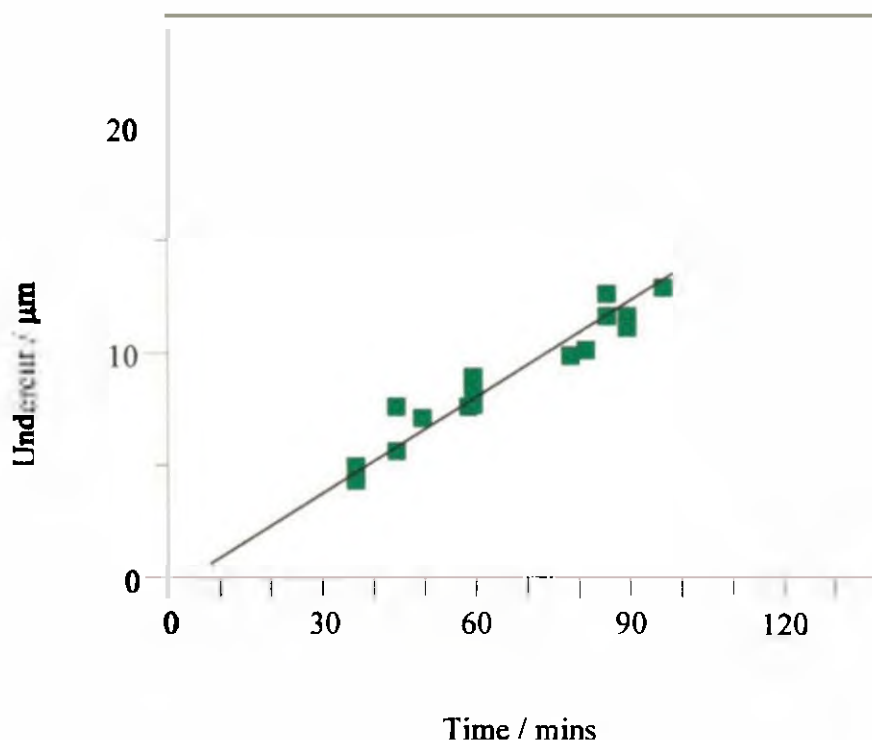

Figure 4.12 Etching Behaviour of etchant D. on SIMOX material.

The undercut rate for the SIMOX silicon dioxide can be seen to be slightly reduced from that of thermally grown silicon dioxide. This is thought to be due to the different stress and defect levels within the materials.

4.4.1.3 UNDERCUT PROFILE

Following resist removal of the samples used in the initial etch trials, the undercut profile shown in figure 4.13 was revealed by scanning electron microscopy. Tests were undertaken to confirm that the undercut profile was similar in the buried silicon dioxide of the SIMOX material to that in this thermal oxide layer - this was found to be the case.

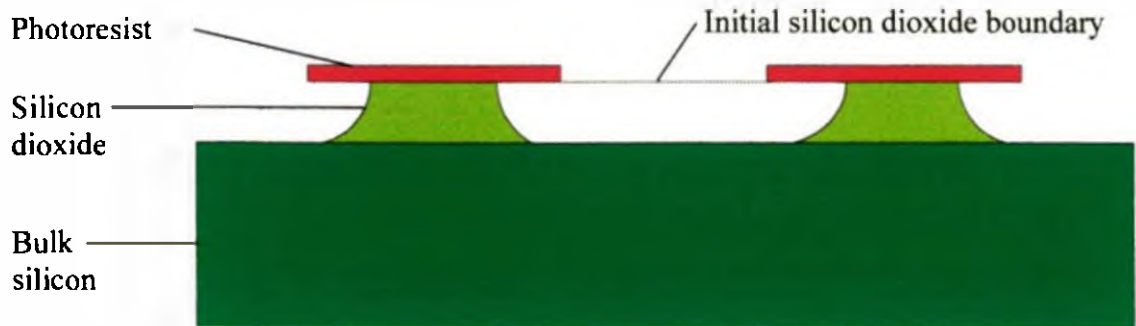

Figure 4.13 Profile of Underetched Silicon Dioxide

4.4.1.4 VERTICAL ETCHING OF BULK SILICON

From measurements of the vertical etch rates, etchants C and D appear to offer the most controllable etching. When combined with the results of the lateral etch tests, etchant D was found to be most appropriate for silicon dioxide etching in sensor fabrication.

The vertical etch trials were also repeated on a thermal silicon dioxide layer using temperature control and a mask offering limited access to the etchant site. As expected, etch limitation by the different mask did not restrict the vertical etch sufficiently to cause a large change to the etch rate. In these trials a vertical etch rate of 0.13 $\mu mmin^{-1}$ was measured at 30 ±0.5 °C.

4.4.1.5 DISCUSSION OF ETCHED PROFILE

The observed profile (see figure 4.13) correlates well with profiles of underetching described in the literature [30], although, in those cases, oxide from the window area was removed previous to underetching by alternative anisotropic means. In the case where low pressure chemical vapour deposition (LPCVD) phosphosilicate glass is being underetched [27], this profile is accounted for by a vertical variation in the phosphorus content of the film and/or by stress variations through the film. Increases in either parameter have been found to result in a faster etch rate [31].

In the case of vertical etching of thermal silicon dioxide, a slowing of the etch rate has been observed toward the substrate boundary [32]. This is considered to be due to a partial densification of the lower silicon dioxide layers. In our case, we would expect the final undercut profile to be accounted for partially by the initial shaping of the etch well, since removal of the silicon dioxide in the window did not precede wet etching, as in literature examples of undercutting. This may be combined with the effects of densification and/or stress. Furthermore the buried oxide in implanted wafers is known to have a Gaussian oxygen distribution which may cause some slight variation in etch rate through the layer [7].

4.4.1.6 DISCUSSION OF LATERAL ETCHING

During underetching, as the etch front progresses, the reaction may change from kinetic control to diffusion control. Here a combination of several effects may occur, such as a build up of reaction products in recessed areas and progression of reactant molecules towards the reaction site, which is slowed by product molecules diffusing away from it.

The underetch rate of 0.16 $\mu m min^{-1}$ for thermal silicon dioxide, deduced from experiment as described, is high compared with a literature value of 0.057 $\mu m min^{-1}$ for low temperature, LPCVD silicon dioxide using the same etchant composition as in this work at a lower temperature of 25 °C [22]. The mask geometry is not discussed in this report, but silicon dioxide layers were 0.5 μm and 1 μm in thickness. Using a stronger etchant composition of 6.4 v% HF, 35 v% NH_4F and 58.6 v% H_2O a lateral etch rate of 0.047 $\mu m min^{-1}$ is reported for thermal silicon dioxide etching at 30 °C [33]. Again, the geometry is not given, in this case the silicon dioxide layer thickness was 0.5 μm. The variance in the reported etch rate is likely to be accounted for by the differences in the etch conditions between the different studies.

Doping of silicon dioxide is known to have a dramatic effect on the vertical etch rate [28]. This explains the reported, increased lateral etch rate of 2.3 $\mu m min^{-1}$ for 8 w% phosphosilicate glass (PSG), etching in 7.5:1 volume part HF: water, used at 25 °C [27]. This compares with underetching rates for 6 % PSG of 1.11 $\mu m min^{-1}$ with 3.6 % HF and 20 $\mu m min^{-1}$ with 49 % HF, both used at 23 °C, reported by Lui [23].

The latter two reports [23, 27] both refer to the underetching of long channels and provide detailed insight into the lateral etching behaviour.

There are two main differences between these works by Lui [23] and Monk [27] and the current work carried out in pressure sensor fabrication:

(i) The materials: deposited PSG not implanted oxide is the material being etched.

(ii) The geometry: long channels are underetched from an etch window opened through the oxide layer, instead of circular areas, from a small central mask opening.

In both cases a model is derived to describe the etching behaviour observed experimentally. It was found that as the etch front progresses, the etching becomes diffusion limited and the plot of etch distance versus time deviates from its linear characteristic, indicating a decreasing lateral etch rate. This effect is possibly increased due to the large molecular size of the reaction product, fluosilicic acid [27].

In the first paper of this type to be published, by Monk [27], channels of 8 % phosphorus LPCVD PSG framed on either side by polysilicon and above with transparent silicon nitride are fabricated in a variety of dimensions from 10-100 µm long and 1-5 µm wide. The channels are 2.2 µm in height and the etch window is opened through the silicon dioxide layer to produce an initially vertical etch front. Etching of the channels was carried out at 25 °C, in a number of different concentrations of HF. Errors in the experimental data may have resulted from continued etching along the channels subsequent to removal of the sample from the etch tank, but prior to measurement [27]. This will also be the case in our work, where the undercut from a central window was measured subsequent to sample removal from the etchant and rinsing. A first order Deal-Grove model [34] has been applied to describe the observed etching behaviour, by Monk [28]. In the derivation, several assumptions were made, these are that there is:

(i) one component diffusion

(ii) one dimensional geometry

(iii) a constant diffusion coefficient

(iv) immediate transportation of reaction products to the surface

(v) negligible heat generated at the reaction front

(vi) constant density in the solution

To derive the model, the diffusive flux [27]:

$$J = \frac{D_{HF-H_2O}\left(C_{HF} - C'_{HF}\right)}{\delta} \qquad (4.2)$$

where

D_{HF-H_2O} = the diffusivity of HF in water
C'_{HF} = the concentration of HF in the bulk solution
C_{HF} = the concentration of HF at the oxide surface
δ = the undercut distance

Can be equated to a reactive flux [27]:

$$J = kC'_{HF} \qquad (4.3)$$

where

k = the first order reaction rate constant

This can be expressed as a movement of the etch front as a function of time [27]:

$$\delta = \frac{D_{HF-H_2O}}{k} \pm \sqrt{\left(\frac{D_{HF-H_2O}}{k}\right)^2 + \frac{4D_{HF-H_2O}C_{HF}[MW]_{HF}}{[\rho]_{SiO_2}}t} \qquad (4.4)$$

where

$[MW]_{HF}$ = the molecular weight of hydrofluoric acid
$[\rho]_{SiO_2}$ = the density of silicon dioxide

In the reported work [27] plots were drawn of the Deal-Grove equation using estimates from alternative sources [34] for the reaction rate constant of $1.45\text{x}10^{-6}$ cms^{-1} and diffusivity of $3.1\text{x}10^{-5}$ cm^2s^{-1}. These plots were seen to fit the experimental data well at low etch times but deviated from the experimental data at longer etch times. Both the reaction rate constant and diffusivity were then adjusted to allow the plot to

fit the experimental data. In this way, a good fit could be obtained. The diffusivity required to fit the data in the reported work [27] was found to be of the order of 10^{-9} cm^2s^{-1}, this is approximately four orders of magnitude lower than that for most liquids. This indicates that the reaction does display diffusion limitations at longer etch times, in the published graphs [27] the onset of diffusion limited etching was observed after between 4 to 35 minutes, depending on the solution concentration. The variations in reaction rate constant seen for the various etchant compositions tested in the work [27] suggested that the reaction is not first order. The value for reaction rate constant determined for the 6.68 M solution was 7.83×10^{-8} cms^{-1}. This is the solution discussed in the literature [27] closest to the concentration of HF used in our experiments (5.99 M).

The work reported by Monk [27] which is outlined above was criticised in a subsequent publication by Lui [23] for not being tested across a wide enough spectrum of solution concentrations to allow the model to be considered universal. A further inadequacy in Monk's work was the lack of experimental data. The low number of points at higher etch times, in some cases makes the standard of fit difficult to assess.

In the current work, the Deal Grove equation derived by Monk was fitted to the experimental data gained from the undercut trials on SIMOX samples, in which the temperature was controlled to 30 ±0.5 °C. Initially estimated values for reaction rate constant and diffusivity were used. As in the literature, a deviation was seen between the plot and the experimental data at higher etch times, although this deviation was not as great as that reported [27]. Figure 4.14 shows experimental data from the current work and the Deal-Grove equation with the estimated values of diffusivity and reaction rate constant (shown by the solid line). Some discrepancy in this fit would be expected due to the fact that the reaction rate constant will be quite different to the literature estimate since the etch rate is very different (due to the difference in temperature, silicon dioxide formation method and phosphorous content between the two works). As in Monk's report, the diffusivity and reaction rate constant were then adjusted to fit the data, this plot is shown by the dotted line in figure 4.14. The adjusted values are 2.25×10^{-9} cm^2s^{-1} for diffusivity and 7.97×10^{-12} cms^{-1} for reaction rate constant.

This value of diffusivity agrees well with that determined by Monk for HF underetching, and is approximately four orders of magnitude smaller than that observed in 'open' etching. This indicates that the undercut etching in the current work did experience diffusion limitation, which slowed the etch rate down. The circular geometry, used in pressure sensor fabrication would seem to cause a similar degree of diffusion limitation to that for channel etching, although the height of the etch channel is greater in the literature structure (2.2 μm) [27] than in our SIMOX structure (0.4 μm).

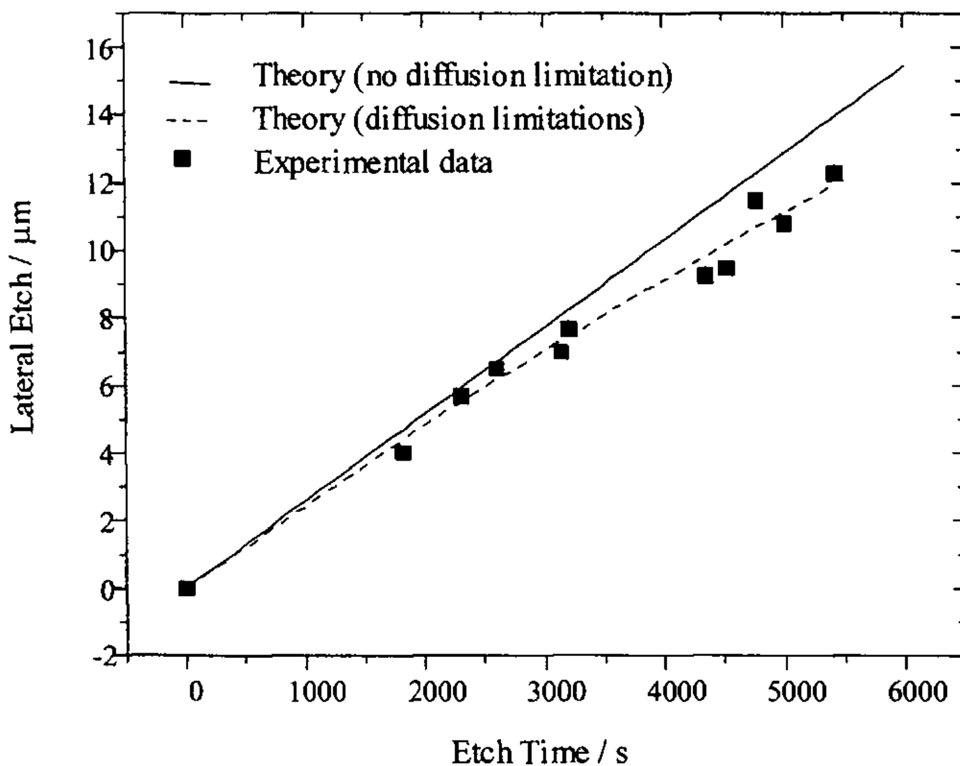

Figure 4.14 The experimental data points with the derived equation plotted with estimated and adjusted values for the reaction rate constant and diffusivity.

Work by Liu, [23] published two years after Monk's work [27], aims to determine a universal model for first and second order reactions incorporating the diffusion limitations experienced in channel etching. Experimental data was obtained from the etching of LPCVD silicon dioxide with a 6 % phosphorus concentration annealed for one hour at 1000 °C [23]. This was patterned into the channel and coated on the three

exposed faces with LPCVD silicon nitride. Prior to wet etching an etch window was opened through the silicon nitride using dry etching. Channels of various dimensions were fabricated, with widths ranging from 4 to 200 μm and heights from 0.24 to 1.7 μm, the channel length was typically 3000 μm. A scale with 10 μm divisions was integrated on the structure to allow assessment of the undercut distance.

Experimental data gained by Lui [23] did display a deviation from the linear, indicating diffusion limitation. However, in this case the limitation is only observed at etch distances greater than 100 μm. Liu assesses several models, the diffusion [35], Deal-Grove [27] and Langmuir-Hinshelwood [36] models were all found to be inadequate, failing to fit the experimental data across the full range of concentrations examined.

The 'universal' combined first and second order model derived by Liu [23] gives a good fit across the full range of concentrations tested in his work. However, when this universal model was applied to the data for SIMOX etching, a good fit could not be gained. Attempts to reproduce Liu's curves from details in the paper were also unsuccessful indicating that there may be some errors in the published information [23].

In Lui's work [23] the effects of temperature, channel size and the production of bubbles was also examined. The assessment of the effects of temperature showed that, initially, raised temperature causes the etch rate to increase, but after approximately 100 minutes of etch time, the underetched distance in channels etched at different temperatures is comparable; this was considered to be due to the production of bubbles which occur around this stage of the process, enhancing convection [23]. However, this could also indicate that temperature affects the etch rate while the process is reaction controlled (as would be expected) but when diffusion becomes the limiting factor temperature does not affect the diffusion effects as strongly. However, the published work [23] only describes two temperatures, separated by just 12 °C and therefore any conclusions drawn can be considered to be of limited value.

It has been concluded by Lui [23], that the width of the channel, has no effect on the etch rate while the height does, with thinner channels etching slower, considered to be due to surface interaction or limited flow. This seems somewhat unrealistic as the

channel height and width are interchangeable, simply by etching the sample on its side. The more critical factor in the variation of etch rates would seem to be the ranges within which these dimensions have been tested, it could be inferred that at widths or heights greater than 4 μm, any increase in dimensions does not adjust the etch rate. While at widths or heights below 1.7 μm, a decrease in dimensions is accompanied by a reduction in the etch rate.

Bubbles were reported [23] to form in the channels which was unexpected as the HF, silicon dioxide reaction is not thought to yield any gaseous product. The bubbles were seen to form at the etch front and move towards, and out of the etch window, while increasing in size. The effect of bubble formation on etch rate was dependant on both channel dimensions and temperature. The presence of bubbles was also observed in the etching of SIMOX carried out in this project but did not appear to have any detrimental effect on the etching.

4.4.1.7 SUMMARY OF WET SILICON DIOXIDE ETCHING

Following consideration of all the results of this study, etchant D was considered appropriate for silicon dioxide etching in pressure sensor structure fabrication. The formulation of the selected etchant D was:

- **7:1, NH_4F : HF**
- HF 60 ml
- NH_4F 420 ml
- Temperature 30 °C
- Agitation moderate

The SIMOX etch rate was determined as 0.13 $\mu m min^{-1}$ although there was some evidence of non-linearity at higher etch times. A Deal-Grove model was applied which gave a good fit to our experimental data and indicated diffusion limitation as the cause of the non-linearity.

Adjustments to etch compositions, suggested in literature sources, such as the addition of surfactants [37] or use of vapour phase HF [24] were not considered necessary, as

satisfactory etching was achieved with the above composition alone. Furthermore the anti-stiction reduction benefits of vapour HF etching are made irrelevant by the necessity for post etch rinsing to remove silicon dust.

In addition to the selection of etchant D, this study served also to demonstrate that undercutting of the required dimensions is achievable and confirmed the feasibility of using time to control the extent of underetch and hence diaphragm size and ultimately, pressure measurement range.

4.4.2 DRY SILICON DIOXIDE ETCHING

Reactive ion etching was considered as an alternative to wet techniques for the silicon dioxide underetching step. The conditions used would be required to result in highly isotropic silicon dioxide etching with selectivity over silicon and photoresist. In order to compare with wet techniques, a rate of underetching in the region of 6 $\mu m hour^{-1}$ was required. Although an unusual set of requirements for dry processing, the use of this method of etching would eliminate the occurrence of stiction by removing the presence of liquid. However, it is difficult to achieve a high selectivity over silicon and resist using the same silicon dioxide etching system. A selectivity of 1:15, silicon : silicon dioxide has been reported with CHF_3 [38] and the addition of oxygen further enhances selectivity (although this was not an option on the equipment used in this project). These parameters were used with low power as a starting point for tests, along with a second system reported to give a 1:11 silicon to silicon dioxide selectivity [39]. The two sets of conditions are listed below. Cl_2 [40] has been reported as demonstrating slightly isotropic etching (this was also unavailable on the equipment used in this project). Dry etch systems tested:

- Power density = 0.5 Wcm^{-3}
- RF Power = 13.56 MHz
- Gas pressure = 30 mT
- Si etch rate = 20 $Åmin^{-1}$
- SiO_2 etch rate = 300 $Åmin^{-1}$
- $Si:SiO_2$ selectivity = 1 : 15 [38]

- Power density = 0.45 Wcm^{-3}
- RF power = 13.56 MHz
- Gas pressure = 20 mT
- Flow rate = 20 sccm
- Si etch rate = 60 $Åmin^{-1}$
- SiO_2 etch rate = 680 $Åmin^{-1}$
- Si:SiO_2 selectivity = 1 : 11 [39]

These parameters were then varied in a controlled manner in an effort to achieve isotropy. In particular, the effects of high gas pressure combined with high power were examined. Under these conditions a high radical concentration and high temperature exist, resulting in a predominance of chemical (rather than physical) etching. This was expected to produce the highest degree of isotropy.

Following several tests, no set of conditions had shown sufficient isotropy or the reported selectivity. This is not surprising for a number of reasons:

- RIE is primarily a directional technique
- RIE is equipment dependent, making it difficult to replicate reported work
- Complete parameter sets are rarely reported in the literature

This method of etching was therefore not used in the production of sensors.

4.5 STICTION

Stiction is the adhesion to the substrate of a microstructure which is intended to be suspended [41]. In many cases, subsequent release is not possible, resulting in complete device failure. This phenomenon is a significant microfabrication problem which persists in many fields of micromachining, having been acknowledged and investigated by several researchers [42]. The consensus of opinion suggests that surface tension produced by the drying rinse water is the mechanism for pulling the microstructure toward the substrate. There it becomes permanently fixed by a

combination of Van der Waals and other atomic forces. In pressure sensor fabrication, stiction occurred during the drying of rinse water within the cavity, following the underetch step. This caused the collapse of a high percentage of the underetched structures formed in the initial fabrication of the pressure sensing devices and sensor yield was very low.

To combat stiction, a sequence of additional rinse steps was developed and implemented in the fabrication process following the HF etch and DI water rinse. This exposed the diaphragms to liquids of increasingly lower surface tension [43]. Firstly a 30 minute soak in IPA was carried out, followed by a 30 minute acetone soak and finally a chloroform soak. In each case, the solvents were put into beakers at approximately 70 °C. The samples were then placed immediately in the solvents and covered. Each beaker was placed directly in an ice bucket for rapid cooling. Following the rinse sequence, the samples were oven heated for one hour at 150 °C and exposed to HMDS vapour (as in the photolithographic process). This is reported [44] as preventing stiction from re-occurring in subsequent processing or diaphragm/substrate contact. This procedure resulted in a dramatic increase in the yield. For a matrix of 2500 diaphragms, an estimation of the yield, achieved by counting the number of collapsed structures under an optical microscope, was ~ 99 %, following the introduction of these rinses compared with ~ 15 % prior to their use.

4.6 OTHER FABRICATION PROBLEMS

In addition to stiction in initial etch trials the device yield was also reduced by cracking in the top silicon layer (see figure 4.15). The cracks were observed, originating from the sharp corners of the etch windows and were possibly due to stress concentration. Furthermore, the window size was considered to be too large, reducing the membrane tension and therefore its ability to remain self-suspending. As a consequence of these two observations, the mask for pressure sensor fabrication was designed to define small, circular etch windows. These adjustments resulted in a significant reduction in cracked structures.

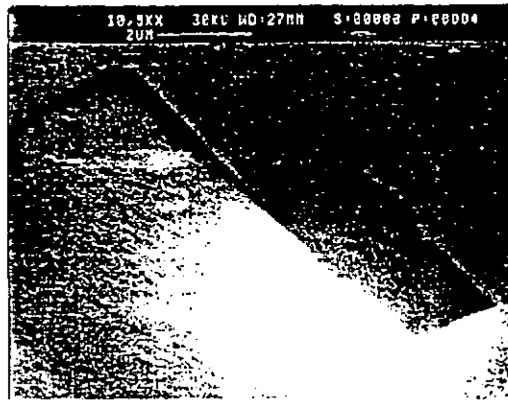

Figure 4.15 Cracking produced from the corners of the etch windows

Optical microscope observation of the sensor samples following the HF etch and rinse steps revealed some areas of surface staining as shown in the micrograph of figure 4.16. Within the circular stained areas, the diaphragms had broken away from the surrounding substrate. Immediately outside these regions, diaphragms were etched and remained suspended in the usual manner. This did not significantly reduce the yield, as staining covered a small area compared with the matrix size (generally encompassing only approximately 10 diaphragms) and more commonly occurred at sample edges, outside the matrix area. Energy dispersive x-ray (EDX) analysis and raman spectroscopy of these areas did not reveal any differences from the adjacent regions of the sample. Similar circular surface stains have been reported by Kikyuama [37], with the suggested cause being hydrogen bubbles liberated from the silicon/HF reaction, which adhere to the surface, causing non-uniform etching. The trapping of air in HF solutions can also cause staining and etch defects as a result of foam adhesion to the etching surface. In this case, stains are described as discolorations, thought to be ≤ 20Å thick, which occur for a variety of etch conditions [45], but are more prevalent for boron doped samples. These stains reportedly appear upon sample removal from the HF bath and immersion into rinse water; which corresponds with observations in the current work. Following analysis, Schimmel [45] concluded that the stains originated from sub-oxides of silicon resulting from incomplete oxidation. The suggested methods for avoiding these effects include a 15 second immersion in 2:1 HF:0.038 M $KMnO_4$, (a strong oxidising agent), following the etching [45]. This was not implemented in the process sequence for pressure sensor fabrication due to the infrequent occurrence of staining within the patterned areas.

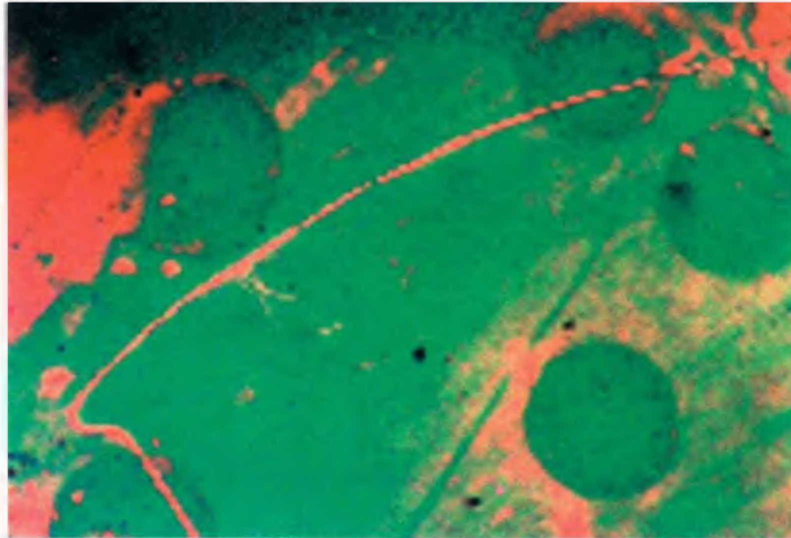

Figure 4.16 An optical microscope micrograph of surface staining subsequent to the BHF etch step.

4.7 METALLISATION

In order to take electrical measurements from the pressure sensor diaphragms, metal connections are required. For the packaged, tested devices and for most test structures, aluminium was the metallisation used.

4.7.1 ALUMINIUM DEPOSITION

Aluminium was deposited by magnetron sputtering with the sample either stationary or rotating. In most cases a 3 minute static deposition was used which resulted in an aluminium thickness of 0.269 μm. A rotating holder allowed multiple sample deposition, in this case, a 33 minute deposition was used to achieve a similar aluminium thickness. A 'customised' holder was constructed to accommodate the small sample sizes used in the sensor fabrication. This was a standard wafer size metal plate with a hole cut in it. The hole was slightly smaller than the sample which was placed behind the hole. The SIMOX was secured in place using a wire clip as shown in figure 4.17.

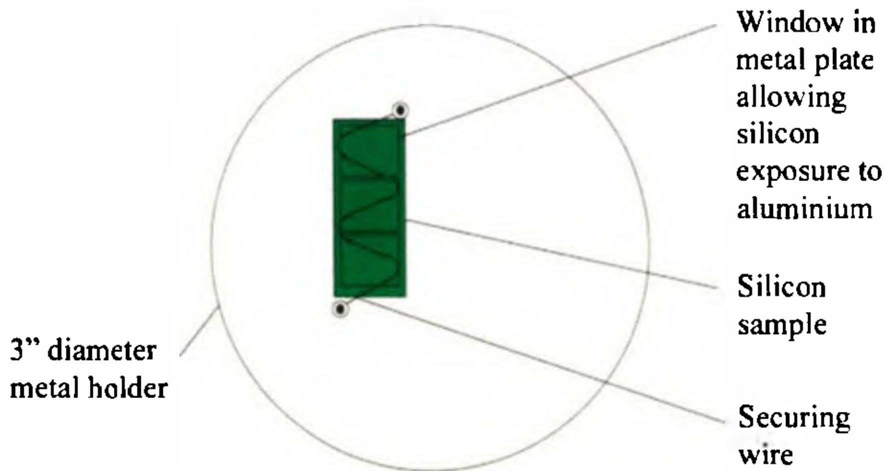

Figure 4.17 Typical sample holder for metal deposition

4.7.2 ALUMINIUM ETCHING

The aluminium layer was masked using positive Shipley resist 1813 and wet etched in a Merck aluminium etchant (containing phosphoric acid) at 50 °C. Etching was terminated by sample removal when, by observation with the naked eye, the aluminium was judged to have been removed from the unmasked areas. This point occurred suddenly and could readily be seen. The time required to etch the 0.269 µm thick layer was approximately 4 minutes. Samples were then rinsed, dried and examined under an optical microscope. If necessary, they could be replaced in the etchant for a short additional etch time. The mask used for sensor metallisation consisted of a matrix of rings to surround each diaphragm. These were 10 µm wide and the outside diameter of the ring was 63 µm. Each ring was connected by a track to a large bond pad.

4.7.3 PROTECTION OF METALLISATION

Experiments demonstrated that the aluminium was attacked during the silicon dioxide etch step, despite the protection of a photoresist mask. With the standard photolithographic process, approximately 65 % of the aluminium had been removed on completion of the silicon dioxide etch. The attempts to develop a system by which metallisation and the long buffered HF step could coexist are detailed below, they

have been tabulated in tables 4.2 to 4.9 for clarity. The success of each method was assessed by the percentage of aluminium 'ring' structures remaining after HF etching for 50 minutes. In the cases where gold was tested as an alternative metallisation, it was deposited by evaporation for seven minutes using a SEM coating unit. Gold etching was achieved using a 1813 resist mask in a composition of 2 g I_2, 8 g KI and 80 ml water. The layer was typically etched in one minute.

Firstly protection of the aluminium with negative photoresist or positive resist after a variety of heat treatments was tested. This failed to provide sufficient protection to the aluminium through the HF etch.

No	Method	Reason	Details	Success
1	Negative resist	Test improved HF resistance compared to positive	Negative resist applied by the procedure outlined in section 4.1.1	No better than the standard process
2	Double layer of positive resist with increased bakes	Test increased HF resistance	Applied as standard with softbake 1 min/105 °C post exposure bake 7.5 min/90 °C hardbake 20 min/150 °C	35 % of aluminium remained after HF etching
3	Double layer of positive resist with increased bakes	Test increased HF resistance	Applied as standard with softbake 2 min /105 °C post exposure bake 10 min/90 °C hardbake 20 min/150 °C	40 % of Al remained after HF etching

Table 4.2 Trials with negative and positive resist with varying bakes

Lift off techniques were also tested to allow deposition and patterning of the aluminium after diaphragm formation as summarised in table 4.3. This also proved unsatisfactory due to incomplete removal of the resist and therefore the metal layers. Several photolithographic techniques for lift off were attempted, but none resulted in a high lift off yield. This was thought to be due to:

(i) The design of the metallisation, which comprised many isolated structures requiring each to be sufficiently attacked by acetone.

(ii) The use of sputtering rather than evaporation for the metal deposition with more likelihood of metal deposition on the sidewalls of the resist profile

(iii) The effect of the harsh environment of the magnetron sputterer on the resist coat - inhibiting its removal.

No	Method	Reason	Details	Success
4	Lift off	To allow metal deposition after cavity etching	Positive resist deposited as outlined in section 4.2.1 to protect diaphragms in Al deposition Patterned with inverse of Al etch mask	Incomplete resist removal in lift off leaving areas of undefined aluminium
5	Lift off with thick resist	To give longer resist sidewall to profile for improved lift off	standard resist application excepting slower spin speed of 200 rpm.	Incomplete resist removal in lift off leaving areas of undefined aluminium
6	Lift off with double layer of resist	To give longer resist sidewall to profile for improved lift off	Second resist coat was applied and softbaked. Exposure and develop times doubled	Incomplete resist removal in lift off leaving areas of undefined aluminium
7	Lift off with staggered profile (figure 4.18)	To give improved resist profile for lift off	First layer exposed for longer - second layer for shorter - times to give a staggered profile as shown in figure 4.18	Incomplete resist removal in lift off leaving areas of undefined aluminium

8	Lift off with PREDA-914-EZ resist	To give improved resist profile for lift off	Applied by the process outlined in section 4.2.1	Incomplete resist removal in lift off leaving areas of undefined aluminium

Table 4.3 Lift off trials

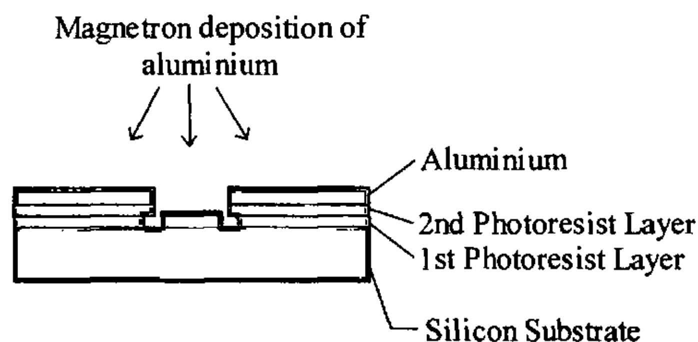

Figure 4.18 Aluminium Deposition Over Staggered Photoresist Profile.

Despite well documented adhesion problems with gold single layer contacts, the unreactive nature of the metal made it attractive for this application due to high resistance to HF attack. However, the experiments conducted, which are summarised in table 4.4, indicated that the gold/resist bond was stronger than the gold/silicon bond, causing the pads to 'float' off after a fairly short time in the HF.

No	Method	Reason	Details	Success
9	Gold metallisation	Improved HF resistance compared to Al	Sample surface cleaned, HF dipped and gold deposited for 7 minutes. Gold etched with a positive resist mask	Gold lifted substantially during gold etching due to poor adhesion

10	Gold metallisation on a sputtered surface	Improved gold adhesion	Silicon surface prepared by RIE sputtering in 5% Ar prior to gold deposition	Gold still lifted during gold etching

Table 4.4 Trials with gold on silicon contacts

Gold aluminium bilayer contacts were also examined, but were only expected to allow fairly immediate sensor testing and not to be a solution for the provision of permanent device contacts due to doubts about the long term stability of this arrangement. However, the trials, summarised in table 4.5, did not prove successful in retaining sufficient metallisation through HF etching. Either the gold adhesion to the aluminium was poor and hence the gold protection was removed, exposing the aluminium to HF, or the HF attacked the aluminium under the gold, reducing the bonding area, releasing the gold pads. However, by the end of the etch step, this had retained a higher percentage of the metallisation than any of the previous methods.

No	Method	Reason	Details	Success
11	Bimetal layer of gold on aluminium	Gold protects Al and Al improves contact quality and gold adhesion	Al sputtered, defined and sintered then gold sputtered, patterned in alignment and etched	The Al became exposed for attack, but better results than previous trials - demonstrated on SIMOX – 45 % remain after HF but corrosion concerns (see section 2.4)

Table 4.5 Trials with gold on aluminium contacts

Direct bonding was tested, see table 4.6, in the absence of success in achieving sufficient metallisation by conventional means. It was considered that this method may allow some electrical assessment of the sensor structure. The most successful way of achieving this was determined to be using conductive epoxy to join the gold wire to the sensor surface.

No	Method	Reason	Details	Success
12	Direct wire bonding	To allow sensor testing	Die held at 370 °C - the eutectic temperature for silicon and gold	Gold softened and blocked capillary - no ball contact formed
13	Direct wire bonding	To allow sensor testing	Epoxy deposited in area where pad should be - gold wire dipped in this and the other end ball bonded to the package	Successful contact formed

Table 4.6 Direct wire bonding to silicon

Since aluminium masked by a double resist layer with heat treatment was largely retained during the early stages of HF etching up to a time of 20/25 minutes (reported in table 4.2, trial 3), a double etch step process was proposed, remasking the sample midway through the full etch time required for diaphragm formation. This was successful, but the cost, time and labour intensive nature of a second photolithographic and alignment step is a strong argument against using this method as a practical solution to electrical device contact, the process is summarised in table 4.7.

No	Method	Reason	Details	Success
14	Double masking	To re-protect aluminium by remasking midway through HF etch	Sample removed from HF, rinsed, remasked and then replaced in etchant for remaining time	after initial 15 minutes of etch time 80 % of the metallisation remained

Table 4.7 Trials with two step mask and etch process

A thicker aluminium layer was deposited as described in table 4.8 to investigate whether this would allow enough of the layer to remain after hydrogen fluoride etching to allow wire bonding. An aluminium layer dynamically deposited for 2 hours withstood HF etching more successfully than the previous experiments. However, considerable amounts of the aluminium had still been removed. Following this relative success, aluminium was deposited for 3 hours on a silicon-on-insulator sample and masked with a double layer of photoresist. During HF etching, aluminium attack was monitored after 15, 27 and 39 minutes. After a total of 45 minutes, almost all aluminium remained, although the surface appeared rough, indicating some etchant attack. Subsequent examination with the scanning electron microscope confirmed the uneven surface and revealed the presence of regular rectangular pits (see figure 4.19).

No	Method	Reason	Details	Success
15	Thick aluminium layer	To allow sufficient aluminium for bonding to remain after HF etching	2 hour aluminium deposition carried out, then etched (longer etch time) and sintered as standard, double resist coat used to protect metal	Following HF etching approximately 47 % of the aluminium remained

16	Extra thick aluminium with double resist coat	To allow sufficient aluminium for bonding to remain after HF etching	3 hour aluminium deposition carried out, double resist coat applied as standard procedure with no extra bakes	All aluminium areas remain but their surface is roughened after 15 minutes of etch but remains the same to the end. Rectangular etch pits present

Table 4.8 Trials with thick aluminium layers

A specialised photoresist application technique was also considered as a means of sensor protection for post fabrication metallisation (see section 4.8), this is summarised in table 4.9. This photoresist was patterned using a negative of the metallisation mask. Aluminium was then deposited and, since it had previously been established that lift off was not a viable option, a second photoresist layer was spun and exposed on top of the sputtered aluminium and the metal was etched and the photoresist removed. The aluminium surface appeared smooth and of high quality, allowing the successful combination of metallisation and HF etching. A second sample was treated in a similar way but without the first layer of resist as protection. This also gave good results with no residue aluminium observed in the cavity following metal etching. This method was therefore chosen for subsequent sensor fabrication as it avoided the additional photolithographic stcp and metal roughness of the previous successful trial.

No	Method	Reason	Dctails	Success
17	Aluminium deposited after HF etch with resist diaphragm protection	To avoid Al exposure to HF	Photoresist applied as outlined in 4.8 to cover the open diaphragms	This worked well but in some cases the resist provcd difficult to removc

18	Aluminium deposited after HF etch	To avoid Al exposure to HF	No resist protection. Relied on aluminium etch accessing all areas in which aluminium was deposited	This worked very well

Table 4.9 Trials with aluminium deposited after cavity formation

4.7.4 ALUMINIUM SINTERING

Subsequent to aluminium deposition and patterning, sintering was carried out to dissolve the surface silicon into the aluminium to form a better ohmic contact. The amount of dissolution which occurs in such a process is dependent on both the solubility at the anneal temperature and the volume of aluminium present.

For sintering, the samples were loaded into a furnace in a quartz boat, raised to 450 °C, with N_2 flowing. Once in position, forming gas was set to flow through the furnace at 2 $lmin^{-1}$ for 30 minutes, after which the samples were slowly withdrawn in a nitrogen flow. This set of conditions, chosen specifically for the SIMOX material, form an ohmic contact without allowing conduction through the buried oxide layer [46].

4.7.5 KIRKENDALL EFFECT

During sintering, voids in the silicon were produced as a result of the slower dissolution rate in the <111> direction. These voids then fill with aluminium. This is known as the Kirkendall effect [7] and results in aluminium spikes protruding down from the sample surface. Figure 4.19 shows the top surface of a SIMOX sample following aluminium deposition, definition, sintering and subsequent removal. Pits can be seen, resulting from the etching of the aluminium spikes. In figure 4.20, the pits are viewed at a higher magnification to reveal their rectangular nature.

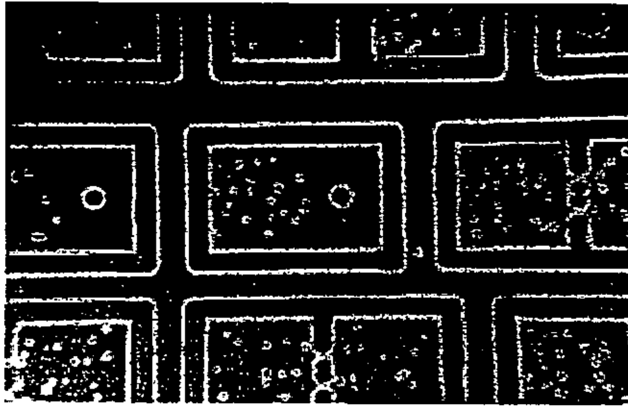

Figure 4.19 Optical microscope photograph of rectangular pits resulting from aluminium spiking.

Figure 4.20 Optical microscope photograph of rectangular pits under high magnification

4.8 CAVITY SEALING

It has been reported that polymers such as photoresist can be spin deposited on a wafer surface in such a way that they form a surface film which seals etched cavities [47]. Due to the surface tension in the spreading phase of the spinning cycle, the resist does not actually enter the cavity. This technique is potentially low cost, IC compatible and avoids the thermal oxidation, LPCVD or sputtering processes which are commonly used to seal structures. These require elevated temperature or vacuum, resulting in environments which are harsh for circuitry and fragile microstructures.

This polymer spin technique can also be applied to the fabrication of buried capillaries, valve membranes and thermally isolated microstructures. The reported procedure involves a polymer dispensed at 200 rpm. Spinning was then maintained at 200 rpm for a further 2 seconds after which the wafer was accelerated at 1667 $rpms^{-1}$ to 8000 rpm where it was held for 30 seconds [47]. This typically gave a resist thickness of 1.72 μm, measured on the alpha step.

To seal the pressure sensor cavities fabricated in this work, an initial spin speed of 500 rpm was used for the dispensing of 1813 photoresist, 2 seconds elapsed before the spin speed was raised within 5 seconds to 8000 rpm where it was sustained for 30 seconds. In the published work [47], the photoresist layer was retained as a complete surface covering. In sensor fabrication, photolithographic definition of this sealing layer was carried out to retain photoresist only over the diaphragm central opening. In this way the diaphragm behaviour was expected to remain broadly dependent on the physical attributes of silicon.

During patterning of the sealing resist coat, a low exposure time of 15 seconds was used in conjunction with the negative of the mask used to define the etch windows. This was intended to produce a circular resist plug slightly larger than the opening to ensure complete cavity sealing. On examination, the plugs appeared to be successfully sealing the diaphragm. In some cases on test structures examined on the scanning electron microscope the photoresist was seen to bulge (see figure 4.21), which may have been due to internal gas expansion due to heat generated by the electron beam.

Figure 4.21 Spun on sealing layer 'bulging' under SEM conditions.

4.9 SUMMARY

The novel fabrication of an array of micro-miniature diaphragms to form a capacitive pressure sensor has been carried out. The sensor structure was produced by the fabrication sequence developed in this work, involved the removal of a section of the buried oxide layer of the SIMOX material using time controlled isotropic etching. Access to the buried oxide was gained via a window in the silicon top layer formed by anisotropic etching. As a result of this lengthy etch, metallisation was unusually deposited after diaphragm formation in the penultimate process step. Sealing of the cavities with photoresist applied by a specialised spin cycle was finally implemented. This work has demonstrated the feasibility of fabricating pressure sensing devices using a novel combination of SIMOX material and underetching techniques.

The processes to be used in sensor fabrication were experimentally characterised and optimised for use with SIMOX material. This provided information regarding non-standard processing techniques used to address issues specific to this work. These are not reported in literature and hence the work enabled an effective 'recipe book' for the manufacture of SIMOX sensors to be assembled with the identification of specific etchants and conditions for each etch step. These were $KMnO_4$, HF, H_2O at 25.5 °C with mild agitation for SIMOX silicon etching at a vertical rate of 0.4 $\mu m min^{-1}$. HF and NH_4F at 30 °C were used for the repeatable, controlled underetching of the SIMOX buried silicon dioxide layer with a lateral etch rate of 0.13 $\mu m min^{-1}$. These process steps were then adjusted to improve the yield including the introduction of a series of low surface tension rinses. Subsequently, diaphragms were reliably and repeatably fabricated with high yields.

Several benefits over traditional structure device fabrication can be seen for the processing technique developed here including; the avoidance of sacrificial layer growth, bonding and the need for implanted etch stops. The process is simplified over many reported techniques by the single sided approach and the use of reduced mask steps which both have time and cost implications.

Single pressure sensing elements were initially fabricated to demonstrate the feasibility of this novel etch technology combined with the silicon-on-insulator starting substrates. Multiple pressure sensing matrices were then fabricated for testing

to confirm the operation and give an indication of the performance of the novel sensing structure. The final device structure and results of the performance testing are presented in chapter 5.

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CHAPTER 5: DEVICE RESULTS

5.0 INTRODUCTION

5.1 CAPACITIVE PRESSURE SENSORS

5.1.1 FABRICATION SEQUENCE FROM SIMOX

5.1.2 ANALYSIS OF FABRICATION DIFFICULTIES

5.1.3 FUNCTIONAL DEVICE STRUCTURE

5.2 SIMOX CAPACITIVE PRESSURE SENSORS, SINGLE AND ARRAY STRUCTURES

5.3 OVERVIEW OF CRITICAL SENSOR PERFORMANCE PARAMETERS

5.4 SET UP FOR PRESSURE SENSOR MEASUREMENT

5.5 CAPACITANCE-VOLTAGE (C-V) ANALYSIS

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5.8 SUMMARY

5.9 REFERENCES

5.0 INTRODUCTION

Chapter 4 has reported on the development of a suitable fabrication procedure for the novel pressure sensor which has achieved high yield. Chapter 5 concentrates on the characterisation of the sensors with respect to their performance in a sensing application. The change in capacitive output under various applied pressures and temperatures was measured. Although without the aid of any circuitry, parasitic capacitance was expected to be high and the equipment had poor resolution for the capacitance range, it was hoped to demonstrate at least the potential for high

performance from this type of sensor. Before describing the testing procedures and results the final, complete and optimum fabrication sequence for the device is given followed by micrographs of the single and array structures. In the final part of this chapter, the performance measurements made on the SIMOX pressure sensors which have been fabricated, are reported and analysed. The critical sensor parameters outlined in section 5.3 are then compared with both the expected performance and that of similar pressure sensor types.

5.1 CAPACITIVE PRESSURE SENSORS

The capacitive pressure sensor fabricated in this project consisted of a matrix of many interconnected single devices. Each device in turn consisted of a thin diaphragm suspended above a cavity. On the application of a pressure the thin silicon diaphragm deflects, this reduces the dielectric gap between it and the silicon substrate from d_1 to d_2. As a result of this the capacitance between the diaphragm and substrate is increased from C_1 to C_2. Using this principle, the applied pressure can be directly related to a change in output capacitance. This allows the measurement of an unknown pressure, by observation of the output capacitance.

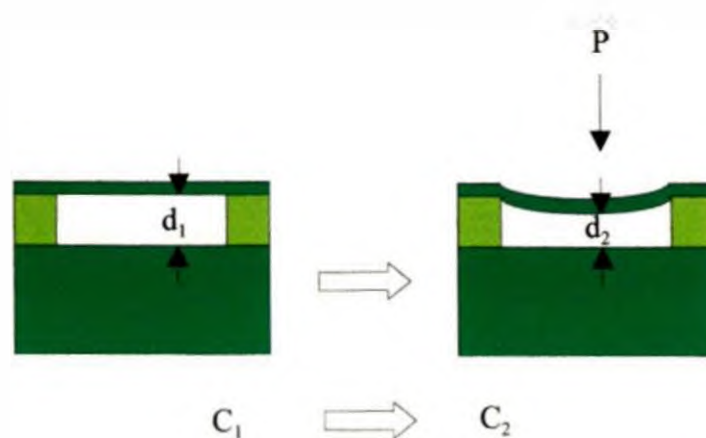


Figure 5.1 A capacitive pressure sensor

In order to eliminate the effects of ambient variations, two such sensors could be packaged together. With only one device exposed to variations in pressure,

comparison of the two outputs (electrical subtraction of one output from the other can be easily carried out) allows the elimination of any unwanted common fluctuations. The degree of variation in capacitance for a particular pressure can be controlled at device manufacture by simply varying either the diaphragm diameter of each individual sensor or the number of units in the matrix. This in turn allows the device to be made appropriate for the measurement of different pressure ranges. For the sensors fabricated, the change in capacitance with pressure was small compared to the base capacitance of the device at atmospheric pressure - this makes measurement difficult and increases the measurement errors.

A range of alternative suspended structures were also fabricated using the same process sequence as the pressure sensor.

5.1.1 FABRICATION SEQUENCE FROM SIMOX

This sequence, which was developed specifically for the production of these pressure sensors during this work, allows simple fabrication of a high performance pressure sensor using predominantly standard photolithographic, etch and deposition processes. This is achieved by application of the sequence to commercially available SIMOX material with a 0.2 μm silicon overlayer on a 0.4 μm buried oxide, table 5.1 summarises the complete fabrication sequence.

Fabrication step	**Process details**	**Equipment**
Material clean	Sulphuric acid / hydrogen peroxide HF dip	Wet bench
Photolithography of SIMOX silicon overlayer	150 °C, 1 hour dehydration bake 20 mins. HMDS 1813 resist application 5000 rpm, 40 s 105 °C, 1 min. softbake 18 s exposure 1.5 mins. develop	Oven Spinner Hotplate Cobilt mask aligner

	150 cc developer / 100 cc water 120 °C, 20 mins. hardbake	 Hotplate
Silicon etching of SIMOX overlayer	0.6 g $KMnO_4$ / 20 cc HF / 280 cc H_2O 25.5 °C, etch time = 50 s	Wet bench and hotplate
Step measurement	4 sites measured to ensure BOX exposed	Tencor alpha step
Resist strip	Acetone / IPA / DI weir plasma ash	Solvent bench Plasmaprep
Time controlled silicon dioxide underetching of buried layer	60 ml HF / 420 ml NH_4F 30 °C, etch time = 50 mins.	Temperature bath PTFE sample basket
Anti-stiction rinses to release microstructure from substrate	IPA / acetone / chloroform 30 mins. in each in pre-warmed beaker	Solvent bench
Undercut measurement	4 sites across sample and estimate yield	Calibrated microscope system
Metal deposition	In sample holder	Magnetron
Photolithography of aluminium layer	150 °C, 1 hour dehydration bake 20 mins. HMDS 1813 resist application 5000 rpm, 40 s 105 °C, 1 min. softbake 16 s exposure 1.5 mins. develop 150 cc developer / 100 cc water 120 °C, 20 mins. hardbake	Oven Spinner Hotplate Cobilt mask aligner Hotplate
Metal etching	Aluminium etchant 50 °C, etch time = 4 mins	Wet bench and hotplate
Resist strip	Acetone / IPA / DI weir plasma ash	Solvent bench
Sintering	Forming gas	Anneal furnace

	410 °C. time = 30 min	
Photolithography to seal diaphragm	150 °C, 1 hour dehydration bake 20 mins. HMDS 1813 resist application 500 rpm dynamic dispense 500 rpm, 2 s 8000 rpm 30 s 105 °C, 1 min. softbake 15 s exposure 1.5 mins. develop 150 cc developer / 100 cc water 120 °C, 20 mins. hardbake	Oven Spinner Hotplate Cobilt mask aligner Hotplate
Final inspection	Confirm yield and quality across sample	Optical microscope / SEM
Packaging	Mount in DIL package gold ball bonding	Wire bonder

Table 5.1 SIMOX pressure sensor fabrication process

Each of these process steps was adapted for the specific requirements of both the SIMOX starting material and resultant micropressure sensor dimensions. Fundamental to the fabrication was the repeatable and controllable vertical dimensions determined by the SIMOX starting material combined with repeatable, well defined underetching of the buried silicon dioxide layer.

A photo-sequence of a pressure sensor during fabrication is provided in Figure 5.2, the left hand sequence shows the fabrication steps schematically, while the right sequence shows corresponding micrographs of the sensor. The basic process steps of (i) silicon etch, (ii) buried oxide isotropic etch, (iii) metallisation and (iv) packaging are shown.

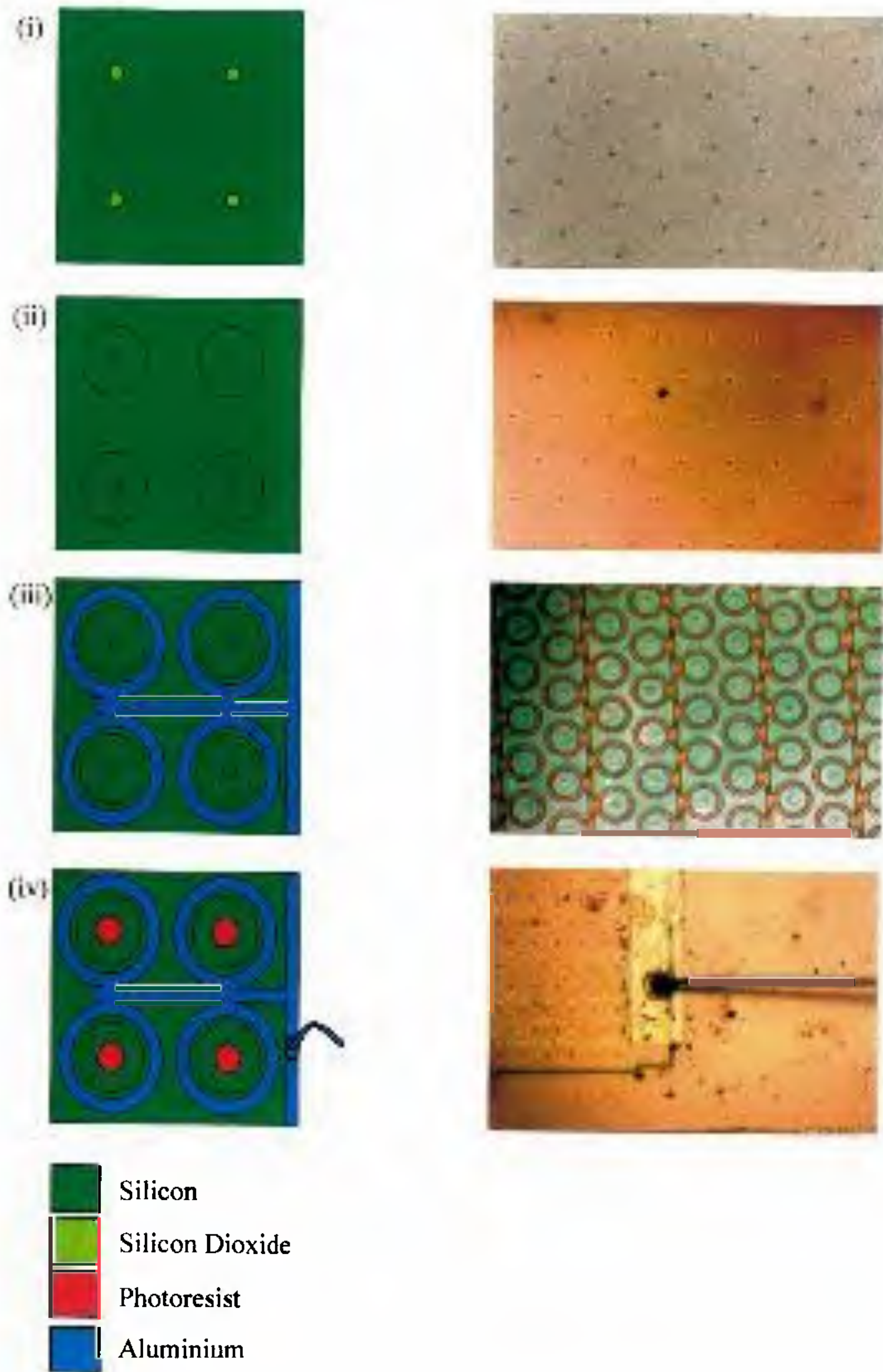


Figure 5.2 Fabrication of a pressure sensor

5.1.2 ANALYSIS OF FABRICATION DIFFICULTIES

Three primary difficulties were experienced during device fabrication - these were observed at the early stages of the sensor development and steps to overcome them, were implemented where possible. These difficulties have been discussed in more length in chapter 4.

- Subsequent to underetching, cracks were seen emanating from the corners of the square etch windows which ultimately resulted in diaphragm collapse. The window design was adapted to a circular opening which overcame this.
- Stiction occurred between the diaphragm and substrate which again resulted in complete diaphragm failure. A sequence of low surface tension rinses was implemented into the fabrication process, post underetch, which virtually eliminated this problem.
- Surface staining occurred on the sample surface following the buffered hydrogen fluoride step possibly due to suboxides [1]. EDX and RAMAN spectroscopy were used to analyse these stains, but no differences from the traces on non-stained samples was observed. Since the occurrence of stains did not significantly affect device yield further analysis or elimination were not attempted.

5.1.3 FUNCTIONAL DEVICE STRUCTURE

The final device structure, shown in figure 5.3, is optimised for both fabrication and operation, incorporating a circular diaphragm. This diaphragm is approximately 17 um in diameter of which 3 or 5 µm is an opening in the silicon layer sealed with a photoresist plug, the remainder is undercut, suspended silicon (dimensionally controlled by the HF etch time). The thickness of this monocrystalline silicon diaphragm is 0.2 um. The height of the dielectric gap between this diaphragm and the substrate is 0.4 µm. Each diaphragm is surrounded by a ring of metal which ultimately connects with the metal bond pad 100 um by 3328 µm in size, which allows external electrical connection.

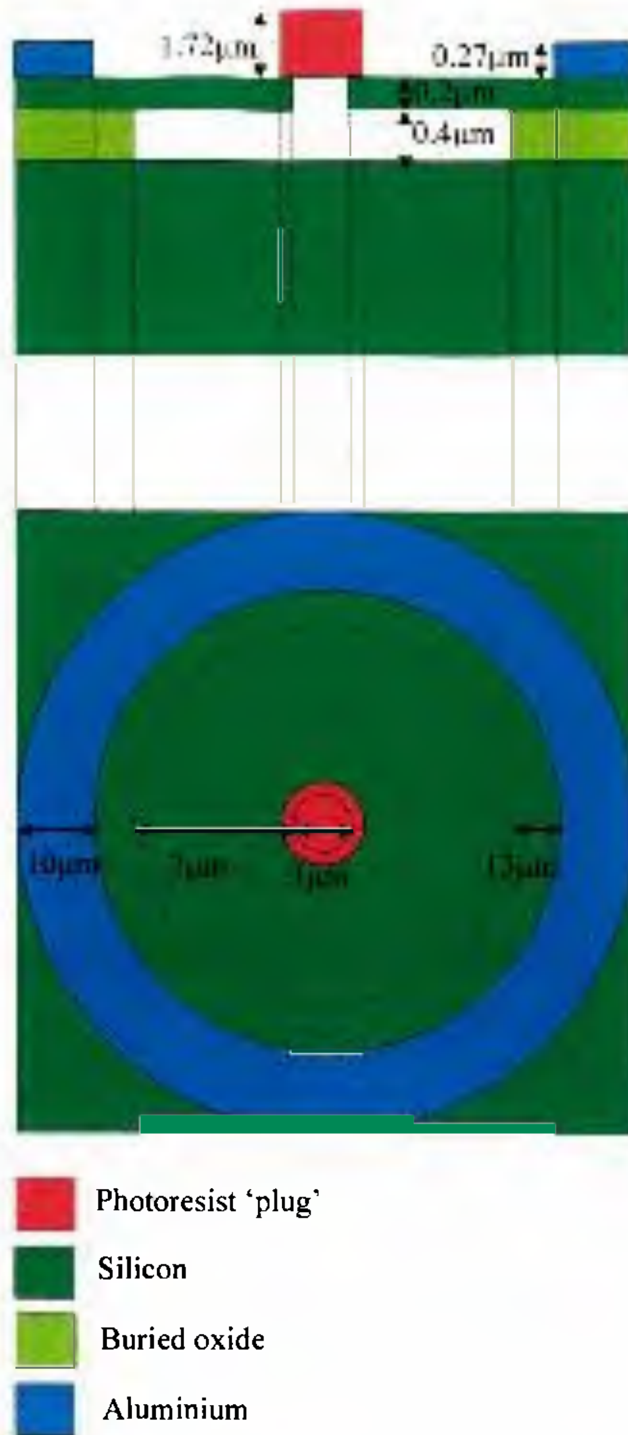


Figure 5.3 Schematic of a single pressure sensing structure

The entire matrix consists of 2500 individual devices and is surrounded by an isolation trench. Some of the benefits of an array design are an increase in fabrication yield, since some non-functional individual devices can be afforded in a functional array sensor, and increased reproducibility of sensor output characteristics [2]. The complete device occupies an area of silicon 3716 µm by 3394 µm. This size is

competitively small (with respect to comparable sensors described in the literature [3]) particularly considering the number of functional elements. This is afforded by the layering of the SIMOX material allowing underetching to form diaphragms with no additional layer deposition or areas of doping. The diaphragm yield, expressed as a percentage of the total number of diaphragms reflects the low amount of diaphragm breakage. On the two samples assessed for yield, using the optical microscope, diaphragms formed from 3 um windows gave yields of 99.8 and 100 %. Diaphragms etched from the larger 5 um windows showed slightly reduced yields of 99.6 and 99.8 %. These yields are very high, however, it has not taken account of undefined silicon windows since this is not a measure of the process reliability but of the standard of photolithography equipment and facilities. The yield in terms of packaged devices which were functional was 83.0 %. Some devices were rejected prior to packaging as a result of poor metallisation which was not suitable for gold ball bonding, these were easily reworked to produce fully functioning devices.

5.2 SIMOX PRESSURE SENSORS, SINGLE AND ARRAY STRUCTURES

The schematic in figure 5.3 clarifies the simple structure of the capacitive diaphragm pressure sensor. Figure 5.4(a) is an optical micrograph of a single novel diaphragm structure fabricated from SIMOX in this work. This consists of a small plugged silicon window with an underetched cavity surrounded by metal which connects to a probe pad. The undercut cavity can be seen as the green area in the micrograph. In this case the green/grey boundary, which defines the perimeter of the cavity is sharp, suggesting a steep wall, and is equidistant around the central etch window demonstrating that time controlled underetching is capable of producing uniform circular diaphragms. The photoresist plug can be seen in the centre of the diaphragm. Figure 5.4(b) shows a SEM micrograph of a similar structure before metallisation and plugging presented in figure 5.4(c), the cavity area is again easily identifiable - in this case as the darker grey region. This micrograph also demonstrates the even nature of the underetching, due to the highly repeatable isotropy displayed by the selected etchant. This allows the formation of a highly symmetric diaphragm which results in good repeatability in the pressure sensor characteristics from device to device.

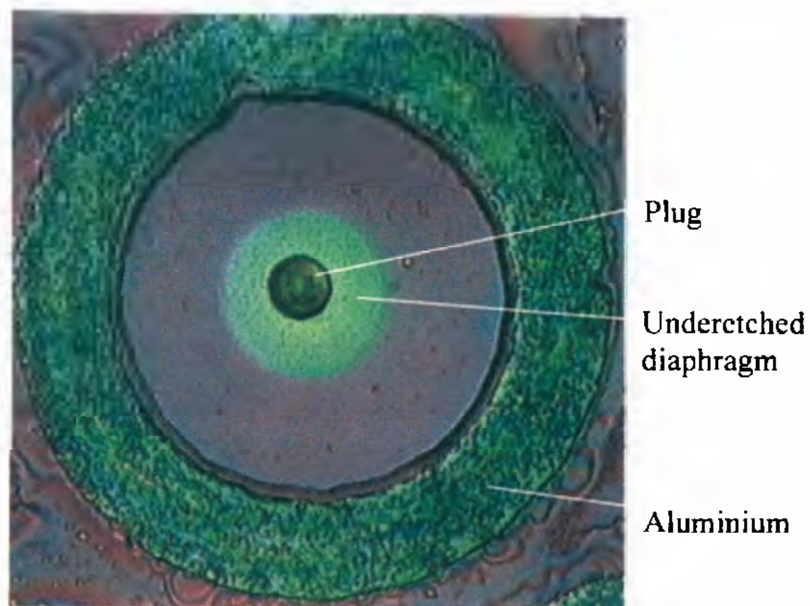


Figure 5.4(a) Optical micrograph of a single, plugged pressure sensing structure

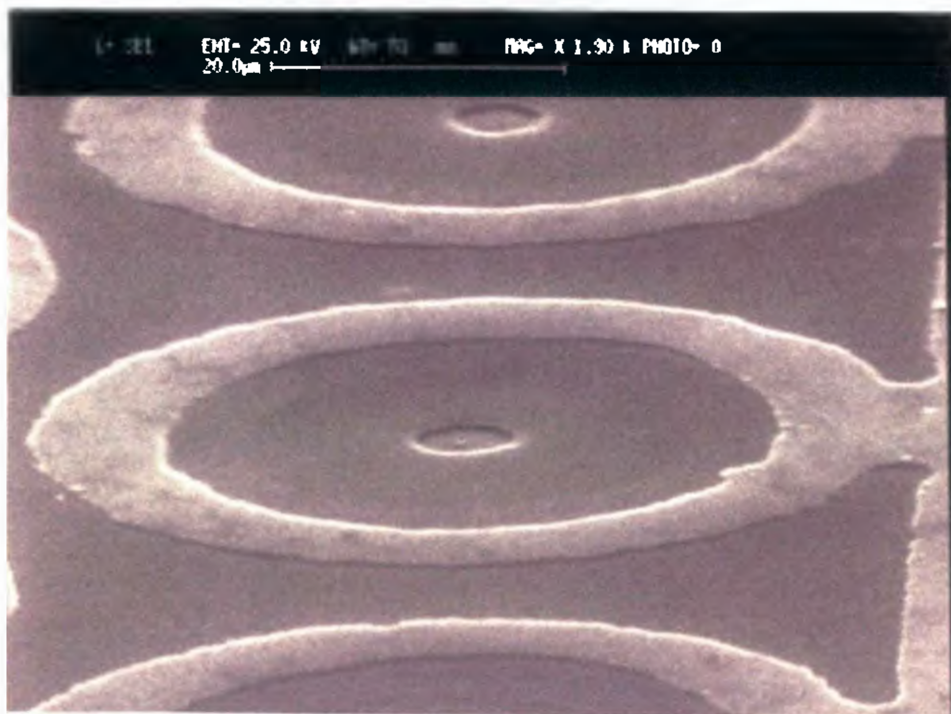


Figure 5.4(b) SEM micrograph of a single, unplugged pressure sensing structure

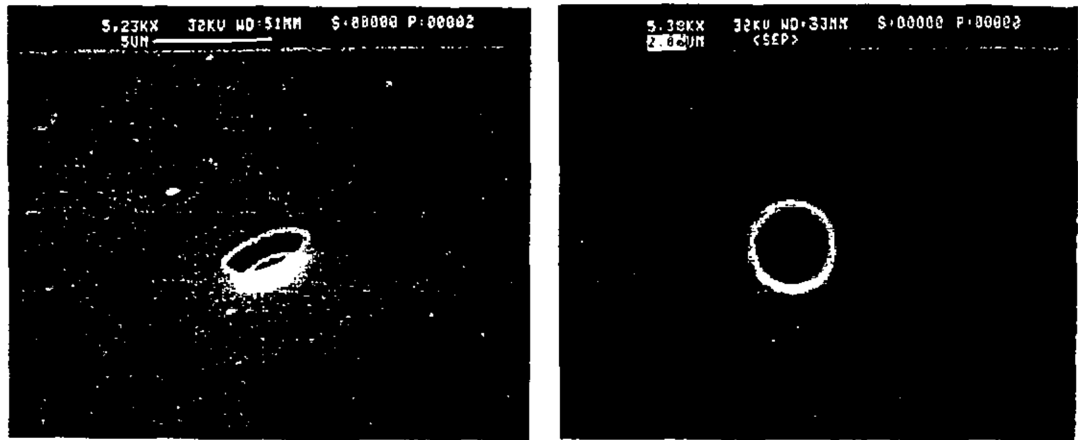


Figure 5.4(c) SEM micrographs of the diaphragm region of the device

Following the successful fabrication of individual sensing diaphragm structures using this novel technology, a functional matrix of diaphragm structures was designed and fabricated to form the full SIMOX capacitive pressure sensor, capable of measurable output. This device consists of a matrix of 2500 diaphragms suspended above 2500 cavities - formed by underetching a region of the buried silicon dioxide layer via 2500 windows etched into the top silicon layer. Around each diaphragm is a metallised ring which contact a metal track to interconnect 50 individual diaphragms. Each of these metal tracks subsequently links to a large metal bond pad running up the side of the chip. Each of the diaphragms is sealed with a photoresist plug. Around the perimeter of the entire matrix and bond pad, an isolation trench has been incorporated into the design in order to minimise parasitic capacitances. The undercut distance was observed to be highly consistent across the matrix resulting in well controlled diaphragm definition. This can be expected to result in identical reaction to pressure from each of the individual structures incorporated in the matrix. In the same way a high degree of repeatability of manufacture and performance would be expected from each subsequent matrix of devices. Figure 5.5 shows a SEM micrograph of a section of an array of unplugged, unmetallised structures fabricated in this work using the developed process sequence. Figure 5.6 is a scanning electron micrograph of a section of an array of plugged structures, with the sample held at a tilt to highlight the plugs.

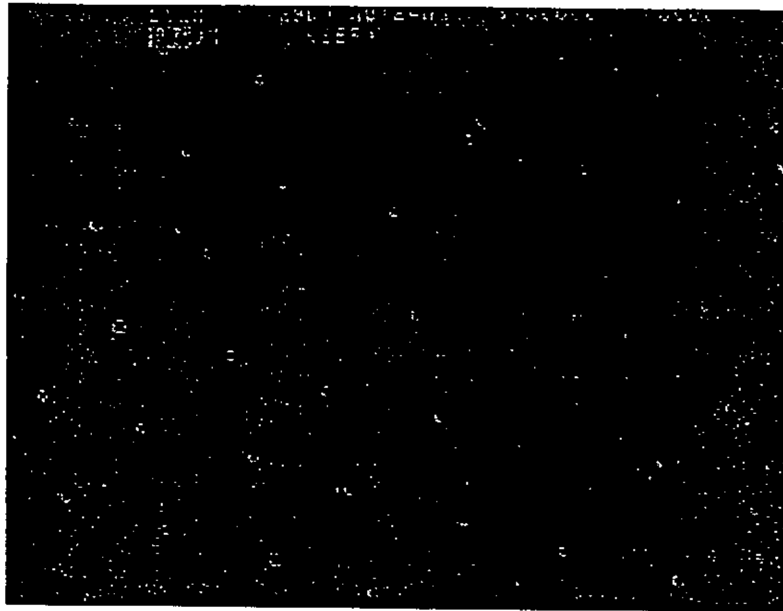


Figure 5.5 SEM micrograph of an array of unplugged diaphragm structures

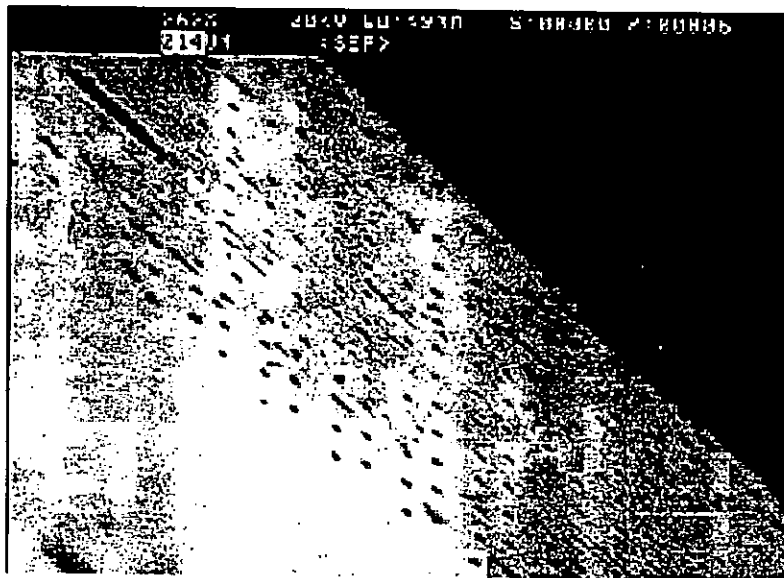


Figure 5.6 SEM micrograph of an array of plugged diaphragm structures

Several sensor devices were made from SIMOX by the process developed in this work. A summary of these devices in terms of extent of fabrication, output and functionality is given in table 5.2.

Device	Etch window size / μm	Undercut / μm	C_o / pF @ 30°C	Plugged	Functionality
Z1	7.0	2.0	-	No	Not tested
SM33	5.5	1.5	423.0	Yes	OK
SM35	9.0	4.0	427.0	Yes	OK
Z4	2.0	7.0	148.5	No	OK
Z5	4.0	7.0	137.0	No	OK
Z6	2.0	7.0	315.0	Yes	OK
Z7	2.0	4.0	120.0	Yes	OK
Z8	8.0	5.0	28.8	Yes	Not functioning
Z9	4.0	7.0	359.2	Yes	OK
Z10	3.0	Not underetched	163.5	-	OK
Z11	5.0	Not underetched	3.2	-	Not functioning

Table 5.2: Summary of fabricated devices

5.3 OVERVIEW OF CRITICAL SENSOR PERFORMANCE PARAMETERS

Although the parameters which affect sensor performance will depend on the particular mechanisms used for sensing, it is possible to indicate which parameters have the largest impact on the operation of sensing devices in general. Table 5.3 below lists several such characteristics, their relevance to our SIMOX capacitive pressure sensor, an indication of their optimum value and usual units of measurement.

Characteristic	Description for pressure sensor	Ideal value	Unit
Sensitivity	Change in capacitance for an applied pressure	High and constant	$pFmmHg^{-1}$
Non-linearity	Capacitance not proportional to pressure	Zero	% FSO

End point non-linearity	Capacitance not proportional to pressure	Zero	% FSO
Working range	Maximum minus minimum capacitance	Infinite	pF
Hysteresis	Systematic error in capacitive - pressure characteristic	Zero	% FSO
Temperature coefficient of offset	Variation in base capacitance due to temperature	Low	% FSO°C^{-1} or ppm°C^{-1}
Non-linearity of temperature sensitivity	Capacitance not proportional to temperature	Zero	% FSO
Hysteresis of temperature sensitivity	Systematic error in capacitive - temperature curve	Zero	% FSO
Temperature coefficient of sensitivity	Variation in capacitance at applied pressure due to temperature	Low and constant over pressure range	% FSO°C^{-1} or ppm°C^{-1}
Repeatability	Change in output under repeated application of identical conditions	Zero	% FSO
Stability	Change in output under continued application of identical conditions	Zero	% FSO
Long term stability	Change in output under continued application of identical conditions over a long time period	Zero	% FSOhour^{-1}
Response time	Time to reach either final value or 90 % final value	Zero - instantaneous response	Seconds
Full scale reading	Calibrated maximum output	Large	pF

Resolution	Ability to measure small pressures	Infinite	mmHg or Pa
Sensitivity drift	Variation in the capacitance /pressure relationship with time	Zero	$pFmmHg^{-1} hour^{-1}$
Baseline drift	Variation in the capacitance at no applied pressure with time	Zero	$pFhour^{-1}$
Ageing	Change in output due to mechanical variation with time	Zero	$pFhour^{-1}$
Interference	Output affected by external conditions	Zero	pF
Noise	Output contains unwanted random signal	Zero	pF

Table 5.3: Critical sensor parameters

Many of the critical parameters of sensors are defined as a percentage of the full scale output. The full-scale output (FSO) is the difference between the maximum and minimum output values. Full scale (FS) is the upper limit of the sensor output in the measurement range [4]. However, for some values, which have been quoted in the literature as a percentage of full scale output, such as temperature coefficients, the definition used for full scale output appears inconsistent. In some cases although the unit of measurement is given as % FSO, if calculation is used to determine the temperature coefficient from data given in a paper, the value quoted appears to have been derived by % FS not % FSO. In some cases, this makes comparison of the SIMOX sensor to other reported devices difficult.

5.4 SET UP FOR PRESSURE SENSOR MEASUREMENT

The performance of pressure sensors fabricated from SIMOX material was evaluated under conditions of applied pressure. The sensor was mounted in a 28 pin DIL

package and then placed in vacuum tubing acting as a pressure chamber. This chamber was connected directly to a nitrogen gas cylinder, which was used to apply the pressure. The temperature of the sensor was controlled by placing the chamber in a temperature controlled water bath. The minimum temperature setting for pressure/capacitance tests was 28 ± 0.5 °C, chosen as slightly above the ambient of the environment and so could be controllably reproduced (the water bath had no cooling ability), this is higher temperature than the temperature generally stated in literature. The maximum temperature which the chamber was raised to was 50.4 °C. A thermocouple placed inside the chamber provided an accurate assessment of the temperature of the sensor. A manometer was positioned between the cylinder and chamber in order to measure the pressure applied by the gas. The chamber also allowed feedthrough connections to be made from the sensor diaphragm and substrate to a Hewlett Packard 4192 LF impedance analyser. The pressure testing system is shown schematically in figure 5.7.

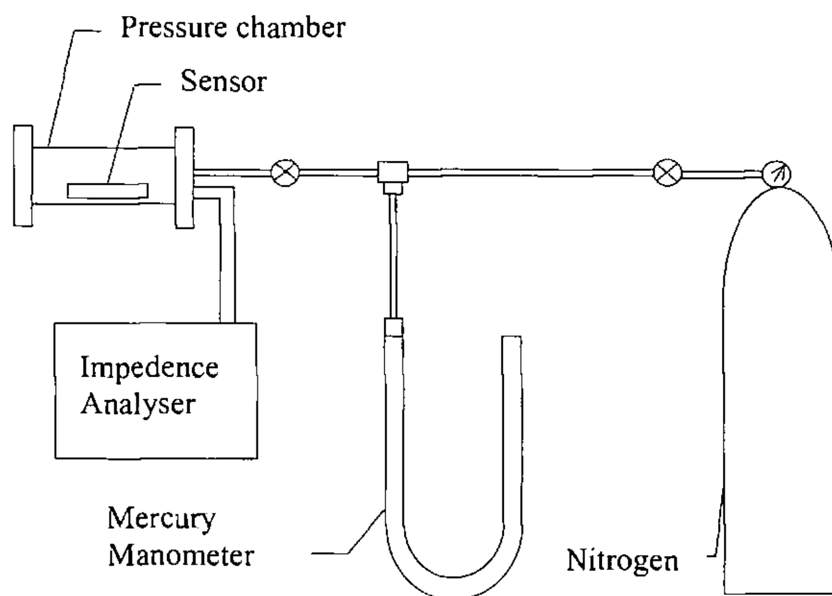


Figure 5.7 Experimental arrangement for pressure sensor measurements

Measurements of the changes in capacitance due to applied pressure were taken over a pressure range of 0 - 500 mmHg. The pressure range for testing, was appropriate for the intended medical applications [5], but was limited by the measuring equipment, in particular the manometer, rather than by the sensor itself. In preparation for making measurements, the system was checked for leaks, the analyser 'warmed up' and

calibrated and manometer levelled. The impedance analyser calibration sequence consisted of an equipment self test and a step to zero the parasitic capacitance resulting from leads etc. The gas pressure was set to an approximate value using the cylinder dial, the valve was then opened to allow the gas to penetrate the chamber. The pressure in the chamber due to the gas was read from the difference in mercury level on either side of the manometer, with an estimated error of ± 0.5 mmHg. The estimated error in capacitance was ± 0.05 pF, where the capacitance is used to interpret an applied pressure this would relate to an approximate error in the calculated applied pressure of ±18.5 mmHg. The capacitive output was displayed on the analyser with the options of data printing or direct saving to disk. Readings of capacitance versus time were taken at various pressures. The pressure was increased or decreased in sequential order and the chamber was not vented between successive applications of pressures. For some of the samples tested the temperature sensitivity of the devices was also examined. The smallest measurable change in capacitance in the test set up used was 0.1 pF which relates to a pressure resolution of 37 mmHg and was largely due to the condition that the change in capacitance was measured on top of a large base capacitance, hence it results from the test method rather than the sensor performance. As discussed elsewhere this problem could be rectified in a number of ways to improve the pressure resolution achievable. For example a MOS switched capacitor readout amplifier circuit has been designed [6] which is particularly suitable for capacitive pressure sensor arrays and can detect capacitance changes of less then 50 fF, while remaining insensitive to temperature variations and stray input capacitance.

5.5 CAPACITANCE-VOLTAGE (C-V) ANALYSIS

C-V analysis of the SIMOX capacitive sensing structures was carried out using a 4192A LF impedance analyser. This allows an insight into device performance under test signals similar to those which would be experienced in actual operation, whilst permitting adjustment of various complimentary parameters. For the majority of the measurements conducted on the SIMOX pressure sensor the impedance analyser was simply used as a tool for measuring the change in capacitance of the diaphragm structure under applied pressure. An introduction to the measurement technique is given below in addition to an overview of the more common C-V profiling mode of

operation, its application to SOI and interpretation of C-V plots. High resolution measurements can be gained in average mode which conducts one measurement per second, alternatively high speed measurements can be performed at 10 measurements per second. The parameter ranges for this equipment are given below:

(i) Frequency 5 Hz - 13 MHz with 1 mHz maximum resolution

(ii) Oscillation 5 mV - 1.1 V rms with 1 mV maximum resolution

(iii) Dc bias V ± 35 V in 10 mV increments

dc bias and frequency can be swept manually in either direction.

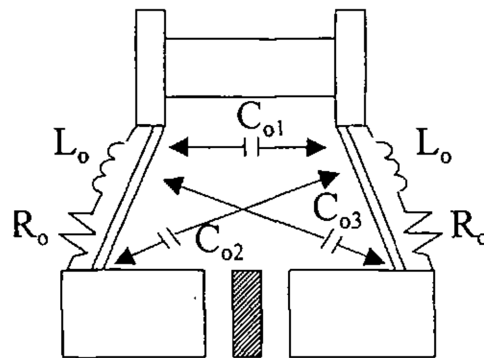
Many of the adjustable parameters can also be swept in steps through a specified range or used at a single value. The apparatus was always allowed a 30 minute warm up prior to use and was housed in an environment which was controlled 23 ± 5 °C and < 95 % humidity at 40 °C.

The equipment initially performs a self test in which six basic functionality tests are conducted and the results displayed as a pass or fail. The accuracy, i.e. number of digits obtainable in a measurement, is dependent upon the oscillation level, measurement frequency and test frequency. A standard is retained for the production of deviation and zero offset conducted to null the effect of test structures with regard residual impedance and stray admittance (this offset adjustment was measured at the frequency to be used in analysis).

The analyser operates by applying an oscillating signal to the device under test, having split the signal by a power splitter. The input signal at one of the arms of the splitter is then compared to the output signal of the device to deduce the effect that the device has had on the signal. Full control of the apparatus was obtained via an external computer. For capacitance measurements the range is from 0.0001 pF to 100 mF with a maximum resolution of 0.1 fF. The equipment will auto range, changing at 200 % FS and 18 % FS or this can be carried out manually. There will generally be a difference in the capacitance measurements taken in parallel and series modes. This is related to the loss factor of the device under test, which is dependent on the series resistance and conductance.

The impedance analyser uses a four terminal pair configuration for connection to the device under test. This arrangement allows high accuracy measurement particularly at

high frequency. The four terminals are high current and potential and low impedance and potential. The current terminals allow the measurement signal to flow through the sample and the potential allow detection of the voltage drop across the sample. This system requires the use of a special test fixture which allows the magnetic fields of the leads to be cancelled, reducing errors due to inductance between leads and minimising any stray capacitances, as shown in diagram 5.8. However, the four terminal pair must be converted to two terminal near to the sample and stray capacitances appear at this point as the sample is connected to the test fixture. These errors cannot be corrected by zero offset adjustment as this is specific to the device under test.



where

C = capacitance

L = impedance

R = resistance

Figure 5.8 The parasitic effects when connecting device under test to test fixture (taken from 4192A LF Impedance analyser operation and service manual)

Capacitive voltage testing is the most frequently used method of electrical characterisation. It allows accurate, fast and non-destructive assessment of a semiconductor material quality. C-V analysis gives a measure of the electrically active net impurity concentration, oxide and interface characteristics and deep

impurity levels can also be studied. Further analysis and/or equipment can be added to the basic C-V set up to allow determination of other parameters such as work function and oxide charge. C-V testing is carried out by the application of a dc electric field, typically between the silicon substrate and a contact made on silicon dioxide. A region which is depleted of carriers is then formed. The differential capacitance of the silicon space charge region is then measured by superimposing a small ac voltage on the dc bias. By application of the expression for a parallel plate capacitor, the capacitance of the depletion region can be approximately determined and its width and dopant level deduced. The depletion region can extend laterally well beyond the electrode, effectively increasing the junction area [7], this can result in significant errors.

Analysis results in a C-V curve which can be assessed by comparison with an ideal curve, such as that shown in figure 5.9 for a p-type semiconductor. Such a curve is obtained if:

(i) The insulator behaves like a vacuum but with a different dielectric constant.

(ii) The difference in work function between the two capacitor plates is zero.

(iii) No surface charge exists.

(iv) The boundary of the depletion region is sharp and there is no leakage.

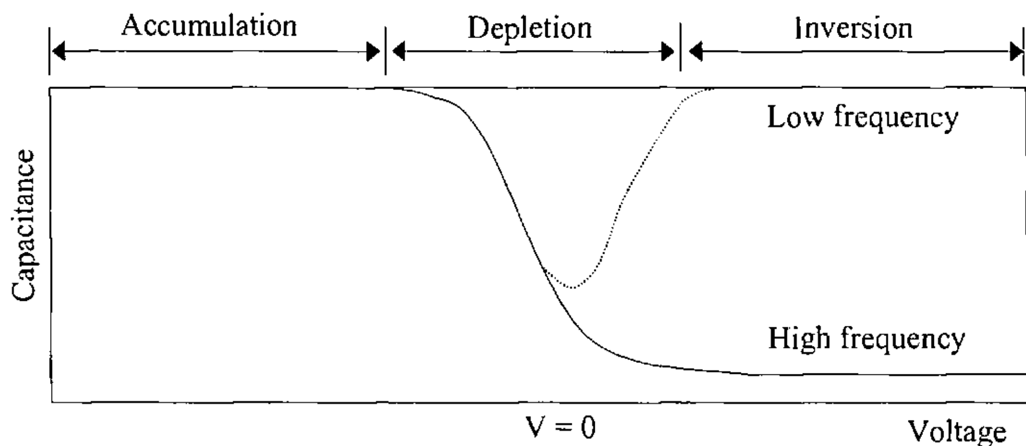


Figure 5.9 Ideal CV curve for p-type silicon

The ideal curve for a p-type semiconductor can be divided into several regions. Where V < 0 the material is in accumulation i.e. there is an accumulation of majority carriers at the surface because the majority carriers are attracted to the interface by the gate voltage. A thin highly concentrated charge layer is formed which acts as a capacitor plate, the resultant capacitance is then dependent on the geometry and thickness of the insulator, in accumulation, the depletion depth is zero.

When the applied DC voltage, V is zero, the energy bands are flat out to the surface, this is known as flat band condition.

Where V > 0, majority carriers are repelled from the surface leaving ionised impurities uncompensated. In this region the capacitance changes rapidly with voltage, charges in the semiconductor material are repelled by the gate bias voltage creating a depletion region under the gate. This acts as an insulator separating the effective capacitor plates of the gate metal and substrate. Analysis of the curve in this region can yield the doping concentration and depth into the semiconductor. Heavy doping can be recognised by a gradual depletion slope, while light doping gives a steep slope. Valid doping profiles can only be deduced when the device is in depletion. Where V has a sufficiently large positive value, the density of minority carriers at the surface can become greater than that of majority carriers in the bulk. This situation is called inversion and the decreasing capacitance during depletion is limited by the onset of this condition. Inversion occurs as the voltage across the semiconductor becomes sufficient to attract minority carriers away from the semiconductor, toward the interface. This results in an inversion layer at the interface which incorporates more minority than majority carriers, therefore at the surface, the conductivity type is inverted, for example from p-type to n-type. The capacitance due to inversion is dependant on the area of the gate and is effectively the capacitance of two plates separated by the oxide layer. The important difference between this and accumulation is that the charges responsible for the capacitance are the slow moving minority carriers. The conditions of accumulation, depletion and inversion, described above, correspond to the structure situations shown in figure 5.10

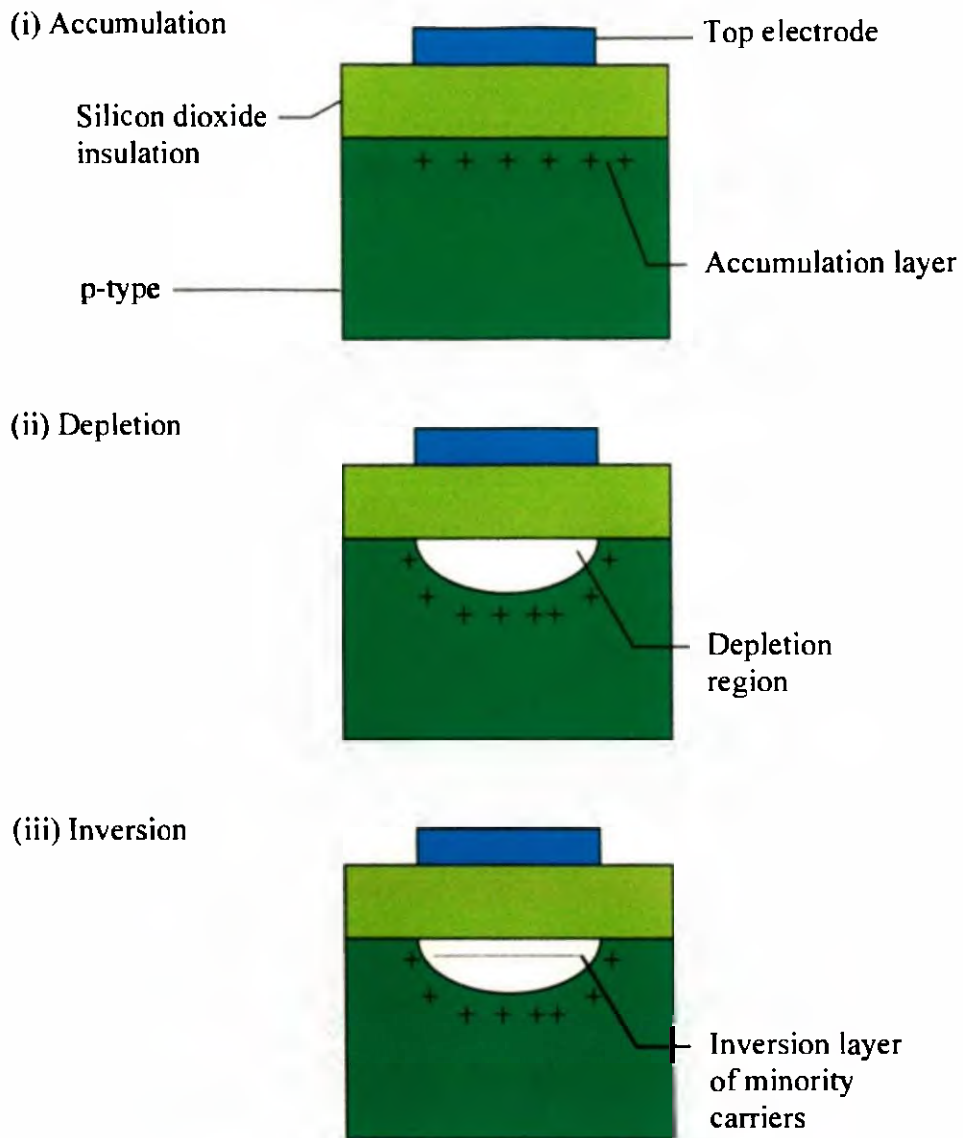


Figure 5.10 The C-V phases within the structure

In addition to the bulk silicon charge which depends on the device bias, the total capacitance is also due to fixed oxide, mobile ionic, oxide trapped and interface trapped charges. If loss mechanisms are neglected, experimental curves can be compared to the ideal curve to ascertain material properties. If (referring back to the conditions for an ideal curve) (ii) is not the case, the curve will be shifted along the V axis, by the difference in work function between the contact and semiconductor, but without distortion. If (iii) is not the case, there is an additional translation along the V axis, which is a measure of charge in the surface states.

If interface states are present which are dc but not ac dependant the C-V curve will be distorted and displaced along the V axis, however, the ratio of minimum to maximum capacitance will remain unchanged. If dc and ac dependent interface states are present the curve will be distorted and displaced and the ratio of capacitance changed, depending on the energy and spatial distribution of the interface states. If the curve is shifted (due to any of these effects), to the left compared to the ideal curve, the interface charge is positive and donor states are present, a shift to the right indicates that acceptor states are present. High frequency C-V curves are not symmetric in shape and their curvature is related to the conductivity type in the surface space charge region, the slope is negative for p-type materials such as the SIMOX material employed for sensor fabrication.

The limitations of C-V characterisation are that only surface potential i.e. charge in the space charge region can be measured. The series combination of the semiconductor and insulator capacitance is limited by the fact that the latter allows only partial examination of the semiconductor capacitance. If the semiconductor capacitance is much larger than the insulator capacitance it can no longer be measured, restricting the region of forbidden gap which can be examined. The inversion layer capacitance displays a dependence on the bias and frequency which is complex due to several minority carrier transfer processes, therefore the inversion region of an experimental C-V curve may not vary from the ideal simply due to surface states. Non-uniform spatial distribution of surface states can lead to curve ambiguity in comparison of experiment with theory, the oxide capacitance and doping of space charge region must be accurately known, since these form a reference point for calculations. Furthermore, the maximum depth of C-V analysis is limited by the onset of avalanche breakdown. For silicon the maximum sustainable field is $\sim 4 \times 10^3$ Vcm^{-1} i.e. 2×10^{12} charge cm^{-2} in the depletion region.

In some cases a dip occurs in the high frequency C-V curve at the onset of inversion, giving the false impression of a decrease in depletion width. A common cause of this is insufficiently high frequency. High and low frequency curves should saturate at the same capacitance in accumulation. If this is not the case, this indicates the presence of a series impedance which could be due to cables and probes, high resistivity substrates, bad backside contact or parasitic p-n junctions. Random noise may cause the two curves to overlap, this is an indication of low resolution. Low frequency

curves should be flat with no peaks or tilts. If this is not the case oxide leakage maybe occurring. Less commonly, broad peaks may be due to mobile ionic charge drift and narrow peaks due to a permanent inversion layer.

C-V analysis can provide much information about the buried oxide properties in SOI material, however, the interpretation of C-V data is difficult on SOI due to the number of interfaces, thin closely spaced films, large parasitics and series resistances [8]. Metal layers can be deposited on the top silicon surface to reduce the series resistance of the contact. Using the BOX as capacitor dielectric MOS C-V analysis has been extended to model SOI as two silicon/silicon dioxide interfaces, giving the ability to ascertain parameters such as doping concentration, oxide thickness, interface trap and oxygen charge density for each interface by fitting the output to a theoretical curve. The minority carrier generation lifetime gives a good indication of the material quality. Assuming neither minority carriers or interface traps contribute to the measured capacitance, the SOI capacitance (C_T) can be represented by the equation below:

$$\frac{1}{C_T} = \frac{1}{C_{Bulk\,Si}} + \frac{1}{C_{Ox}} + \frac{1}{C_{Top\,Si}} \qquad (5.1)$$

Interface traps are defects or impurities, resulting from processing or damage, which are located around the interface. They can be charged and discharged which means that they act as small additions to the device capacitance. However, traps may respond slowly to changes in gate voltage therefore they can be evident in the low frequency curve but not the high frequency. With the substrate grounded, a positive bias has been shown to deplete the epi-oxide interface, and a negative bias depletes the substrate-oxide. Results have demonstrated that higher temperature anneals cause a reduction in the density of fixed oxide charge and interface traps at both interfaces but the density of fixed oxide charge at the top silicon/BOX interface is much larger than the interface trap density or density of fixed oxide charge at the substrate/BOX interface. A definite dependency of the defect density at the top silicon/BOX interface on processing history, in material which was initially identical, has also been revealed (the substrate/BOX interface is thought to be less sensitive to processing) [9]. The SOI CV profile displays a strong dependence on the total silicon thickness. The origin of traps has been attributed to the introduction of metal impurities during oxygen

implantation [10], which interact with defects at the top silicon/BOX interface. Due to the positive charge in the BOX, lightly doped p-type substrates are easily inverted and charge can diffuse to adjacent areas under the pad causing the substrate capacitance to change. This explains a 'dip' typically seen in SOI C-V profiles [11].

I-V has also been used for the evaluation of SOI, this gives information on mobility, threshold voltage, sub-threshold swing and leakage current from the front and back interfaces [8]. Point contact I-V measurement on single implant SIMOX has revealed self-healing behaviour, which was considered to be due to the presence of silicon clusters which explosively evaporate to fill weak spots in the oxide. This could occur many times within a test and is evidenced by a series of voltage jumps in the characteristics. Some single implant material has shown low oxide reliability with parameters indicative of connection paths through the oxide [12].

In the current work, prior to any pressure sensitivity measurements, the C-V characteristics of a typical SIMOX sensor with no applied pressure were first studied and optimised. The typical capacitive output of a sensor through a voltage sweep (-10 V to +10 V) under conditions of no applied pressure is shown in figure 5.11.

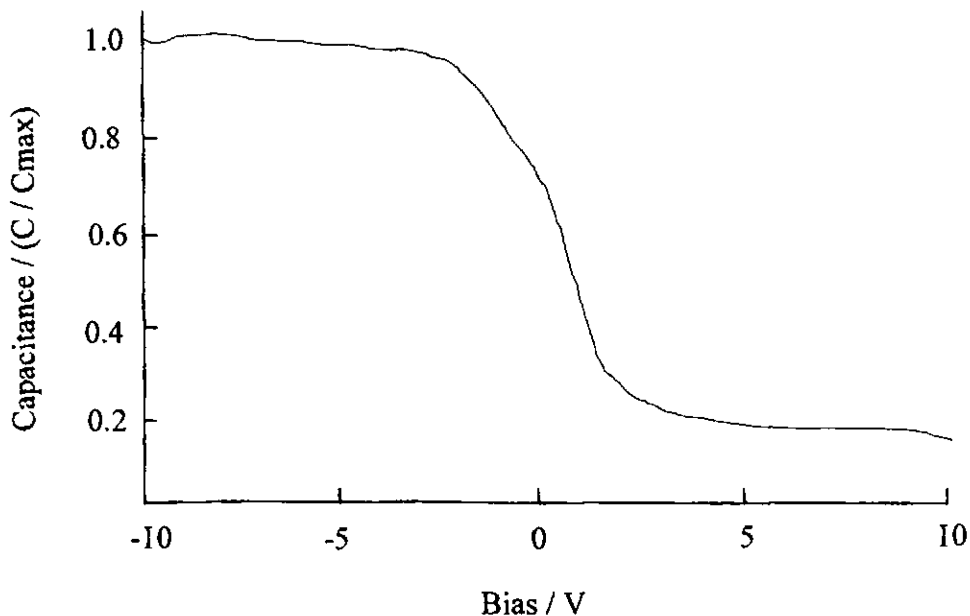


Figure 5.11 A typical SIMOX sensor C-V curve

Several points were apparent from curves taken during the C-V measurements:

(i) At the boundary between the inversion and depletion sections of the curve, there is a dip. This may be due to either insufficiently high frequency or changes in the substrate capacitance due to charge diffusion which can occur in SOI material. The former could be the cause since a larger dip was seen in characteristics measured at a lower frequency.

(ii) The slope of the depletion region is steep – this was expected as it indicates low levels of doping, which was the case for the material used to fabricate the sensors.

(iii) The accumulation region of the graph has a tilt to it, this indicates that some oxide leakage maybe ocurring, i.e. current is passing through the oxide layer between substrate and top silicon layers. This was less evident on measurements made on early fabrications of single structures, which may indicate that the differences in processing carried out for the array, particularly the application and sintering of metal, initiate some degree of oxide breakdown. Alternatively the material used for the early structures was from a different supply batch of SIMOX and may have differed in initial buried oxide quality.

(iv) The C-V characteristics measured, for the same device, at different frequencies displayed a difference in the value of maximum capacitance. Although the measurements made in this work would not be considered as high and low frequency curves, this small offset may indicate the presence of a difference in the value of oxide capacitance between the true high and low frequency curves. When these differences occur they can be accounted for in several ways. There may be a series impedance, caused for example by the cables, contacts or a parasitic junction. Traps maybe present in the material which will only be evident at low frequency while in the high frequency test, the frequency may be so large that there is not sufficient time for the minority charge carriers to react.

(v) The experimental curve, when compared to an ideal curve, is shifted slightly along the voltage axis, this can also signify several different factors. The two capacitance plates may have a different work function, or surface charge may exist, or there may be interface states present, The later is only dc dependant and if, as in this case, the offset is to the left, this indicates that these charges are positive.

Following offset adjustment, measurements of the sensor capacitance under applied pressure were conducted at a bias of 0 V. A series of experiments were carried out to determine the parameter set producing a curve of the form closest to the ideal C-V output. The impedance analyser was then set up accordingly with an oscillation (frequency) period of 30 ms and measurement frequency of 100 kHz. Measurements were carried out with the instrument in averaging mode to ensure the highest measurement resolution, accuracy and repeatability. In this mode the final capacitance value is the average of seven seperate measurements.

In separate experiments, the analyser was set up to measure capacitance under conditions of fixed bias while stepping in time. The time was correlated to the application and release of pressure, or variations in temperature, depending on the sensor characteristic being monitored.

5.6 RESULTS OF PRESSURE TESTING OF SIMOX SENSOR

Prior to sealing of the SIMOX sensor access holes, some very simple capacitance tests were carried out to confirm sensor operation. In these tests deflection of the sensor diaphragms was attempted using a jet of nitrogen gas supplied through a fine nozzle.

An unsealed pressure sensor was mounted on the chuck of the HP 4145 and C-V curves taken with and without the stream of nitrogen applied to the device. The application of nitrogen was initiated at a bias of 3 V (scanning in voltage from positive to negative). The results are shown in figures 5.12 and 5.13 and show that a sudden change in capacitance occurred at 3 V, when the nitrogen stream was applied to the device. As a control an unetched SIMOX sample was subjected to the same test to confirm that the observed capacitance change was not due to an effect other than diaphragm deflection, such as nitrogen cooling or movement of probes due to the gas stream, no significant change in capacitance was observed for this control.

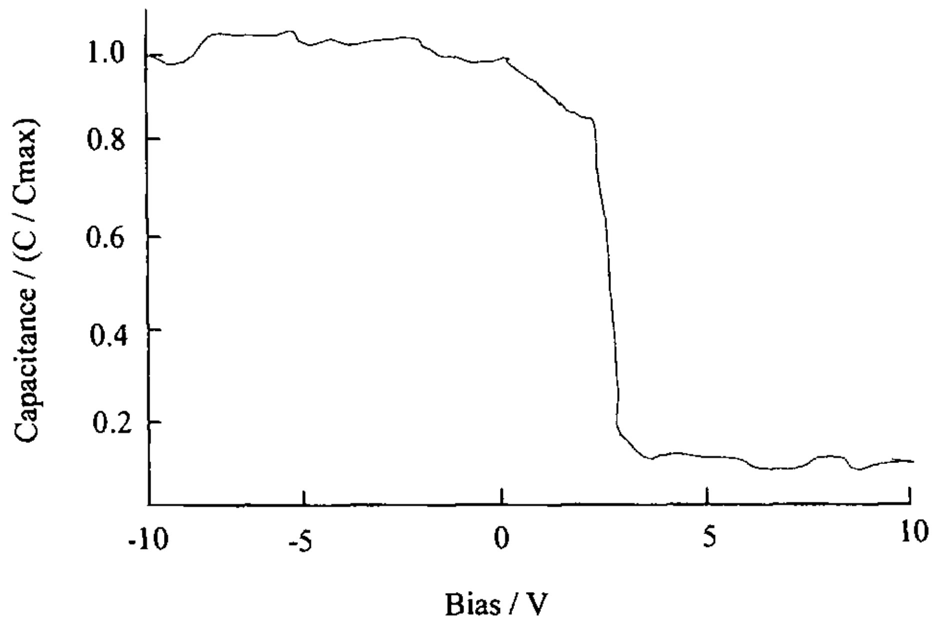


Figure 5.12 Application of nitrogen to a single unsealed pressure sensor

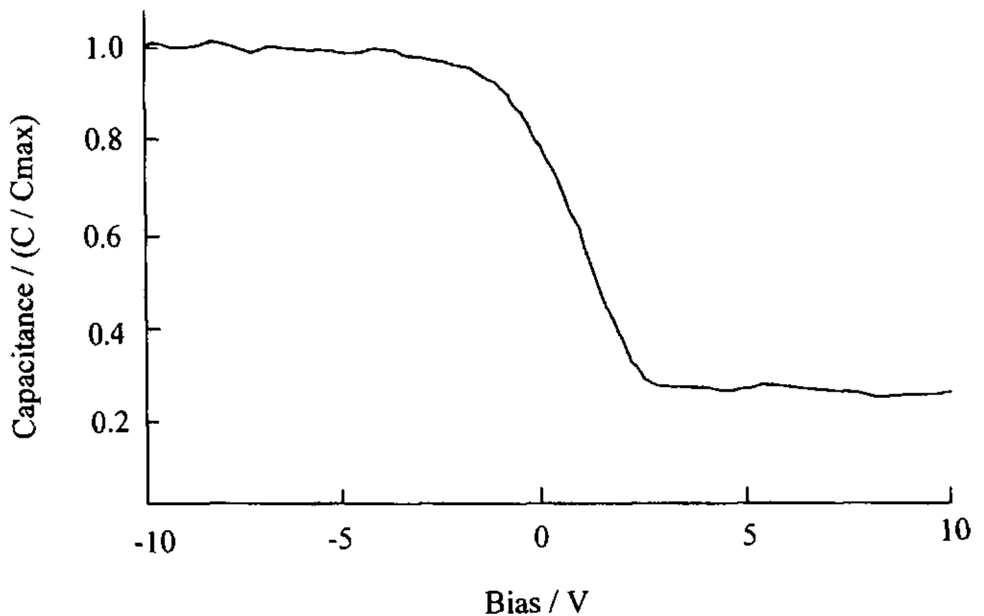


Figure 5.13 The same unsealed single pressure sensor without the application of nitrogen

Following these simple tests, the set-up described in figure 5.7 was arranged. It was confirmed that the system suffered no significant pressure leakage by measuring its ability to hold a pressure overnight. With the sample outside the chamber the effect of the test equipment on the base capacitance was assessed. With just the package and

immediate wiring attached as in figure 5.14, the output capacitance was 3.16 pF, with just the feed through plate and immediate wires as in figure 5.15, the capacitance was 2.14 pF. In combination along with the surrounding chamber as in the full test set up, the capacitance was 3.24 pF. A sealed device was then initially tested in the pressure chamber and a change of capacitance due to the application of pressure was confirmed. This was followed by testing of the ability of the device to hold a deflection for an extended period of time, i.e. assessment of the quality of the diaphragm sealing method.

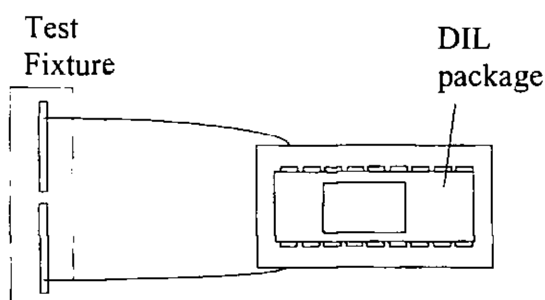


Figure 5.14 Sensor and immediate wires only

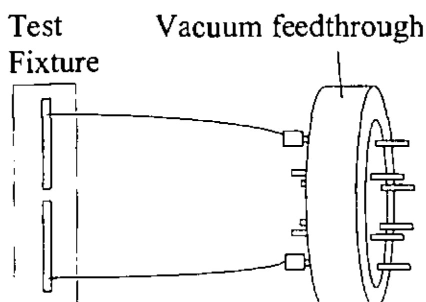


Figure 5.15 Feed through plate and immediate wires only

A sensor was mounted in the chamber and a pressure applied which resulted in an immediate rise in capacitance of 0.5 pF. The system was left in this state overnight. During this test the chamber temperature was not held at a stable value therefore there

was fluctuation in the output capacitance value due to variations in room temperature. After 15 hours, the chamber was vented, there was an immediate drop in capacitance of 0.4 pF. The small difference of 0.1 pF between the two values is within experimental errors for the capacitance measurement. The results are presented in figure 5.16 in which the time axis is not to scale. The increase in capacitance as pressure was initially applied occurred over a period of 75 seconds, by comparison the dotted line over which period the sensor retained its response represents approximately 15 hours. The results of these investigations confirmed that the polymer diaphragm seals were functioning properly and not leaking. Therefore the diaphragms had been successfully designed and fabricated and allowed the sensor to retain a reaction to pressure. Following successful demonstration of the SIMOX sensor operation, a range of further characterisation measurements were carried out, these are described in the following pages.

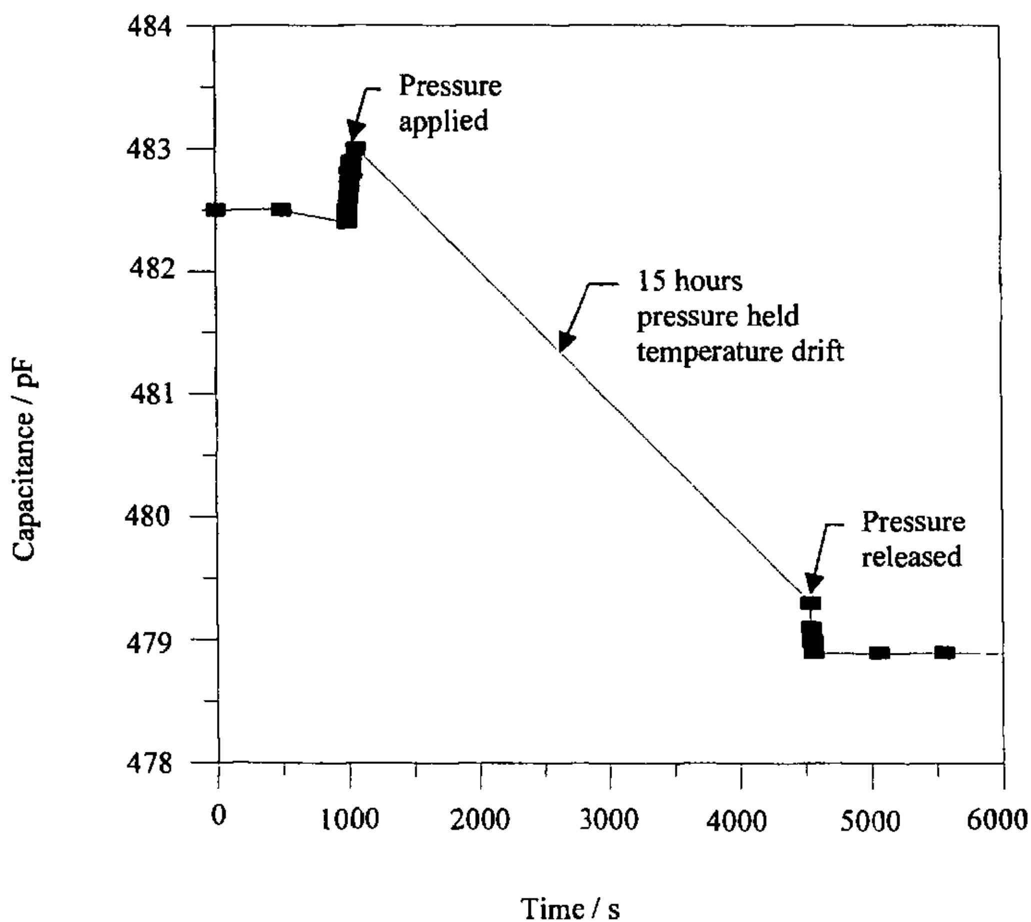


Figure 5.16 Release of pressure after holding chamber pressurised overnight

The most fundamental operational parameter for sensors in general is sensitivity. This indicates the size of the output measurement signal in response to the applied parameter to be measured. It therefore determines what circuitry is required and the limits for measurement. In the case of the SIMOX pressure sensor, sensitivity is interpreted as the change in output capacitance per unit change in applied pressure. The output of a capacitive pressure sensor is inherently non-linear for pressure versus capacitance, due to the relationship between capacitance (C) and diaphragm deflection (w) given in equation 5.2.

$$C \propto \frac{1}{w} \tag{5.2}$$

In general for this type of sensor the pressure-capacitance characteristic is of the form shown in figure 5.17

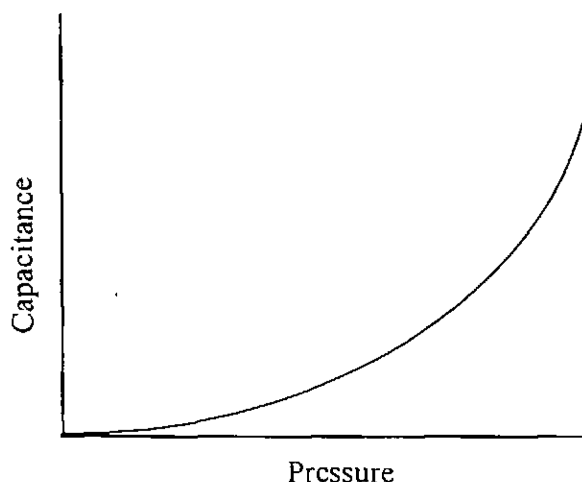


Figure 5.17 A 'typical' pressure-capacitance characteristic

In the case of the SIMOX pressure sensor fabricated in this work, the pressure-capacitance characteristic was typically found to differ from this 'ideal' case as shown in the plot in figure 5.18.

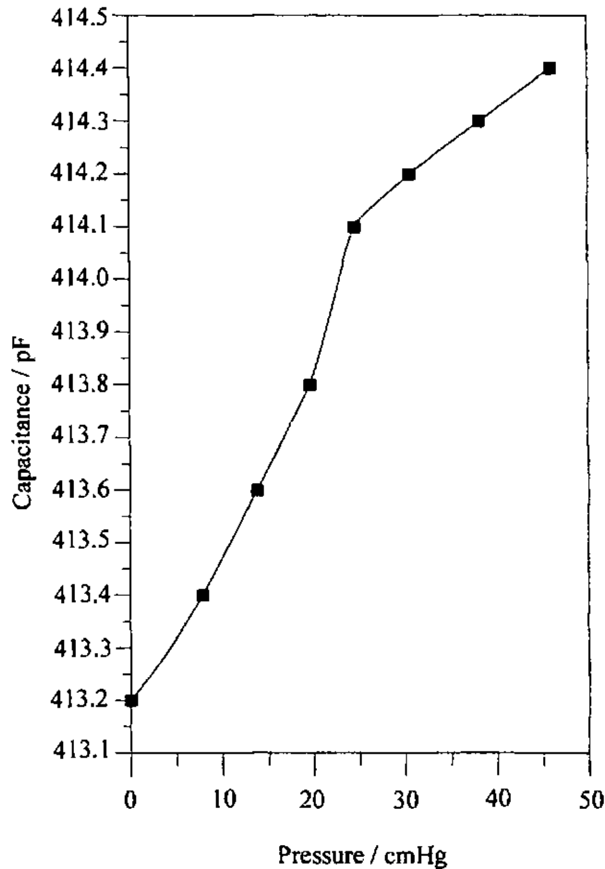


Figure 5.18 The pressure-capacitance characteristic of a typical sensor fabricated from SIMOX

There are several points to note about the plot in figure 5.18. Initially the capacitance tends to rise in the 'ideal' manner as would be expected. At an applied pressure of ~ 22 cmHg, the gradient of the characteristic changes, displaying a reduction in the sensitivity. Each of the devices tested exhibited a similar shape characteristic and in each case the change in gradient was seen at approximately the same applied pressure. For some devices, as shown in figure 5.18, there is an intermediate region, connecting these two distinct sections of the curve. In this intermediate region a sudden rise in capacitance is observed, however, this was not obvious on all the characteristics, possibly due the separation of the data points. The mean device sensitivity for all of the sealed devices which were fabricated was determined as 0.0027 $pFmmHg^{-1}$ and the maximum sensitivity observed was 0.0058 $pFmmHg^{-1}$.

There are several explanations for the 'non-ideal' shape of the characteristic:

(i) It has been shown [5] that the gradient of a sensor characteristic can be dramatically reduced by gas (air) trapped inside the cavity during the sealing process. The relationship which determines the force (F) operating against the pressure applied to the diaphragm due to the trapped gas is dependent on the volume (V) of the gas as described by equation 5.3.

$$F \propto \frac{1}{V} \tag{5.3}$$

As the diaphragm deflects, the volume of the gas is reduced and therefore its opposing force is increased. Since the relationship in (5.3) is inversely proportional it could be expected that rather than this effect being present throughout the pressure-capacitance curve, it only becomes obvious at high applied pressures where a small change in volume relates to a large increase in the opposing force. This would result in a smaller deflection and therefore a smaller capacitance change than expected for a particular applied pressure which could account for the reduced sensitivity seen in the characteristic in figure 5.18.

(ii) A second effect which affects the shape of the pressure-capacitance curve is contact of the diaphragm with the substrate under the action of the applied pressure. The gradient of the curve has been shown to reduce [2] at the pressure which induces substrate contact and in one case [13], this contact is used to determine the onset of the measurement range to utilise the increase in linearity which results. In the case of the SIMOX pressure sensor, calculation (see chapter 3) suggested that at the maximum applied pressure of 500 mmHg the diaphragm deflection will be less than half of the cavity height. However, not only is this a simple approximation but also the behaviour of the photoresist in forming the plug is not known - it could be pulled down the etch window by capillary action during spinning to form a slight meniscus below the level of the diaphragm thus reducing the effective cavity height. This would allow premature contact of the diaphragm with the substrate resulting in a sudden relaxation in device sensitivity.

(iii) A further explanation which accounts for all three regions of the characteristic shown in figure 5.18 is a sudden change in diaphragm profile. A very similar capacitance-pressure curve to that shown in figure 5.18 has been reported [14]

for a polysilicon diaphragm, this is shown in figure 5.19. This curve shape has been accounted for by considering a deflection in the fabricated diaphragm at no applied pressure due to residual stress. Although single crystal silicon would be expected to display low residual stress, again, the effect of the photoresist plug is not known, it could swell after formation. As a pressure is applied the diaphragm displays a deflection which follows the expected plot. However, at a critical pressure the shape of the diaphragm suddenly 'flips' from bulging upward to downward in the centre. Associated with this transition is a sudden increase in the capacitance as the gap between the plates is rapidly reduced. Following this, the capacitance continues to rise but at a slower rate than the initial region. In the case of the 1 μm thick polysilicon diaphragm [31] this behaviour has been confirmed by the authors using phase measurement interferometry to observe the deflecting diaphragm.

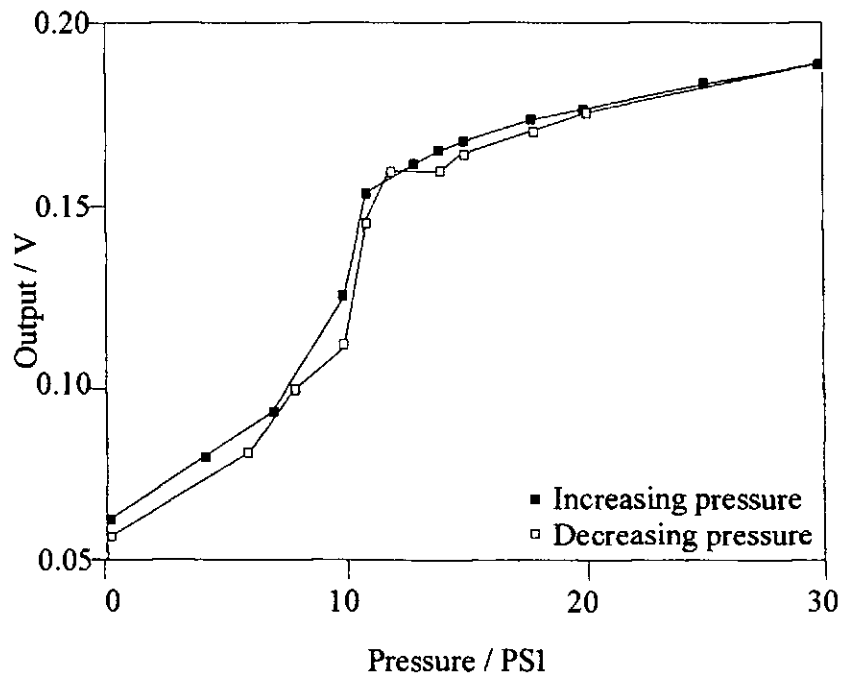


Figure 5.19 Characteristic from polysilicon capacitive pressure sensor [14]

In general, the linearity of a capacitive pressure sensor output is poor, however a high linearity of output is desirable since it allows easy extrapolation and calibration of

sensor characteristics. The non-linearity for a sensor is defined as the difference between a curved plot and a linear fit line through the same set of data points on the capacitance-pressure curve. For the SIMOX sensor this non-linearity has been determined as ~ 0.016 % FS from the sensitivity characteristic which is plotted in figure 5.20. This is a small value for non-linearity compared to similar sensing devices (see table 5.4)

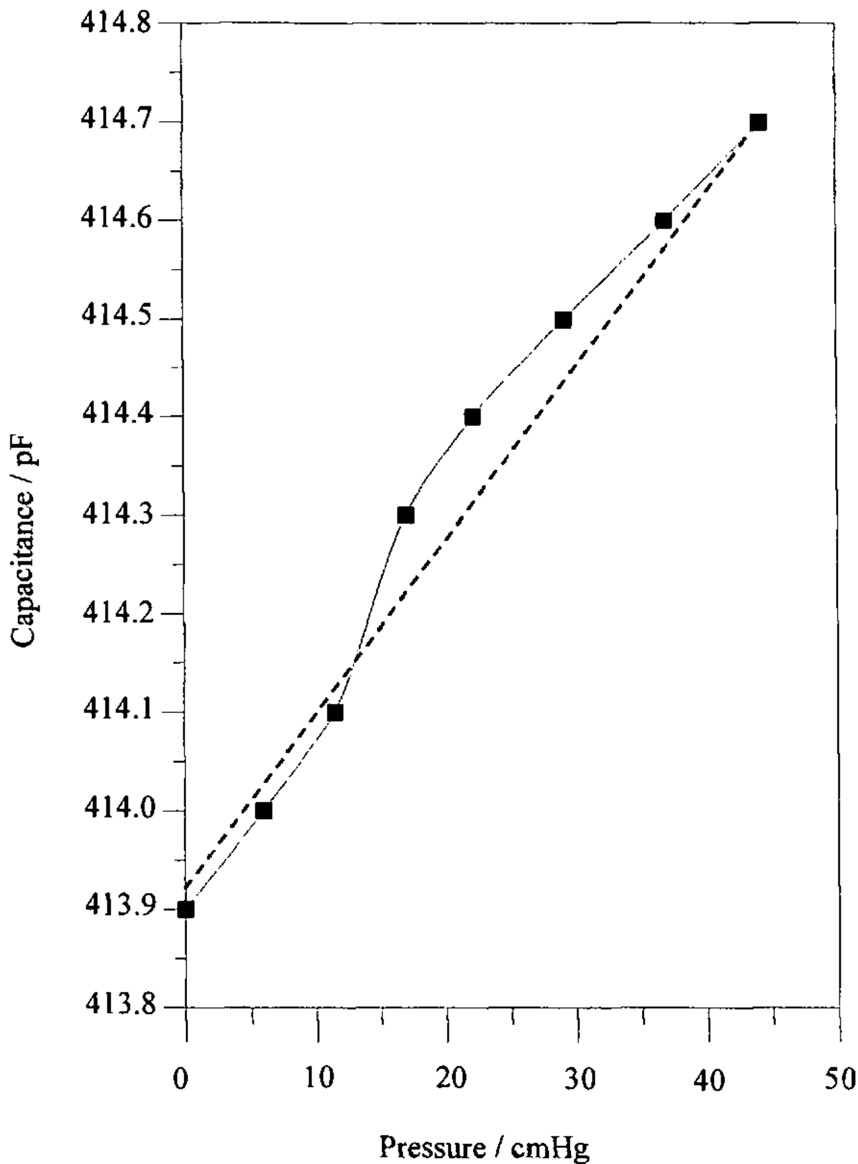


Figure 5.20 Comparison of linear and curve data fits for the capacitance/pressure response of a sensor

The capacitance under conditions of increasing and decreasing pressure was measured in order to allow an estimate of the sensor hysteresis. This is generally expressed as % FSO. Hysteresis has been defined as the maximum difference in output at any value within the measurement range when the value is approached with increasing then decreasing values [4]. Elastic hysteresis is implied by heat generation and fatigue phenomena in repeated cycles of stress [15]. With application to diaphragms which undergo deflection, where the elastic limit is not exceeded, hysteresis results from the dissipation of energy. This is related to the existence of defects such as point defects, line defects, dislocations and grain boundaries. As the diaphragm deflects the defects move and in doing so absorb energy and produce heat. Hence the higher the number of defects and grain boundaries, the higher the hysteresis. It can be seen that for a sensor this is highly dependant on the diaphragm material and in the case of the SIMOX sensor tested in this work low hysteresis would be expected due to the intrinsic low defect density of the top single crystal silicon layer. There may be some increase over bulk silicon caused by defects from the oxygen implantation which have not been removed in the annealing process. However, this increase would be expected to be small compared to alternative materials used in diaphragm fabrication such as polysilicon, silicon dioxide and metals which have a high number of grain boundaries and higher defect levels than silicon. Higher hysteresis also results where the diaphragm is fabricated from layers of materials with different elasticity such as the silicon nitride/aluminium diaphragm of Lysko [16]. Hysteresis is further affected by diaphragm design and operation. In the case of a diaphragm which contacts the substrate above a particular applied pressure, an increase in hysteresis has been observed [2] and has been attributed to friction between the two contacting surfaces.

Considering the small value for non-linearity, it is justified to determine the sensor hysteresis from linear plots of the increasing and decreasing pressure measurements. The experimental assessment of hysteresis was carried out at 28 °C ± 0.5 °C, on a device with 7 μm undercut and a 4 μm plugged window. The data is plotted in figure 5.21, it can be seen that the hysteresis is fully accountable for by the error bars i.e. within the accuracy of the experimental measurements there is no hysteresis.

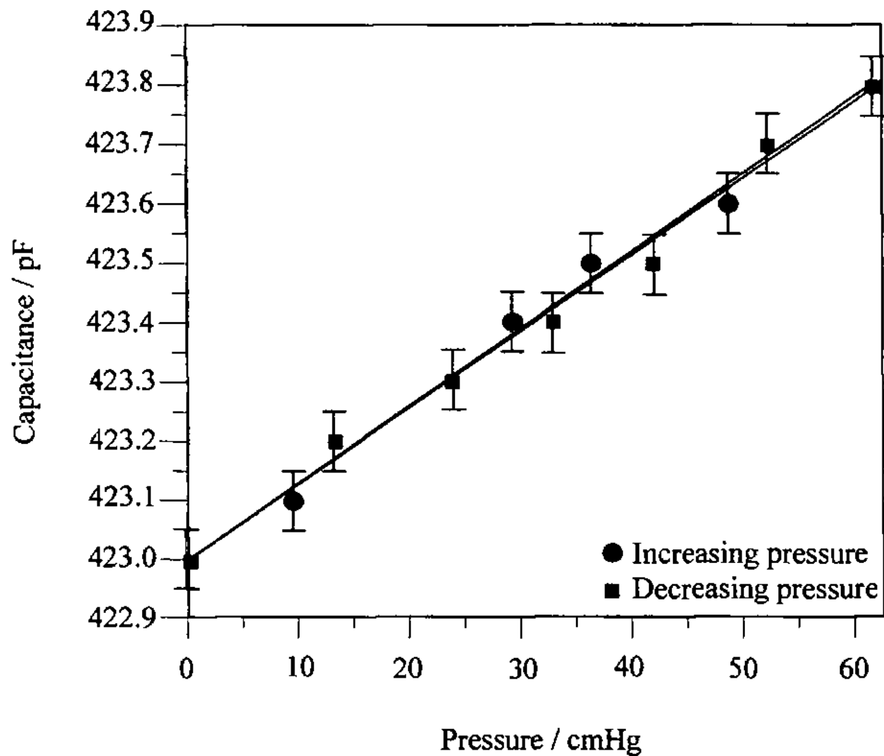


Figure 5.21 Linear plot evaluation of sensor hysteresis.

The effect that temperature has on a pressure sensor is vitally important, it is significant in capacitive sensors and even more so in piezoresistive sensors. An indication of the effect of temperature is given by the temperature coefficient of offset (TCO) and temperature coefficient of sensitivity (TCS). The former is the fractional change in C_0 (the capacitance under no applied pressure) per degree change in temperature. The latter (TCS) is the fractional change in C_P (the capacitance under the application of a specified, fixed pressure) per degree change in temperature. Both quantities are commonly quoted as ppm$^{o}C^{-1}$ or % FSO$^{o}C^{-1}$. Much of the temperature sensitivity in devices similar to the SIMOX pressure sensor has been considered to be due to diaphragm stress, mismatch of material thermal characteristics and temperature generated expansion of gas trapped in the cavity. For the SIMOX sensor, it would be expected to be possible to achieve low thermal sensitivity, although the design was not optimised for this parameter, since the use of monocrystalline silicon for the entire substrate and diaphragm eliminates the unequal thermal expansion coefficients seen, for example in silicon/Pyrex or other multi material diaphragm designs which can

result in thermally induced bimetallic bending and high non-linearity of thermal characteristics. The temperature range investigated in the current work was limited by the practical constraints of the temperature controlled water bath used. The sealing of sensor cavities under vacuum conditions can reduce temperature sensitivity caused by gas expansion, but also reduces the device pressure sensitivity. Figure 5.22 illustrates the measured capacitance/temperature behaviour for a typical unsealed SIMOX device fabricated in the current work.

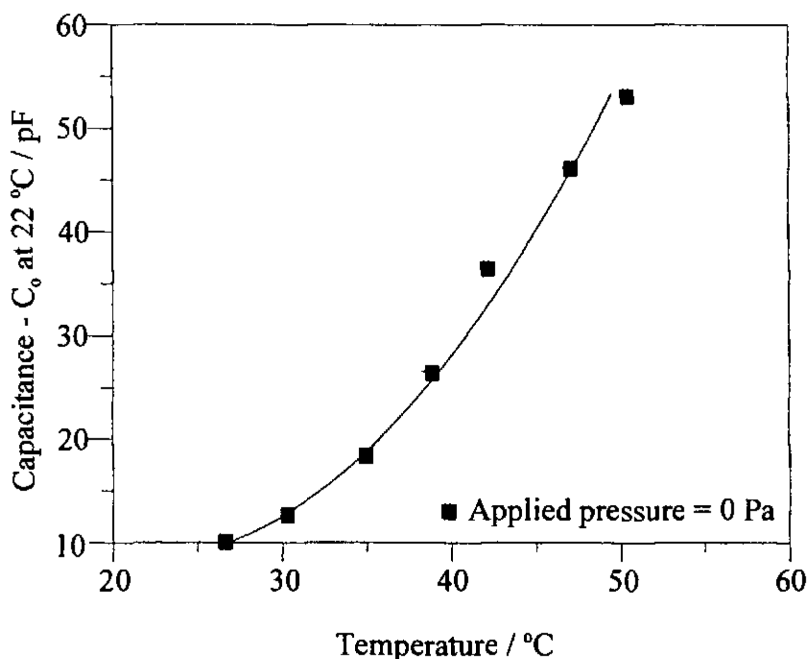


Figure 5.22 TCO for unsealed device

From the measurements shown in figure 5.22, a value of 1.01 % FSO°C^{-1} was determined for the TCO of an unsealed SIMOX device. This can be compared to the results shown in figure 5.23, for a similar SIMOX device, which was sealed under ambient clean room conditions. This allows the effects of gas expansion in the cavity and the thermal behaviour of the plug to be assessed.

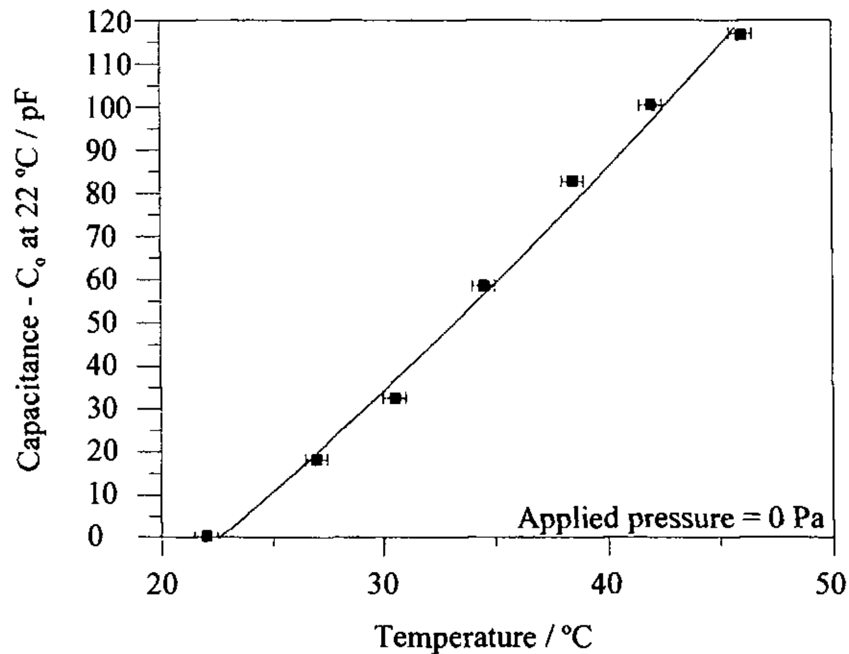


Figure 5.23 TCO for sealed device

This is similar to the previous graph for an unsealed device but results in a TCO of 0.95 % FSO°C^{-1}. However, for some devices a negative TCO has been reported in the literature for sealed devices [17]. This change from positive to negative coefficient has been accounted for by the expansion of trapped gas under the application of heat which applies an outward pressure on the diaphragm from within the cavity, deflecting the diaphragm away from the substrate. Hence for the SIMOX sensor it can be deduced from figures 5.22 and 5.23 that the effects of trapped gas are not sufficient to cause a dramatic reversal in temperature characteristics. Other factors, apart from stress which could cause temperature sensitivity in the SIMOX device include the behaviour of the polymer plug, when heated and effects within the SOI material structure such as electron leakage through the buried oxide. Despite the high temperature sensitivity seen for the SIMOX device, electronic compensation for this thermal sensitivity could be readily added to the sensor to reduce or eliminate this problem [18]. High performance circuitry is routinely achieved on SIMOX material and would be compatible with the standard processing techniques used for the sensor fabrication. Furthermore, since the application for this

device is medical and its small dimensions lend it to internal implementation, the small changes of temperature witnessed within the body, 37 °C ± 2 °C or smaller, reduce the significance of a high temperature sensitivity.

In order to assess the temperature coefficient of sensitivity (TCS) for a SIMOX capacitive pressure sensor, figure 5.24 shows the pressure/capacitance response curve for the same device at two different temperatures (28 and 31 °C). The maximum difference of 0.83 pF between the two curves, which occurs at a pressure of 23 cmHg corresponds to a TCS value of 9.2 % FSO°C^{-1}.

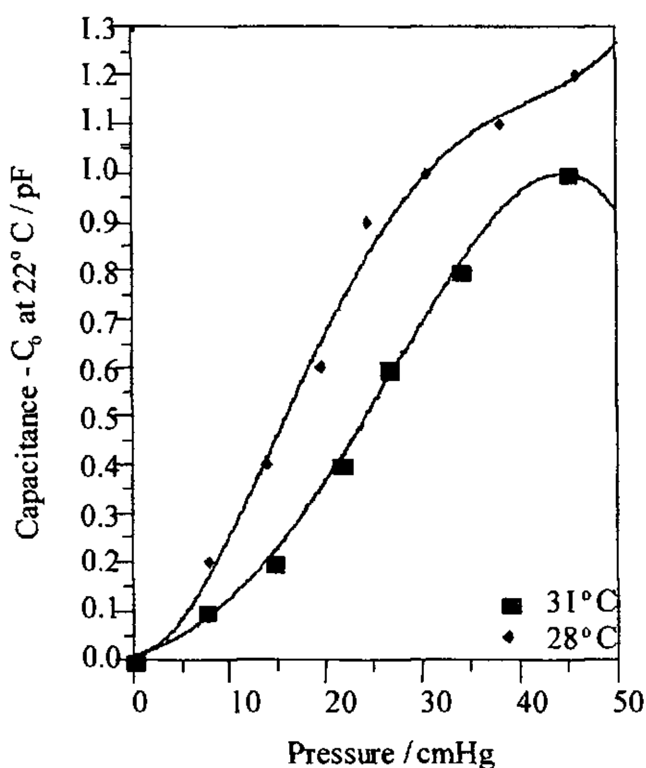


Figure 5.24 The temperature coefficient of sensitivity of a typical device

The hysteresis in sensor temperature sensitivity can be determined from the data shown in figure 5.25 as 2.91 % FSO. In designs with high compressive stress, buckling can occur at room temperature which results in hysteresis during temperature changes. The value for hysteresis in temperature sensitivity for the SIMOX sensor is low which implies low compressive stress.

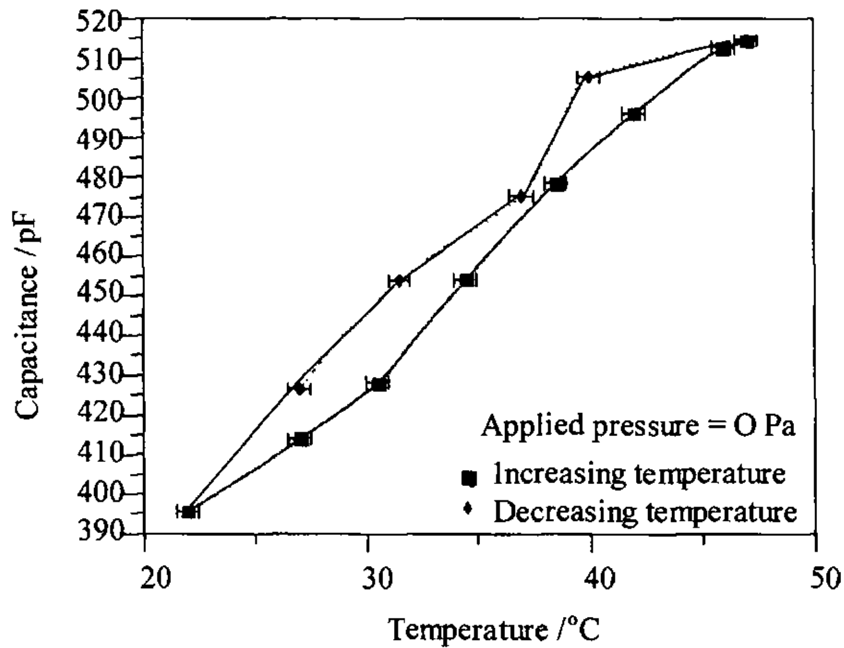


Figure 5.25 Hysteresis of temperature characteristics

The non-linearity of temperature sensitivity has also been assessed - this parameter is critical when considering how readily the effects of temperature can be compensated. Figure 5.26 indicates that the non-linearity of temperature sensitivity for a SIMOX sensor, which has been calculated as 1.7 % FSO.

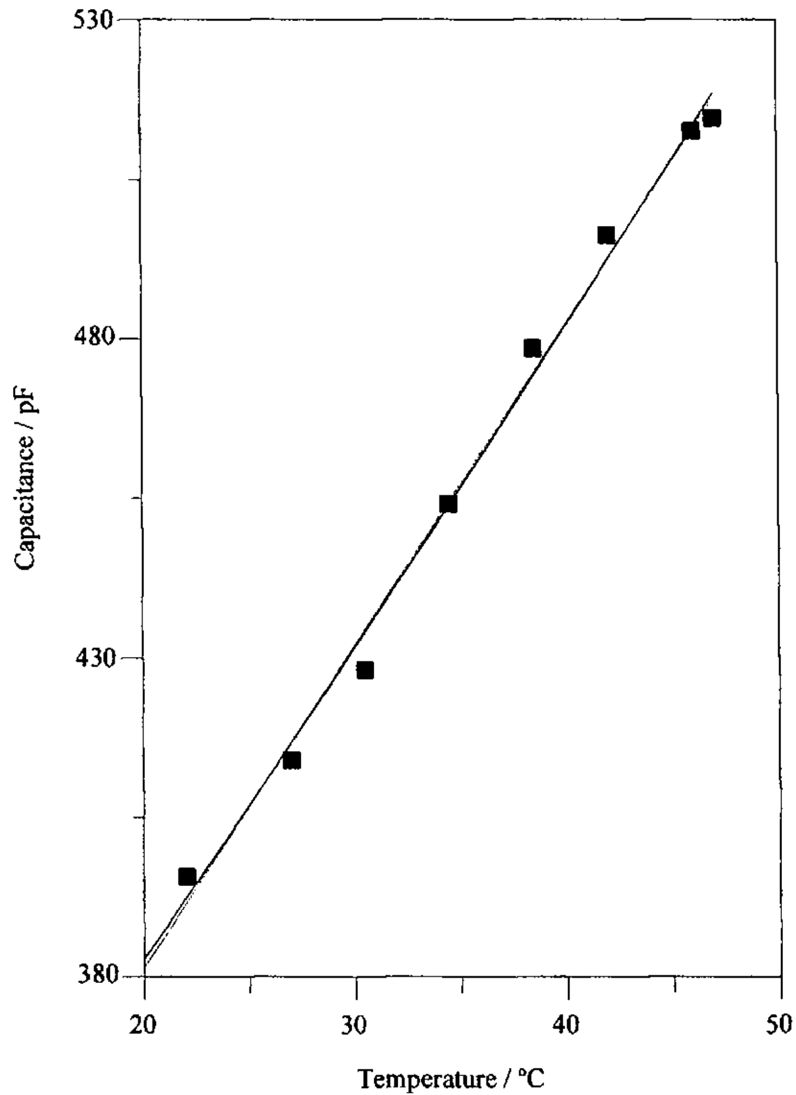


Figure 5.26 Non-linearity of temperature characteristics

The repeatability of a sensor is a measure of its ability to reproduce a reading at a particular temperature, under the same applied conditions approached from the same direction. It is effectively the maximum difference between two measurement sets from tests with identical conditions, stated as a percentage of full scale output.

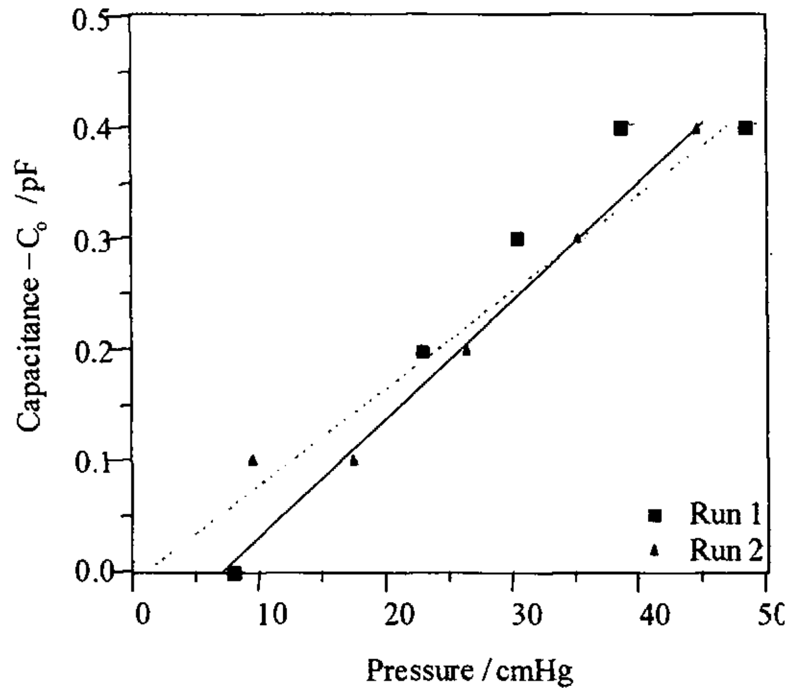


Figure 5.27 Assessment of sensor repeatability

The repeatability of the SIMOX sensor was investigated using a device with a 4 μm diameter plugged window and an undercut of 7 μm. The graph in figure 5.27 shows the repeatability from two consecutive sets of measurements. The two data sets have been appointed the same origin by the subtraction of the respective C_o from each data point. The worst repeatability between the runs is displayed at a pressure of ~ 7.5 cmHg which can be expressed 0.01 % FSO. The offset between the two capacitances at zero pressure is 0.3 pF.

The stability of the sensor was also assessed. Stability is commonly defined as the error band required to maintain a constant output under conditions of constant pressure and temperature. Measurements of the output capacitance were taken approximately every hour over a period of 6 hours under conditions of atmospheric pressure and a constant temperature of 28 °C. These results are shown in figure 5.28.

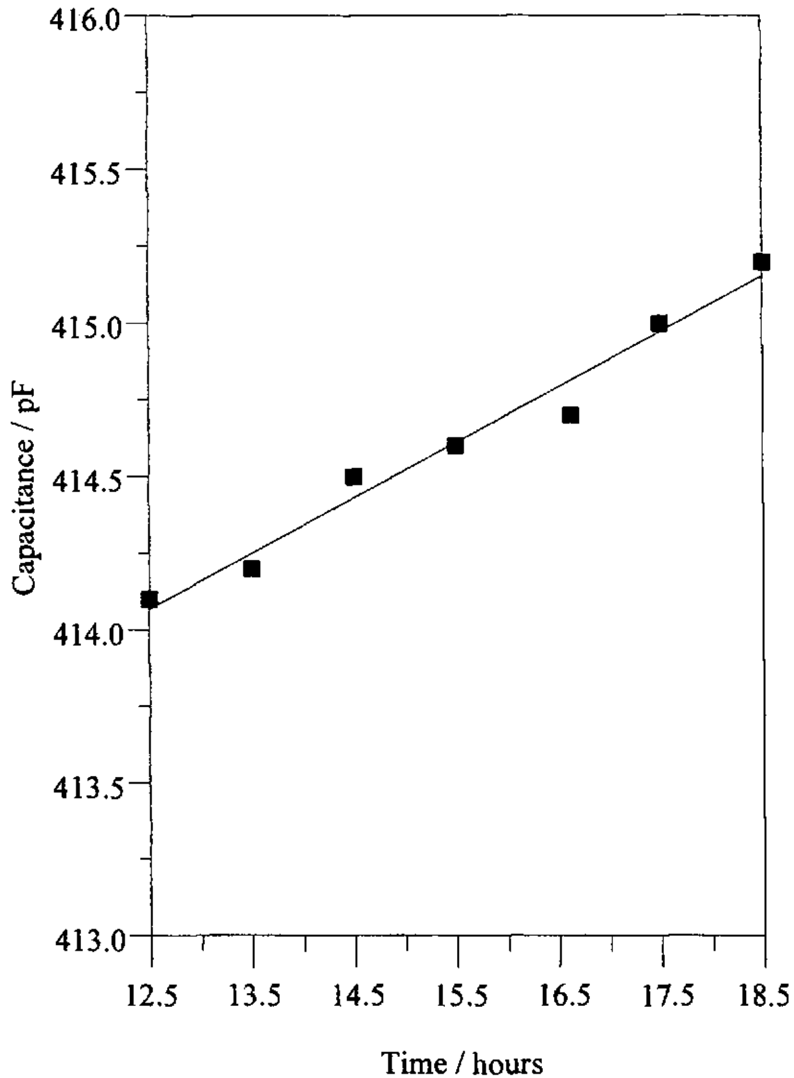


Figure 5.28 Sensor stability

Analysed directly this data set gives a stability of 0.14 % FS. However, the error in the temperature measurement for this experiment was ± 0.5 °C, which is fairly significant considering the high sensitivity of the output capacitance to temperature which has been observed. Furthermore one would expect device instability to occur in the positive and negative direction from the initial reading, whereas in this case the graph shows a continual upward trend. This could be accounted for by an upward trend in the temperature (remaining within the error band). Alternatively, since the data was collected following capacitance/pressure testing it may be the case that the one hour period between the completion of pressure application and stability measurement was not sufficient to allow full settling of the device back to its original state.

The long term drift of the SIMOX pressure sensor was also examined. This is defined as the difference in the measurement of a particular pressure at the same temperature following some lapse of time. This is considered a critical parameter for clinical use and was measured as 0.02 % FShour^{-1}. This is low compared to similar devices which would be expected due to the entirely silicon design and capacitive measurement means which is beneficial compared with piezoresistive means for this parameter [38]. However, this test was carried out over a fairly short length of time and over a longer period, a larger value would be expected.

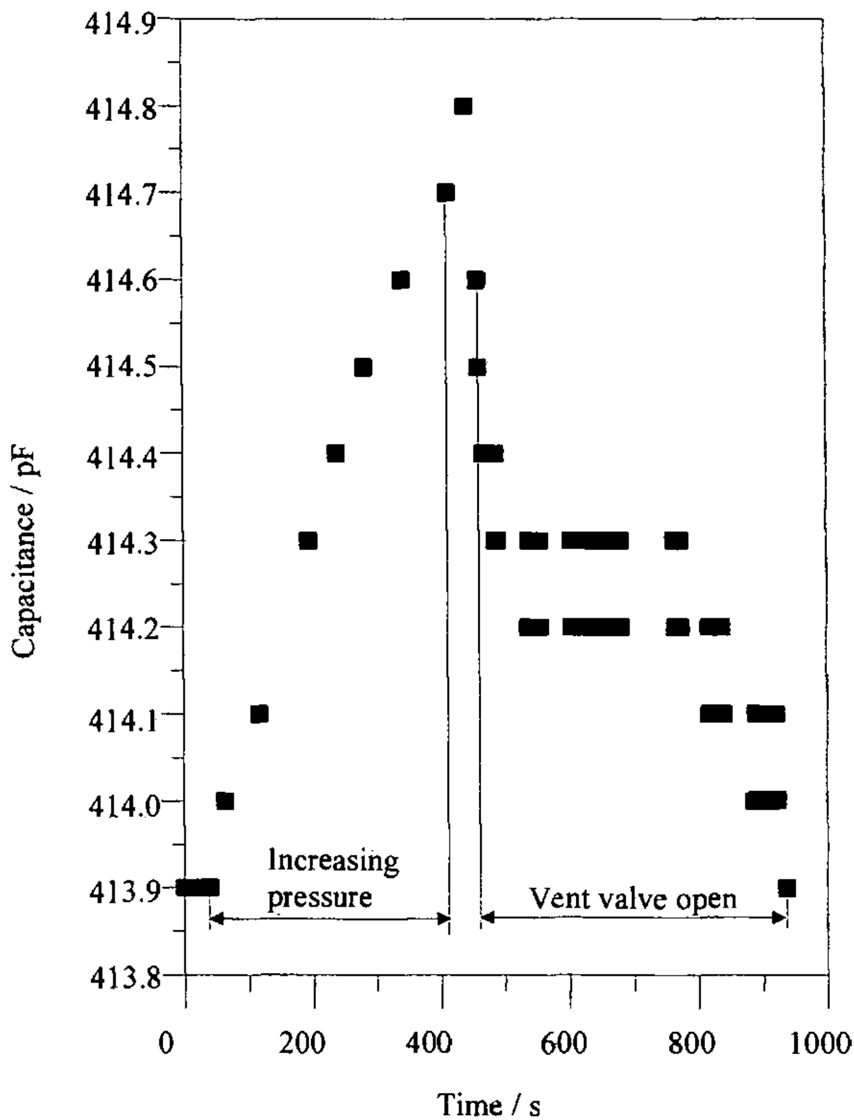


Figure 5.29 Response time for the pressure sensor on venting the chamber to atmospheric pressure

The response time was assessed for a SIMOX sensor, by monitoring the time taken on the release (by venting the chamber) of a 44.2 cmHg pressure, for the output capacitance to return to its original value (C_o prior to the application of any pressure) under conditions of constant temperature of 28 ± 0.5 °C. The response time calculated from figure 5.29 was 11.56 minutes. This is slow for a microsensor, however, this may be accounted for in two ways:

(i) As previously discussed there is considerable drift in the device output which seems exaggerated during and after testing. This may increase the response time as the 'target' baseline will have moved from the initial value.

(ii) The pressure application method may slow the reactions of the sensor as the mercury level observed in the manometer is seen to rise and settle fairly slowly following opening of the valve to the nitrogen source, and again settles slowly following opening of the valve to the test chamber.

5.7 ANALYSIS AND DISCUSSION OF RESULTS

On the whole the results of pressure sensor testing have been successful in showing that the sensor performs well. Several of the parameters which appear less satisfactory, such as the response time and pressure resolution reflect limitations in the the test equipment, which could be rectified by the use of an improved measurement system. However, the pressure measurement system has been shown to exhibit low levels of leakage which enhances the measurement accuracy. Possibly the most critical parameter, pressure sensitivity, is high for our device and its characteristic is fairly linear. The high sensitivity is related to the small dimensions of the diaphragm design, with a thin diaphragm and small substrate separation. The non-linearity has not been optimised by this pressure sensor design although the non-linearity of the 'as fabricated' device is already competitively low. Several studies have been undertaken [13] which demonstrate how diaphragm designs can be adapted to improve linearity, these adaptations could, if necessary be applied to the SIMOX sensor The hysteresis of the fabricated sensor is fair but possibly not as low as would be expected from an all monocrystalline silicon design, this however may be in part due to high cross sensitivities such as to temperature. The temperature sensitivity of both the offset capacitance and measurement capacitance of the sensor are high. This is the poorest parameter of the sensor performance and is thought to be primarily due to, the

temperature sensitivity of the electrical characteristics of the SIMOX material itself, the polymer plug and trapped air within the cavity. However, the temperature sensitivity does display a low hysteresis and good linearity, this means that it can be simply corrected with the addition of basic electronics or calibration techniques. Furthermore for medical usage, exposure to a large temperature range would not be expected. The repeatability of the SIMOX pressure sensor is high due to the small dimensions and array design, while the stability, long term drift and zero drift are all fair for the first iteration of a sensor design and could possibly be improved in subsequent designs or could be compensated for by the addition of appropriate electronics [19]. In the subsequent sections of this chapter, the sensor performance is shown to compare favourably to other similar devices reported in the literature and to the performance predictions made in chapter 3

5.7.1 COMPARISON OF PERFORMANCE TO PREDICTIONS

If we firstly consider the benefits proposed in chapter 1 of the SIMOX pressure sensor over traditional devices, it was expected that fabrication could be simplified by the use of single sided processing, and the elimination of the need to grow a sacrificial layer. This was indeed seen to be the case, with the design being successfully fabricated using underetching to form a working sensor. This design was also expected to allow a small size of device enabling its medical application without proving cumbersome or impractical for patients use. In terms of sensor performance, it was predicted in chapter 3 that such a device would display a high pressure sensitivity, estimated at 0.02 $pFkPa^{-1}$. Analysis of the test results showed that the sensitivity was indeed high and the mean sensitivity of all devices tested was in-fact 0.03 $pFkPa^{-1}$. Likewise the predicted change in capacitance for the application of the full pressure of 66 kPa, was 1.37 pF, the measured change was very close to this value at 1.35 pF. The monocrystalline nature of the diaphragm was expected to enable a device to be manufactured, which performed independently of the processing used and allowed stress free large diaphragms. It was also predicted that application of the full pressure range would not result in diaphragm breakage, this was seen to be the case in testing – with no fractured diaphragms observed. The predicted high performance resulting from the use of a monocrystalline silicon diaphragm was also

seen by the high repeatability and low hysteresis shown in figures 5.21 and 5.27. A low temperature sensitivity was also expected, however, this was not found to be the case; the high temperature sensitivity of the device is thought to originate from several sources which have already been discussed, but could be readily corrected for example by the addition of a reference chamber or electronics.

5.7.2 COMPARISON OF PERFORMANCE TO REPORTED PRESSURE SENSORS

In this section, the performance of the SIMOX micromachined pressure sensor is assessed by comparison with an extensive list of published capacitive devices which are sufficiently similar, this is summarised in table 5.4. This comparison includes pressure sensors of many different designs, utilising various diaphragm materials, furthermore some of those reported devices have been optimised for one or two particular sensor parameters, thus skewing the apparent performance of other devices under direct comparison. In some cases reported devices consist of the sensor alone while in other cases performance enhancing circuitry has also been included and it is often not specifically stated which of the presented measurements benefit from the additional electronics. These problems make direct comparisons difficult. There is also a lack of clarity in some published work where the text does not agree with data plotted in the figures. Having stressed these problems, comparison does allow insight into how the SIMOX sensor performs against similar devices that it would be expected to compete with in a commercial forum and therefore how relevant the current research is to the field of microsensors. In general, the results obtained from the SIMOX sensors compare favourably with other sensors, this is particularly encouraging since this device is in many respects the first iteration of a design which could easily be developed and optimised further. Measurement of some of the sensor parameters were limited by the measurement set-up and would be expected to show improvement if a more sophisticated system were used. With the addition of some simple and standard electronic circuitry, this sensor could rate among the best of those currently reported. It is considered that this is mainly due to the performance enhancing features of the basic sensor design such as the monocrystalline silicon diaphragm and small size, particularly diaphragm thickness and diaphragm to substrate separation, which are facilitated by the use of the layered SIMOX structure.

The pressure range for the fabricated devices, over which measurements were taken was approximately 66.66 kPa (or 500 mmHg); this was a limitation which was set by the measurement equipment. This pressure range is wider than several reported devices, all of which are combined silicon-Pyrex designs incorporating additional electronic circuitry, with measurement ranges from 20.39 Pa [20, 21] 39996 Pa [22, 23]. Without the constraints of the pressure measurement equipment the SIMOX sensors would be expected to show an even wider pressure range. Firstly, the device was initially designed to deflect to just ~10 % the cavity depth at a pressure of 66.66 kPa, indicating that it could be sensitive (in terms of available deflection) to pressures considerably greater than 66.66 kPa, this would allow for a pressure range wider than the majority of reported devices. Secondly the substrate will act as an overpressure stop, meaning that beyond its operational pressure range, the sensor would not be destroyed.

The capacitance, under no application of pressure, essentially reflects the non-variable parasitic capacitance of the pressure sensor; for the SIMOX sensor this value was relatively high but could easily be reduced by the addition of some electronic circuitry. For the SIMOX pressure sensor the base capacitance (C_0) differed from sensor to sensor, but was typically 120 - 430 pF at 28 ± 0.5 °C depending on the device dimensions. Published data on the base capacitance for similar sensors gives values between 41 fF to 24 pF [24]. However, base capacitance is dependent upon the temperature at which it is measured and in these reports no temperatures were given. For further comparison, a list of C_0 values for capacitive pressure sensors is given in *capacitive sensors: when and how to use them* [24] but again no temperature values are given.

The pressure sensitivity for the SIMOX pressure sensor has been calculated as 0.000043 $pFPa^{-1}$, this is a highly competitive sensitivity for this type of micromachined device and is sufficiently high for many sensing applications. It is in fact only bettered by two reported devices [21, 22], of those considered to be similar enough to be compared, which are Pyrex-silicon devices incorporating electronic calibration or compensation. Both have square diaphragms and large diaphragm sizes compared to many other devices (approx. 2 mm^2) resulting in sensitivities of 0.0074 $pFPa^{-1}$ [22] and 0.00052 $pFPa^{-1}$ [21]. All other devices which have been compared show lower sensitivities to applied pressure than that demonstrated by the SIMOX

device, these range from 0.0000003 [5] - 0.00001 [13] $pFPa^{-1}$. In designs where boron doping of the diaphragm has been utilised as an etch stop, the doping has been seen to cause high tensile stress in the diaphragm resulting in reduced pressure sensitivity [5].

There is inherent non-linearity in the capacitance/pressure response curve, however for an ideal pressure sensor this should be minimised. The non-linearity is also highly dependent on the diaphragm design. A standard flat diaphragm only remains linear in terms of its displacement while its displacement is considerably less than its thickness, furthermore with any diaphragm design, non-linearity results as the centre deflection approaches the depth of the cavity. Non-linearity can also result from membrane curvature under conditions of no applied pressure, which in some designs results from fabrication procedures. By minimising the diaphragm movement to ~ 30 % of the total available deflection, the linearity of the device can be enhanced [25]. Work to optimise pressure sensors with respect to improved linearity has been described in the literature [13], this obtained a non-linearity of < 1 % by allowing the membrane to touch the bottom of the cavity and introducing weakened and strengthened regions to the diaphragm. By adjusting the diaphragm design to address the non-linearity of the response the addition of electronics can be avoided or at least their complexity reduced. In SIMOX sensor fabrication, thinning of the diaphragm in selected regions or the addition of a central boss could be achieved in just one extra photolithography/etch step. Three publications have reported lower non-linearities at 0.1 % FS [22, 26, 27], one is of limited validity [22] since over a capacitive output range of 100 pF, the linearity is considered over just 5 pF of that range. The second [26] incorporates a diaphragm optimised for high linearity by the addition of a central boss and corrugations. [27] *et. al.* reports a capacitive pressure sensor which uses feedback to control excitation voltage which adjusts the non linearity. The SIMOX pressure sensor displayed a non-linearity of 0.016 % FS. This is better than all the above devices which were optimised for linearity and other devices considered for comparison have significantly larger values for non-linearity of 3 % FSO [28], 3.6 % FS [20], 4 % FSO [2, 25] up to 16 % FSO [17, 29]. It is stated that this could be readily corrected using compensation circuitry and likewise the 4 % FSO non-linearity listed above has been reduced to 1.85 % FSO by the aid of electronics. In the same way the low non-linearity of the SIMOX device could be reduced further by electronic means.

The hysteresis of the SIMOX pressure sensor is also very low, falling within the bounds of experimental error, this would be expected as hysteresis generally results from the diaphragm material quality and the monocrystalline diaphragm should display virtually no hysteresis compared to alternative diaphragm materials which are commonly used. However, few of the published pressure sensors state the hysteresis of the pressure capacitance characteristic. Of those which do, a silicon nitride diaphragm design [16] displayed a hysteresis of 2 %, which was considered to be primarily due to the influence of aluminium pads and tracks which cross the diaphragm. A silicon dioxide - chrome - silicon dioxide diaphragm has been reported with hysteresis of 0.2 % FSO for applied pressures below 800 kPa and 0.5 % FSO above 800 kPa. Although in part due to the multilayer structure, the hysteresis at high pressure values was considered in part to be due to energy lost by friction as the diaphragm contacts the substrate.

The resolution of pressure sensors is a parameter often detailed in published work [14], however, for the fabricated SIMOX sensor, it is difficult to assess as the resolution measured in the experimental work as 5119 Pa was limited by the measurement equipment and not by the sensor itself. Without this constraint the sensor would be expected to resolve much smaller pressures, due to its small size. Other devices display a range of resolutions from 10 Pa [30], 13.33 Pa [22], 133.32 Pa [29], 399.96 Pa [5], 540 Pa [14] up to 799.92 Pa [23] the last value is reported to be due, in part to sealing of the sensor cavity at atmospheric pressure. However, each of the sensors in the above also benefits from additional electronic circuitry which would be expected to enable smaller pressure changes to be resolved than for the case of a device without electronics such as the SIMOX sensor. In fact in some cases [23] a long detection period was required to obtain the high resolution.

For the SIMOX pressure sensor, which is sealed with photoresist under ambient conditions, a TCO of 0.95 % FSO$^{\circ}C^{-1}$ has been calculated, expressed in % FS as many other device parameters are, this corresponds to 0.22 % FS. A negative TCO of - 0.39 % FSO$^{\circ}C^{-1}$ has been reported for a sealed device [17], which is considered to be due to the expansion of trapped gas under the application of heat, causing outward pressure on the diaphragm and deflecting it away from the substrate. This is likely since the diaphragm dimensions in the sensor described by Chau [17] are considerably larger than ours, and the design was square. A square membrane is reported to deflect

more than a circular one under application of equal pressures and combined with the larger membrane diaphragm would be expected to give a larger deflection for the same internal pressure than the SIMOX sensor. Reported devices which have been sealed under vacuum conditions have TCO values of 0.02 % FSO°C^{-1} [2] and 0.012 % FSO°C^{-1} [31], these are both silicon/glass structures. Measurements made on sensors via compensating electronics give values of 0.013 % FS°C^{-1} [20] with unspecified sealing conditions, 3.85 % FS°C^{-1} [32] sealed in a vacuum and 3 % FS°C^{-1} [23] sealed under ambient conditions. These were all measured over a similar range to that used for the SIMOX device. It can be seen that in some cases the inclusion of electronics can actually degrade the thermal sensitivity of a device while enhancing other aspects of its performance. It can be seen that our device has a fairly high TCO, compared with these devices. This is considered partially due to the SIMOX material, which displays some temperature sensitivity in its unprocessed form.

The primary effects resulting in temperature sensitivity of capacitive pressure sensors in general are:

(i) Expansion of gas in cavity, causing diaphragm deflection away from the substrate (when sealed under ambient conditions).
(ii) Mismatch in thermal expansion coefficients of the materials used [33].
(iii) Temperature sensitivity in the circuitry.
(iv) Bimetallic mode bending where metal is used on the diaphragm.
(v) Out-gassing of the material used to seal the cavity.
(vi) Temperature sensitivity of the diaphragm stress resulting in buckling.

In general improved pressure sensitivity results in poorer temperature performance. Thermally induced gas expansion within the cavity induces thermal drift and can result in an offset to the diaphragm displacement which can hinder measurements of small pressures. Ambient sealed devices are expected to display increased temperature sensitivity but reduced pressure sensitivity [5], the reduced pressure sensitivity compared with vacuum sealed devices under conditions of applied pressure, is due to the gas pressure inside the cavity increasing while the volume of the cavity is decreased, this reduces the true differential pressure.

When temperature sensitivity is displayed, it is preferable that the change in capacitance under no applied pressure is linear with temperature, in this case it can be

more readily compensated or calibrated. For the SIMOX sensor there is a linear relationship for the temperature sensitivity but this is not always the case, in some reported devices the offset shift displays strong non-linearity [20].

The value from the graph for TCO of the unsealed, SIMOX sensor, of 1.01 % FSO°C^{-1} is somewhat higher than the reported 0.0075 % FSO°C^{-1} for an unsealed silicon/Pyrex

diaphragm sensor [17]. Any material sensitivity to temperature should be as equally evident in the unsealed structure as in the sealed device and is thought to contribute the majority of the temperature sensitivity of this unsealed sensor, since most of the conventional mechanisms causing temperature sensitivity would not be present for an unsealed sensor.

The temperature hysteresis measured on a SIMOX pressure sensor was low at 2.91 % FSO, this compares with a reported value of 10 % FSO for a silicon/Pyrex design [2] which was considered to be due to compressive stress in the diaphragm causing variations in the degree of diaphragm buckling with temperature. The temperature coefficient of sensitivity of a typical SIMOX pressure sensor was 9.2 % FSO°C^{-1}, or 0.027 % FS°C^{-1}. This would be expected to result from material temperature sensitivity in much the same way as the TCO. However, the TCS value does compare better with reported values for other devices such as 0.005 % FS°C^{-1} [6], 0.01 % FS°C^{-1} [30, 5], 0.02 % FSO°C^{-1} [2], 0.03 % FS°C^{-1} [20], 0.3 % FS°C^{-1} [22], 0.8 % FS°C^{-1} [28], 1.0 % FS°C^{-1} [34]. The same mechanisms will result in temperature dependant sensitivity as cause temperature dependant offset, and a linear dependence allows easier rectification.

The long term drift of the SIMOX sensor was measured as 0.02 % FSOhour^{-1} and the stability as 0.14 % FS. The stability of a silicon/glass/silicon sensor has been assessed under conditions of a constant applied pressure of 110000 Pa [30] over a period of 600 days. Measurements taken independently of the electronics present are stated as giving a stability of 0.1 % FS although the graph of stability published [30] indicated a higher value of 0.8 % of FS capacitance. An alternative design which has been optimised for long term stability [31], has been subjected to several different stability tests. In addition to the standard variation of C_o with time, C_o was also measured after cycling the pressure from 0 - 80 % FS pressure, and after applying a constant pressure

of 80 % FS pressure. A 5 - 30 hour settling time was allowed prior to measurements which were taken over a period of 4 - 10 days, no long term drift could be detected in excess of the uncertainty of the measurement system ± 0.01 % FSO [31]. In some cases the electronics can in fact reduce the long term stability of the device overall [22].

Obviously for many microsensor applications, minimising the size of the chip is one of the critical criteria for optimisation, the size of the SIMOX pressure sensor chip is 3.7 x 3.4 mm, this would be expected to compare favourably with similar devices since the structure of the SIMOX material allows a fabrication regime which minimises the size of the functional elements. The actual diaphragm size is a circular area with a diameter of approximately 17 μm. Considering just the chip area, other reported devices have a chip size ranging from 0.49 mm^2 for a Pyrex/silicon design which had been optimised for small size to allow its insertion in a catheter. The SIMOX sensor fabricated in this work rates approximately midway in size in a list of published devices (see table 5.4). Further listings of the die sizes of typical sensors are given in reviews in [22] and [24]. It is also considered that future iterations of the SIMOX sensor could easily be considerably reduced in size, by for example improving the design layout. Expressed as an area, each individual SIMOX diaphragm is 227 μm^2 which is lower than all other devices found for comparison. This would be very much expected since the diaphragm operates as just one element in an array, however, when the individual diaphragm area is multiplied by the number of devices in the array, the total diaphragm area remains highly competitive at 567450 μm^2. The smallest diaphragm size reported in the literature is 10000 μm^2 for an all silicon square diaphragm design [14]. A device with a silicon diaphragm on a glass substrate has a diaphragm of 159500 μm^2 [17]. All other devices discussed here incorporate increasingly large diaphragms up to a value of 12250000 μm^2 [35]. The separation of the diaphragm from the substrate (or cavity base) is also a significant value for comparison as this affects output parameters such as the pressure sensitivity and measurement range. For the SIMOX sensor the separation was the depth of removed, implanted oxide in the SIMOX material which is 0.4 μm. Of all the published work reviewed here this is the smallest separation for a pressure sensor and can be compared with reported separation values for different sensor designs, ranging from 0.5 μm [34] up to 20 μm [29].

There are several other reported devices in which the pressure sensor is formed from an array of identical diaphragms connected in parallel [2, 16, 24]. The main benefits of this arrangement are increased capacitance output, increased yield of fabrication and better repeatability in output characteristics. In the case of the SIMOX sensor there are 2500 diaphragms in the array, this is by far the largest array in terms of number of devices which has been reported to date in the literature. Others array devices which have been reported incorporate 240 [2], 81 [24] and 50 [16] diaphragms.

When fabricating devices from silicon, in general the technology which is used, is borrowed from the integrated circuit industry, one of the benefits of this is that devices can be batch fabricated. For SIMOX sensor fabrication, whole wafers were not used and test structures were also incorporated in the mask design, however, if a design containing only sensor structures was used, a 4 inch diameter SIMOX wafer would yield approximately 548 sensor chips. This compares to reported chip volumes of 20 [23] from a 20 mm x 20 mm silicon substrate and 88 chips from a 3 inch diameter wafer [30]. To manufacture the sensor structure described in this work, the fabrication process developed uses just 3 masks for silicon/silicon dioxide etch, aluminium etch and plug definition. To the author's knowledge, this is fewer steps than all of the pressure sensors studied which have stated the number of masking steps used. It is desirable to minimise the number of masking steps as this reduces the time and cost of manufacture and the likelihood of defect introduction. For fabrication of a glass-silicon dioxide design, using underetching of an aluminium sacrificial layer [2] and a silicon-Pyrex design using anodic bonding [28] four masking steps were used. A second glass-silicon design which was elecrostatically bonded used 5 mask levels [5] while a trilayered silicon/glass/silicon anodically bonded structure was achieved using 7 mask levels [30].

The comparison between the performance of the SIMOX pressure sensor developed in this work, with similar reported devices is summarised in table 5.4.

Parameter	Fabricated SIMOX sensor	Other reported sensors
Pressure range	66.66 kPa	20.39 Pa [20] 40 kPa [22]
Base capacitance	120 - 427 pF	41 fF - 24 pF [24]
Pressure sensitivity	4.3×10^{-5} pFPa^{-1}	1×10^{-5} pFPa^{-1} [13] 1.25×10^{-6} pFPa^{-1} [28] 2.8×10^{-6} pFPa^{-1} [2] 3.8×10^{-6} pFPa^{-1} [14] 3.1×10^{-7} pFPa^{-1} [5]
Non-linearity	0.016 % FSO	3 % FSO [28] 4 % FSO [2] 16 % FSO [17]
Hysteresis	Within experimental error	2 % FSO [16]
Resolution	5119 Pa	10 Pa [30] 133.32 Pa [29] 399.96 Pa [5] 540 Pa [14] 799.92 Pa [23]
TCO	0.95 % FSO°C^{-1}	0.012 % FSO°C^{-1} [31] 0.02 % FSO°C^{-1} [2]
TCS	0.027 % FS°C^{-1}	0.005 % FS°C^{-1} [6] 0.01 % FS°C^{-1} [30] 0.03 % FS°C^{-1} [20] 0.3 % FS°C^{-1} [22] 0.8 % FS°C^{-1} [28] 1 % FS°C^{-1} [34]
Temperature hysteresis	2.91 % FSO	10 %FSO [2]
Stability	0.14 % FS°C^{-1}	0.1 % FS [30]
Chip size	3.7 x 3.4 mm^2	1.8 x 2.3 mm^2 [32] 2 x 3 mm^2 [432] 1.5 x 3.8 mm^2 [36] 7 x 7 mm^2 [3]
Diaphragm area	227 μm^2 or 567450 μm^2 for array for a typical device	10000 μm^2 [14] 159500 μm^2 [17] 2560000 μm^2 [37] 12250000 μm^2 [35]
Plate separation	0.4 μm	0.5 μm [34] 20 μm [29]
Diaphragms / array	2500	50 [16] 81 [24] 240 [2]
Chips / wafer	548 / 4"	20 / 20 mm^2 substrate [23] 88 / 3" [30]
Masking steps	3	4 [2,28] 5 [5] 6 [37] 7 [30]

Table 5.4 Tabulated comparison of SIMOX sensor with reported devices

The final comparison is with, to the authors knowledge, the only other SIMOX capacitive pressure sensor which has been reported [38]. Diem *et. al.* [38] have recently fabricated a similar device which consists of an array of 4 diaphragms which are each 300mm in diameter from a 4 mm thick epitaxial silicon SIMOX layer. This results in a very similar aspect ratio as the SIMOX diaphragms in the current work and the resulting sensitivity is also comparable to our mean value at 0.02 $pFkPa^{-1}$. The diaphragms in Diem's work are formed by silicon dioxide underetching and plugged with a CVD deposited dielectric. Diem's work was reported [38] after the current work had been published and has the disadvantage of much larger diaphragms which would be expected to increase device fragility and the etch time required for production. The report also refers to the epitaxial silicon (from which the diaphragm is formed), as doped, if this is the case poor long term stability and hysteresis would be expected, for going some of the inherent advantages of the SIMOX monocrystalline silicon layer.

5.9 SUMMARY

This chapter has reported primarily on the results of the measurements performed on the as fabricated pressure sensor. These results were analysed and compared with similar (non SIMOX) reported devices and performance predictions made in chapter 3.

Firstly the optimum, novel fabrication sequence established from the work reported in chapter 4, was summarised together with a discussion of the primary difficulties faced in sensor fabrication. The 'final' structure of the pressure sensor developed in this work was given. Using this structure, both single and array structures were successfully fabricated, as shown by optical micrographs of these structures. An important point to note is that in contrast to other designs, the SIMOX sensor can be fabricated using single-sided wafer processing and only three masking steps. This implies that simple low cost mass production may be feasible for this type of pressure sensor design.

An introduction to the critical parameters for sensor performance was given together with an overview of the measurement set up and analysis methods used. The measurements carried out on the sensor demonstrated that the fabricated SIMOX structure performs well as a pressure sensor and compares favourably to other

published devices. The critical sensor characteristics of pressure sensitivity, linearity, hysteresis, stability and temperature coefficient of sensitivity which were investigated in this work demonstrate a device which exhibits high performance and which is improved in these aspects compared with many similar reported devices.

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CHAPTER 6: MICROSTRUCTURES FROM SIMOX

6.0 INTRODUCTION
6.1 CANTILEVERS
6.2 MICROBRIDGES OR MICROBEAMS
6.3 LATERAL FIELD EMISSION TIPS
6.4 GEARS AND MICROMOTORS
6.5 RESONATORS
6.6 QUANTUM WIRES
6.7 'BRIDGE OF HOLES'
6.8 SUMMARY
6.9 REFERENCES

6.0 INTRODUCTION

Chapters 3 to 5 have reported on work conducted towards the primary aim of this project - to design, fabricate and evaluate a high performance pressure sensor. An additional aim outlined in chapter 1 was to fabricate a number of alternative microstructures to demonstrate the feasibility of this SIMOX technology to a wider field of application and to illustrate the versatility of the novel technology developed in this thesis. Micromachining techniques have been used to fabricate complex structures, which can be combined with on-chip circuitry [1]. The microstructures fabricated in this work are all based on suspended elements and can be realised using exactly the same processing steps used for pressure sensor fabrication; and include the fundamental structures of bridges, cantilevers and resonators which are effectively the 'building blocks' of many micromechanical devices. These devices would be expected to benefit, like the pressure sensor, from the simple fabrication method, incorporation of single crystal silicon active components and reduced thermal mismatch due to the all silicon design. The microstructures described in the following sections were not metallised and therefore have not been electrically characterised. No

additional optimisation was carried out for particular modes of operation, leaving considerable scope for improvement of these 'proof of principle' structures. As the field of microtechnology continues to grow, additional devices which could be manufactured using the novel SIMOX technology described in this thesis, will inevitably become apparent.

6.1 CANTILEVERS

A cantilever is effectively a rectangular plate clamped on one side and free to deflect at the opposite. Cantilevers are one of the most fundamental structures used in sensors for the measurement of parameters such as transient pressure, stress, force and acceleration. In addition cantilevers are commonly incorporated in actuators and micromachines and also have uses in thermal isolation applications.

In sensing applications, it is possible to measure the deflection directly e.g. by interferometry, however, it is more usual to measure the deflection using capacitive, piezoresistive or resonant frequency methods. For capacitive measurement a top electrode is located on the cantilever and a bottom electrode on the substrate. For piezoresistive measurement, piezoresistors are generally located on the clamped end of the cantilever where the stress arising from deflection is at a maximum. Where resonance is employed, a change in the resonant frequency of the cantilever due to the application of the measurand is monitored. Ideal requirements for cantilever structures are repeatable and reliable fabrication, low intrinsic stress, freedom from hysteresis and a high sensitivity to the external measureand. The sensitivity of a cantilever can be increased, and the resonant frequency modified, by loading the free end with a small mass called a 'proof mass' [2]. For undoped cantilevers, such as the ones described here, electronic integration may be achieved by the incorporation of active circuit elements [3]. A typical high volume application of a microcantilever structure is in acceleration sensors for the deployment of air bags in automobiles.

A number of cantilever structures were fabricated from SIMOX using the same method of fabrication as the pressure sensor. These ranged in width from 1 to 10 μm and in length from 3 to 10 μm, the thickness was 0.2 μm as determined by the SIMOX starting material. Some typical examples are shown in figure 6.1.

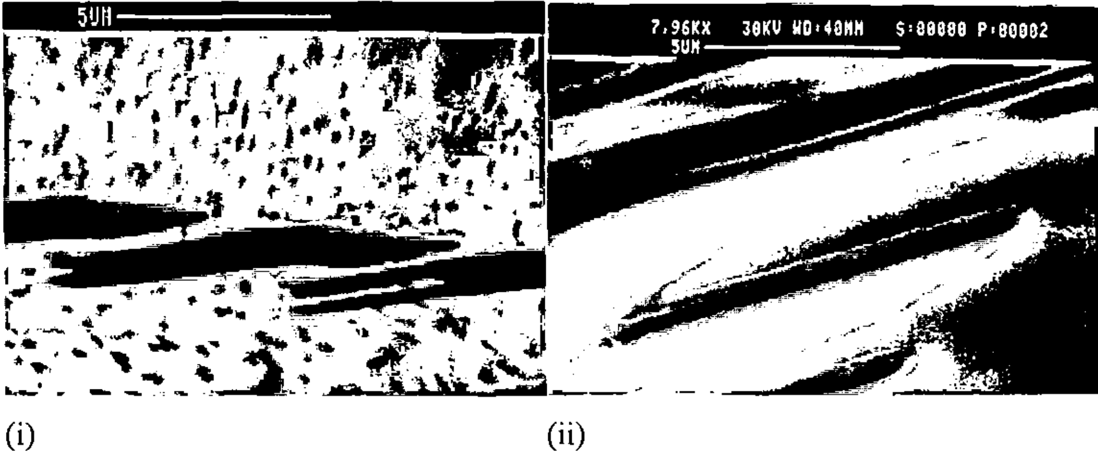
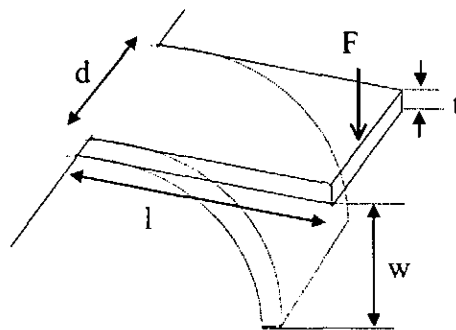


Figure 6.1 Examples of cantilevers fabricated from SIMOX using the process developed during this work.

Figure 6.1 (i) shows two cantilevers of the same length but different widths, figure 6.1 (ii) shows a much wider cantilever. All structures appear fully released and suspended above the substrate, no signs of bowing are evident.

For the purpose of simple illustrative calculations the dimensions of a 'typical' cantilever from the examples fabricated in the current work will be used. This 'typical' structure is characterised by a 4 μm length, 1 μm width and 0.2 μm thickness. Figure 6.2 shows a schematic of the cantilever with the critical dimensions defined.



where

F = force, d = width, t = thickness, l = length and w = deflection

Figure 6.2 Diagrammatic representation of a typical cantilever.

In the following sections, this cantilever will be discussed in terms of deflection, resonant and thermal modes of operation.

In using a cantilever to sense force or acceleration for example, its deflection is often the parameter of concern. It can be shown that the maximum deflection, w, of a cantilever of this type under a load F is described using classical beam theory by equation 6.1 [2].

$$w = \frac{4Fl^3}{Edt^3} \tag{6.1}$$

where
w = deflection
F = force
l = cantilever length
E = Youngs modulus
t = cantilever thickness
d = cantilever width

This equation indicates that a narrow cantilever will deflect more than a wide cantilever. However, the length and thickness of the cantilever have a greater effect on the deflection as these are cubed factors. A long, thin beam will deflect more than a short, thick one. For the purposes of maintaining the miniature nature of these microstructures it is preferable to reduce the thickness rather than increase the length of the cantilever. Therefore cantilevers fabricated from SIMOX, which are substantially thinner than commonly reported structures, will show much larger deflection for a particular force and given length and hence offer higher sensitivity to the measurand. Any variation in thickness will also be cubed in terms of the 'error' in deflection, since the thickness is accurately controlled by the starting material and not an etch or deposition step we would expect high repeatability in the force/deflection characteristics for SIMOX cantilevers. Being composed of very high quality, single crystal silicon, these cantilevers would be expected to show virtually no creep, hysteresis or ageing effects unlike polysilicon or doped silicon which are commonly used alternatives [4].

Equation 6.1 may be used to deduce the magnitude of force which would be required for the cantilever to deflect 0.4 μm - the full distance of the removed buried oxide gap. This is relevant to those applications which use contact of the cantilever to the substrate as the sensing mechanism and also suggests an upper measurand limit for non-contacting applications. In this case, using the 'typical' cantilever dimensions, the force required to induce substrate contact is calculated as 2.38×10^{-6} N.

The maximum stress, σ_{max} in a cantilever - which occurs at the fixed end - is given by equation 6.2 [2]

$$\sigma_{max} = \frac{6Fl}{t^2 d} \qquad (6.2)$$

Using the above force required to deflect the typical cantilever by 0.4 μm, the maximum stress in the cantilever has been calculated as ~ 1.43 GPa. This is well below the fracture strength of silicon (approximately 6 GPa [5]) indicating that the cantilever will not be broken by the application of this force. Under the application of increased force, substrate contact would be expected to protect the cantilever from breakage.

The frequency of vibration of a cantilever offers an alternative to the direct measurement of deflection. Here the resonant frequency of the cantilever is the critical parameter, which can be altered by the measurand. Frequency is particularly easy to measure with modern digital electronics [6] and the resonant frequency of the beam can be chosen to ensure a very high sensitivity to the parameter of interest. The resonant frequency of a cantilever beam is determined by the material properties and the beam geometry and is given by equation 6.3 [2].

$$f \approx 0.16\left(\frac{E}{\rho}\right)^{0.5}\left(\frac{t}{l^2}\right) \qquad (6.3)$$

where

f = resonant frequency
ρ = density
all other symbols are as previously defined

The relationship between cantilever length and resonant frequency described by equation 6.3 has been utilised for a vibration sensor [7]. This consisted of an array of 50 cantilevers of different lengths, which resonate at different frequencies. Ideally a cantilever employed in a sensor should have high resonant frequency, Q factor, stability and sensitivity. The excellent mechanical properties of single crystal silicon allow these requirements to be well satisfied [8]. Equation 6.3 can be applied to the 'typical' cantilever fabricated from SIMOX in the current work, and yields a resonant frequency of ~ 18 MHz. The resonant frequency for cantilevers employed in sensors is reported as typically 20 - 40 kHz [9], however, the SIMOX cantilever is very much smaller - by a factor of around 500 - as compared with the typical reported devices [9], resulting in the considerably higher resonant frequency.

Cantilevers are also commonly used to fabricate thermal sensors [9]. Here, the small, structure, almost isolated from the substrate has a high thermal resistance and can be heated to a detectable temperature at a much smaller power than would be required for a bulk sensor. This results in a device which has high sensitivity with low power consumption and a fast response time. Heat dissipated at the tip of the beam, for example by a laser, flows through the cantilever to the fixed end. The high thermal resistance results in a large temperature gradient along the cantilever which can be measured by a thermopile formed on the beam surface. The large thermal mass of the substrate provides an effectively constant temperature heat sink at the fixed end of the beam. Thermal applications of cantilevers are in temperature and flow sensing. For a cantilever it can be shown that the thermal sheet resistance, R_{st} is given by [9]

$$R_{st} = \frac{1}{kt} \qquad (6.4)$$

where

k = thermal conductivity
t = cantilever thickness

Considering the case where the cantilever is in a vacuum (there is no heat loss via conduction or radiation), the thermal resistance, R_{th} of the cantilever is given by equation 6.5 [9]

$$R_{th} = \frac{1}{kt}\left(\frac{l}{d}\right) \tag{6.5}$$

where

k = thermal conductivity
t = cantilever thickness
l = length of cantilever along which the temperature difference is being measured
d = width of the cantilever

This equation implies that a good thermal sensor requires long, narrow, thin cantilevers with constant thermal properties, as displayed by the single crystal silicon of SIMOX. Returning to the 'typical' SIMOX cantilever discussed above, the thermal resistance of such a structure would be in the region of 1.3×10^5 kW^{-1}. This is a high thermal resistance as predicted from the interpretation of the equation and would be expected to result in a device with high sensitivity. To further increase the sensitivity, the design could be readily narrowed and lengthened by a simple mask design change and a plate added to the free end to allow a larger area of interaction with the heating source.

6.2 MICROBRIDGES OR MICROBEAMS

A microbridge is effectively a rectangular plate clamped on two opposite sides which is free to deflect at its centre. These are also fundamental structures for micromachined sensors and other applications, the same ideal material properties discussed for cantilevers apply here. Bridges are frequently used in sensors for the measurement of parameters such as force, stress, thermal fluctuations and flow. As the measurand is applied the resultant bridge deflection, change in stress or resonant frequency can be measured, for example by capacitive or piezoresistive means. A typical example of a sensor which utilizes a resonant microbridge is a chemical vapour sensor, in this case the absorption of vapour onto a cantilever will alter the beam mass and therefore the resonant frequency [8].

A range of microbridges of varying dimensions were fabricated from SIMOX during this work. Some examples of these structures are shown in the micrographs in figure 6.3.

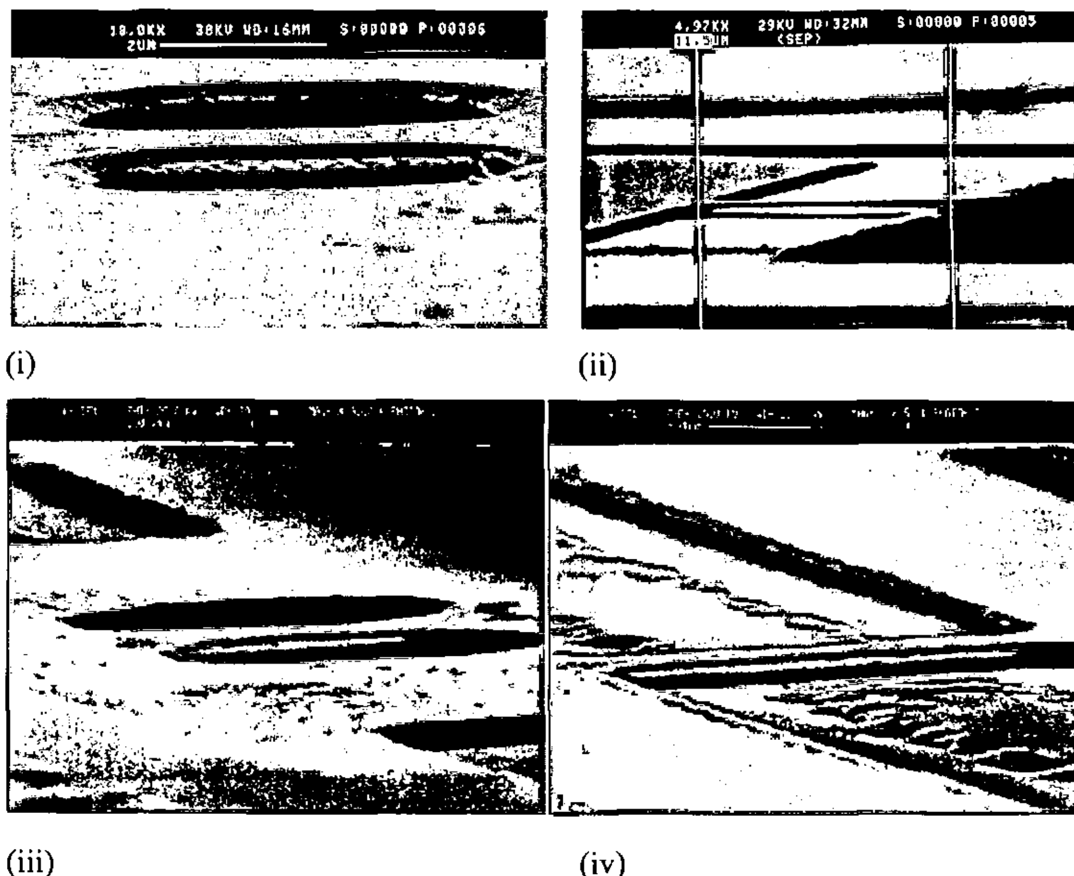
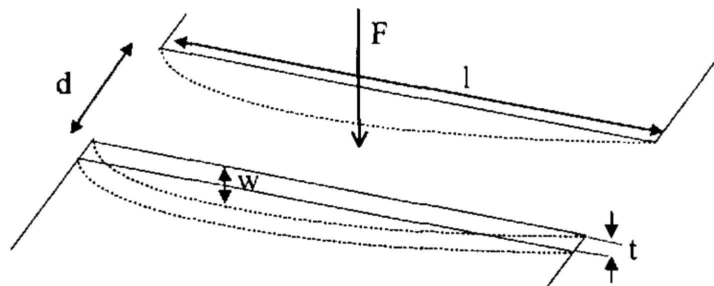


Figure 6.3 SEM micrographs of monocrystalline microbridges fabricated from SIMOX during this work

The micrographs in figure 6.3 (i)-(iv) show a range of bridges of various lengths and widths, they are well defined and clearly completely released from the substrate. In each case the separation is 0.4 μm, resulting from removal of the buried oxide layer by underetching. They appear generally free from bowing or buckling. The fabricated bridges ranged from 3 to 12 μm in length and 1 to 5 μm in width, the thickness of each bridge was 0.2 μm. In contrast with many 'microbridges' which have been reported [10] the dimensions of the devices shown in figure 6.3 are significantly smaller and represent true microstructures, together with the all the benefits of single crystal silicon.

In the following sections some applications of microbridges will be considered and the likely performance of a 'typical' SIMOX microbridge fabricated from monocrystalline silicon is estimated. The dimensions of this typical bridge are length = 6 μm, width = 1 μm and thickness = 0.2 μm. However, as the micrographs in figure 6.3 show, bridges with twice the length of the 'typical' example used here were readily fabricated by the method developed in this work. Figure 6.4 shows a diagrammatic representation of a microbridge under deflection by a force, F.



where

l = length, d = width, t = thickness and w = deflection

Figure 6.4 Diagrammatic representation of a typical SIMOX microbridge

Microbridges are commonly used in the resonance mode in sensing applications. In this case changes in a property to be measured are transformed into changes in stress, mass or form of the vibrating microbridge element, which in turn changes its resonant frequency. The resonant frequency of a microbridge under conditions of no applied load is described by equation 6.6 [9].

$$f_0 = 0.6104 \frac{t}{l^2} \sqrt{\frac{E\left(1-\upsilon^2\right)}{\rho}} \qquad (6.6)$$

where

f_0 = resonant frequency
l = beam length
t = beam thickness
E = Youngs modulus
ρ = density of beam material
υ = Poissons ratio

It can be seen from equation 6.6 that the resonant frequency will be increased by increasing the microbridge thickness or with greater effect by decreasing the microbridge length. The application of equation 6.6 to the typical SIMOX microbridge yields a resonant frequency of 65.5 MHz. This compares well to reported devices, for example a resonant frequency of 2.5 MHz was measured for a much larger 100 x 5 x 0.43 μm bridge made of silicon nitride on monocrystalline silicon which has been used in a mechanical light modulator [11]. However, all silicon SIMOX device would be expected to display a higher Q factor and better temperature stability than this multilayer example. The Q factor is a critical parameter for resonator sensors, this is dependent on the resonance/amplitude characteristics and a high Q factor results in a sensor which displays high resolution, accuracy and long term stability. The SIMOX microbridges fabricated in this work would be expected to display high performance due to the intrinsically high Q factor of the single crystal silicon material. The high mechanical quality of single crystal silicon enables stable, high resolution sensors to be realised with high sensitivity to the measureand. A specific application of a resonant bridge microsensor is for the measurement of force [12]. An externally applied axial force results in changes in the stress at the ends of the vibrating silicon bridge. This alters the resonant frequency of vibration which can be detected to give a measurement of the applied force.

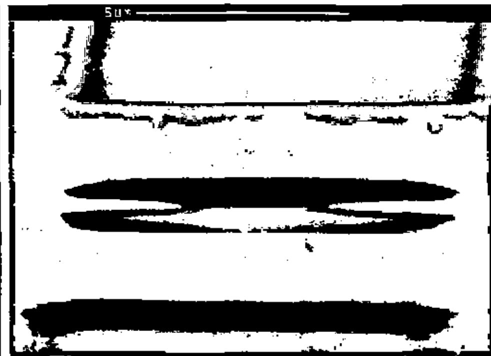
An alternative method of operation for a microbridge in a sensing application is to use the thermal properties of the microbridge. Here the benefits of the bridge structure are thermal isolation from the substrate due to the suspended nature of the structure and

small thermal mass resulting in fast response times. Depending on the application and operating environment of such a structure, the mechanical quality of the bridge, for example its residual stress may also become important. An example of a thermal application for a bridge structure is a radiation thermocouple in which a hot junction 'wire' is free standing above the substrate [13]. Absorbed radiation heats the wire, while the much larger cold junction in contact with the substrate remains at ambient. This type of device can be used as a single element in a detector array.

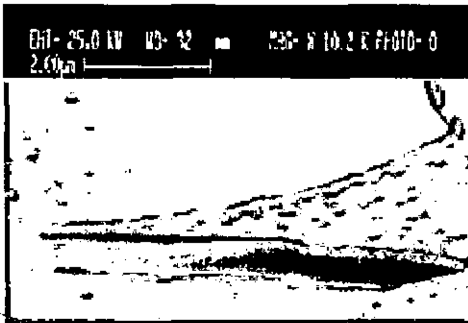
6.3 LATERAL FIELD EMISSION TIPS

Conical shaped lateral facing tips, which could have a use as lateral field emitters have also been realised from SIMOX in the current studies. Such devices are commonly employed for use in field emission diodes. There is much interest in the development of field emitters due to their insensitivity to conditions of high temperature and radiation. Lateral field emitters have several benefits over vertical designs in terms of high speed and high frequency operation [14]. The principle of operation of the emitters is that they are so sharp that a local field is generated which is sufficiently strong to induce quantum mechanical tunnelling between the electrodes. The turn on voltage is the applied voltage at which current begins to flow. The critical parameters for the fabrication of lateral field emitters are precise control of the inter-electrode spacing, sharpness of the tips and long term stability. The use of single crystal silicon for the tips is expected to improve the long term stability of devices over those reported in alternative materials [14]. Likely applications for field emitters are in flat panel displays [14] and tactile sensing [15]. An alternative area of application is vacuum microelectronic devices [16]. This is currently a very active research field and transistors fabricated in this way offer higher voltage and higher frequency operation compared with solid state devices. A variety of different shaped emitter tips were fabricated from SIMOX using the underetch technique and some of these are presented in figure 6.5 (i)-(v).

(i)



(ii) (iii)



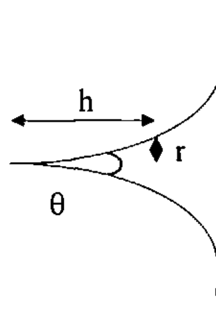
(iv) (v)

Figure 6.5 A selection of field emitter tips realised from SIMOX

These SEM micrographs show a high degree of miniaturisation and sharpness in the fabricated tips, in some cases (as shown in figures 6.5 (i) and (v)), in three dimensions. This is expected to facilitate the generation of a sufficiently strong local field to achieve emission and the tips are sharper than alternative, reported emitters

[14]. The tips can clearly be seen as suspended above the substrate. The smallest tip in figure 6.5 (i) is just 2 μm in length with other tip lengths ranging up to ~7 μm. In the case of this smallest tip, a slight upward curl can be seen at the free end. This is thought to be due to residual stress, which may be reduced by annealing after release.

To the author's knowledge the only other structures similar to the lateral, single crystal silicon, atomically sharp tips fabricated here, are those reported by Park *et. al.* [14] in 1997. Although this report claimed to be the first example of this type of device, they appeared after the SIMOX tips described here were reported. A quantitative comparison of the two structures is difficult in the absence of actual field emission data. However a qualitative estimate of performance can be made by comparison of the relative sharpness of the SIMOX tips fabricated here, with those reported by Park *et. al.* [14]. The tips have been represented in figure 6.6 as a cone with the sharpness defined in terms of the angle θ of the cone.



where
h = height of cone, r = radius of cone and θ = angle of cone

Figure 6.6 Conical model of a lateral field emitting tip

For the sharp tips fabricated by Park, the conical angle at the top of the point has been calculated from the relationship between h and r given in equation 6.7. The values for h and r were interpreted from the published micrographs in reference [14] to give a calculated angle (which is an indication of tip sharpness) of ~ 48.45°.

$$\tan\frac{\theta}{2}=\frac{r}{h} \qquad (6.7)$$

The same calculation has been applied to the tip fabricated in the current study and shown in figure 6.6 (i), for this structure, the cone angle was calculated as 17.06°.

Park's analysis of IV plots gained from sharp and blunt tips indicated that their sharper tip achieves a turn on voltage as low as 22 V but the operating voltage is 38 V, while the blunt tip measures 25 V and 35 V for these parameters respectively. In this case the operating voltage is defined as that required to achieve an output of 6 $\mu Atip^{-1}$. Since the SIMOX tips fabricated here appear considerably sharper in both x and y, by considering Park's results this would lead us to expect that these devices have a decreased emitting area. By considering the relationship given in equation 6.8 [14], this would relate to a squared increase in the field enhancement factor, resulting in a lower turn on voltage and therefore reduced device power consumption.

$$A \propto \frac{1}{\beta^2} \qquad (6.8)$$

where

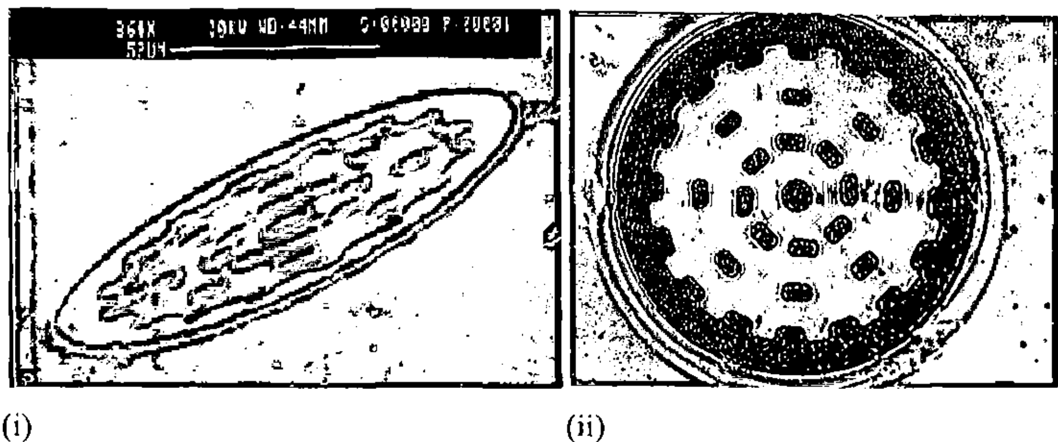
A = emitting area
β = enhancement factor

Since the tips described by Park are stated as turning on and operating at the lowest voltages reported, compared to other devices, the SIMOX tips, which are sharper but otherwise alike could be expected to lower these turn on and operating voltages still further.

6.4 GEARS AND MICROMOTORS

A gear wheel is a fully released mechanical structure with an exact design determined by its specific application. Gears wheels are an important microstructure since they are not limited to one application area. For example they can be used to sense, to allow sensed signals to actuate or as part of a more complex system to form a microrobot to perform specific tasks. An example is the use of microgear wheels in the cleaning of blood arteries. Gear trains, cranks and manipulators have all been

successfully fabricated [17]. Possibly the most common use of gear wheels is their incorporation into micromotors to operate as the rotor, the following sections will concentrate on this application. Micromotors are actuators capable of unrestrained motion in at least one degree of freedom [17]. Micromotors are being increasingly researched, resulting in improvements in both performance and lifetime of fabricated devices. However, small motive torque, high friction and mechanical coupling remain problematic, while repeatability and reliability are compromised by a lack of understanding of the failure mechanisms. Devices may be fabricated ready assembled or as discrete components for assembly. An ideal rotor will have smooth surfaces to reduce friction, low stress to reduce warpage and high fracture strain [17]. In these aspects a SIMOX design should excel, with wet etch definition resulting in smoother edges than the more usual dry etched designs and single crystal silicon providing low stress, avoiding the problems reported with polysilicon rotor warpage. Gear wheels were fabricated from SIMOX using the underetch technique, examples are shown in figure 6.7.



(i) (ii)

Figure 6.7 A monocrystalline silicon structure fabricated from SIMOX for application as a gear wheel or rotor

The monocrystalline silicon gear wheels are intended for full release and not suspension, however, to allow micrographs to be taken of the devices *in situ*, the structures shown above are approximately 90% released. Despite the high degree of release there are no signs of warpage resulting from residual stress. The wheels fabricated from SIMOX vary in design but are typically of the order of 90 μm in diameter.

For micromotors, electrical actuation has shown benefits over magnetic, scaling to microstructures better and requiring only IC compatible materials. Piezoelectric ultrasonic motors [18] benefit from high torque to speed ratios, eradication of friction and warpage problems and are suited to conductive fluid environments. In electric motors, the attractive and repulsive forces transfer charge distributions to the electrodes to achieve motion. The mobile electrode is the rotor and the stationary, the stator. Variable capacitance is the main mode of operation, here motors store electrical energy in the variable stator-rotor gap and the change in capacitance in the direction of motion is proportional to the output torque of the motor. In micromotor operation optimum torque is desirable. For this reason rotary designs have dominated due to a higher force to torque leverage compared with linear styles. Side drive motors have proved preferable to top drive, due to rotor instability and planarisation problems with the later [19].

Commonly reported motors are therefore electric, variable capacitive, rotary side drive devices which are either salient pole or harmonic (wobble) motors. These configurations are shown in figure 6.8. Typical parameters reported for such devices are [17]:

• motive torque	10 pNm
• operating voltage	25-100 V
• air gap	1-3 μm
• electric field intensities (across gap)	10^8 Vm^{-1}
• lifetime	millions of cycles
• operating speed	700-15000 rpm

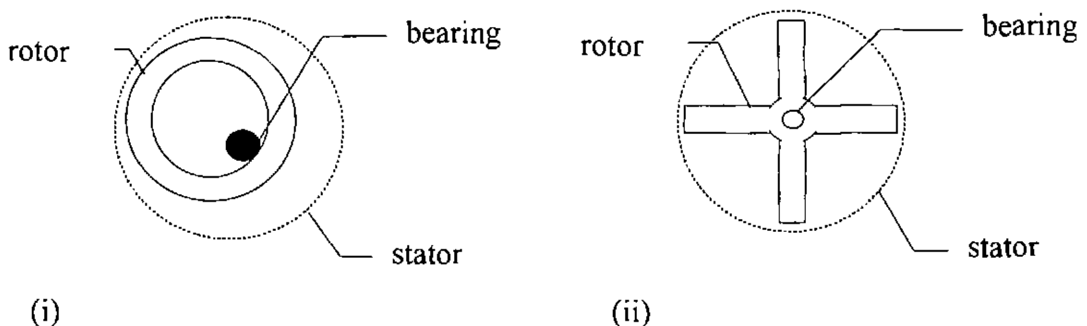


Figure 6.8 (i) wobble and (ii) salient pole motor designs

For operation, the salient pole motor relies on tangential electrostatic forces, excitation is applied to the stator with opposite poles of the same phase excited with equal voltages of opposite polarities. Wobble motors are operated by normal electric fields attracting the grounded rotor to the excited stator pole, the speed of operation is proportional to the electric signal frequency with a proportionality constant of the gear ratio. For comparable designs, wobble motors provide greater motive torque than salient pole designs. All motors currently suffer from friction due to the rotor weight and electrostatic attraction with static friction demonstrated to be larger than dynamic. Wear also limits the motor lifetime due to both wear of components and the build up of wear generated particles. The operation is significantly affected by the rotor release process and operating environment.

Having discussed the operation of micromotors it can be seen that for optimum operation devices should be physically small to result in low moments of inertia which develop low internal stresses during operation [19]. Low temperature sensitivity is also a prerequisite. This indicates that an all silicon design with the low intrinsic stress of single crystal structure without the presence of multilayers will be appropriate for this application. In addition the underetch technology described in this thesis allows the fabrication of gear wheels or rotors of much smaller dimensions then many of those reported in the literature which range from ~125 - 8000 μm. This type of micromotor has many applications, for example microsurgery and sensing application such as blood flow measurement [20]. In this case the field from the microscopic magnet rotor will, as it rotates, modulate the resistivity of a permalloy. The resistivity gives an electrical signal frequency proportional to the rotation rate and therefore blood velocity.

6.5 RESONATORS

Resonator structures have a vast application field and are one of the most common structures utilised in microsensors. These devices have an element which vibrates at resonance which changes frequency as a result of a physical or chemical change. The sensitivity can potentially be much larger than in other methods of detection, for example a resonant sensor examining the change in stress of a suspended element can be 100 times more sensitive than a piezoresistive device [8]. A resonator must be

designed to have sufficient input parameter sensitivity and selectivity to allow measurement. The critical factors for resonator operation are material, fabrication technique, vibrational mode, Q factor and temperature sensitivity. As discussed earlier in this chapter, the Q factor is related to the shape of the resonance peak in the frequency/amplitude graph which describes resonant behaviour. A high Q factor is desirable to simplify the control electronics, minimise the effect of drive electronics, and implies low, unwanted coupling with the external environment. With a high Q, resonator performance can be made almost entirely dependent on the mechanical properties of the element, making the correct material selection paramount in device design.

Although bridges, cantilevers and diaphragms are the most commonly used resonant structures (as discussed in the relevant sections) more complex structures can be used to improve performance. Applications of this type of resonators are in high performance pressure and acceleration sensors [8, 21].

Sensor performance can be increased by several orders of magnitude by designing a device which:

(i) enhances non fundamental modes of vibration and avoids interference from unwanted modes.

(ii) has balanced vibrational modes, for example by using two plates vibrating in antiphase.

(iii) allows effective internal fluid transport along the resonator surface.

(iv) facilitates fluid movement between the two sides of the vibrating element, for example by the incorporation of holes to reduce damping.

Several resonators have been reported in the literature with complex structures to enhance or modify performance. To demonstrate the utility of SIMOX for the formation of such structures a number of the more complex designs were incorporated in the mask used during this work. Some examples of fully suspended resonator structures fabricated from SIMOX are shown in figure 6.9.

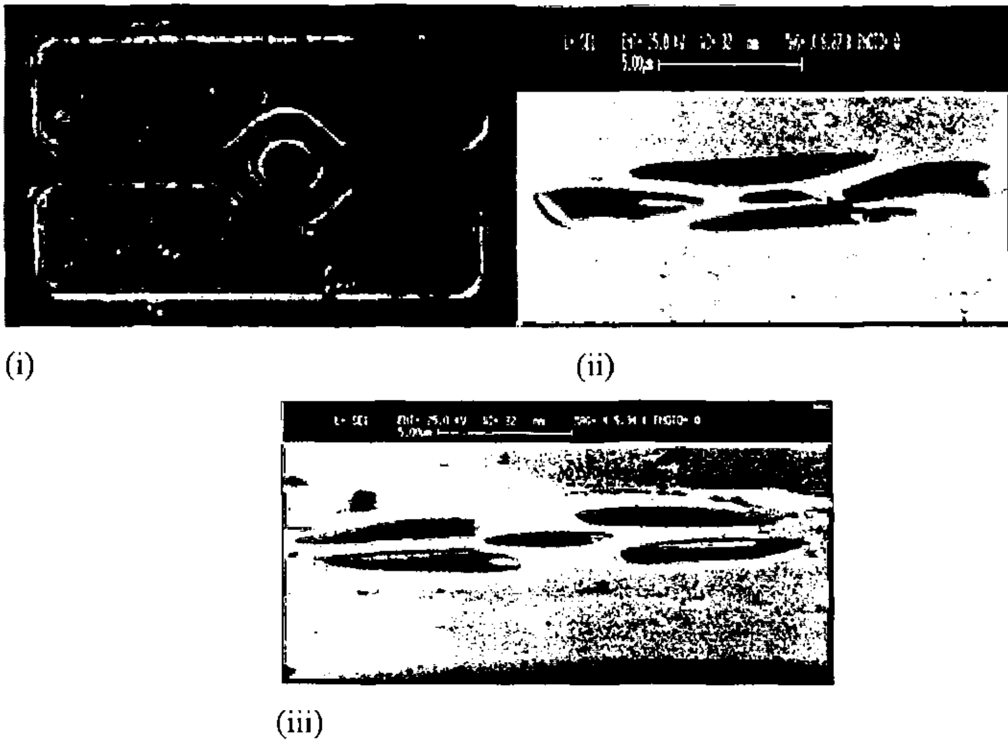


Figure 6.9 Optical and Scanning electron micrographs of various resonator structures fabricated in this work

The well defined resonators in figure 6.9 can clearly be seen as suspended above the substrate with no sign of bowing. The designs shown include features to encourage non fundamental, balanced modes of vibration while providing holes through the resonator to reduce air damping. The incorporation of these holes combines well with the SIMOX fabrication technique allowing access to the buried oxide layer at several locations and therefore reducing the underetch time required to fabricate the device. The largest contribution to the temperature sensitivity of resonators, typically several $\%°C^{-1}$, comes from thermal expansion coefficient mismatch. To reduce this effect, multilayers should be avoided and the resonator, supports and mount made from the same material. For the SIMOX devices fabricated in this work, as shown in figure 6.9, the resonator, supports and mount would all be single crystal silicon. Calculations have shown that in this case the temperature dependence of the resonant frequency would be determined only by the temperature dependence of the elastic constants, typically as low as 10 $ppm°C^{-1}$, reducing cross sensitivity [8].

The materials commonly used for resonant sensors are silicon and quartz. The outstanding mechanical properties of single crystal silicon make it the most suitable, it

resonates with a high Q factor, can be micromachined and is low in defect and dislocation densities. Polysilicon has a lower Q factor and can suffer from stress resulting from deposition, while quartz cannot be micromachined by standard techniques. However, where single crystal silicon doping is used to achieve etch selectivity, internal losses are caused by impurities and dislocations, typically reducing the Q factor from 10^6 to 10^4. These losses can be neglected when undoped single crystal silicon is the resonator material as in the case of a device fabricated from SIMOX. An example of a resonant pressure sensor has been reported consisting of two single crystal silicon plates, adjacent to each other and vibrating in antiphase [21], this has produced a Q factor of 20000. However, in order to etch this device by traditional methods heavy P+ doping was used to achieve etch selectivity, if fabricated using the underetching of SIMOX developed in this thesis, P+ doping would be unnecessary and a higher Q factor and therefore improved performance would be expected.

6.6 QUANTUM WIRES

Very thin wires which are suspended above the substrate have been reported in the literature [22]. These can be used to study quantum and phonon transport effects at low temperature and as microfuses. These structures have been widely researched but problems with fabricating such thin suspended structures have been encountered. If the wires can be made with a diameter less than the Fermi wavelength or dominant phonon wavelength then the energy states for the electrons and phonons respectively will display one dimensional quantisation, devices which are 0.6 μm in width have been reported for this purpose. In the case of SIMOX wires this would simply require a change to the mask dimensions. Quantum effects necessitate that the wires must minimise scattering and be free standing to provide isolation from the substrate. Currently the main application of quantum wires is for research into these effects themselves, however, a sensitivity to light and heat has been observed [19], this could be utilised for specific sensing applications.

Thin wire structures were fabricated from SIMOX in this work, a typical device is shown in figure 6.10.

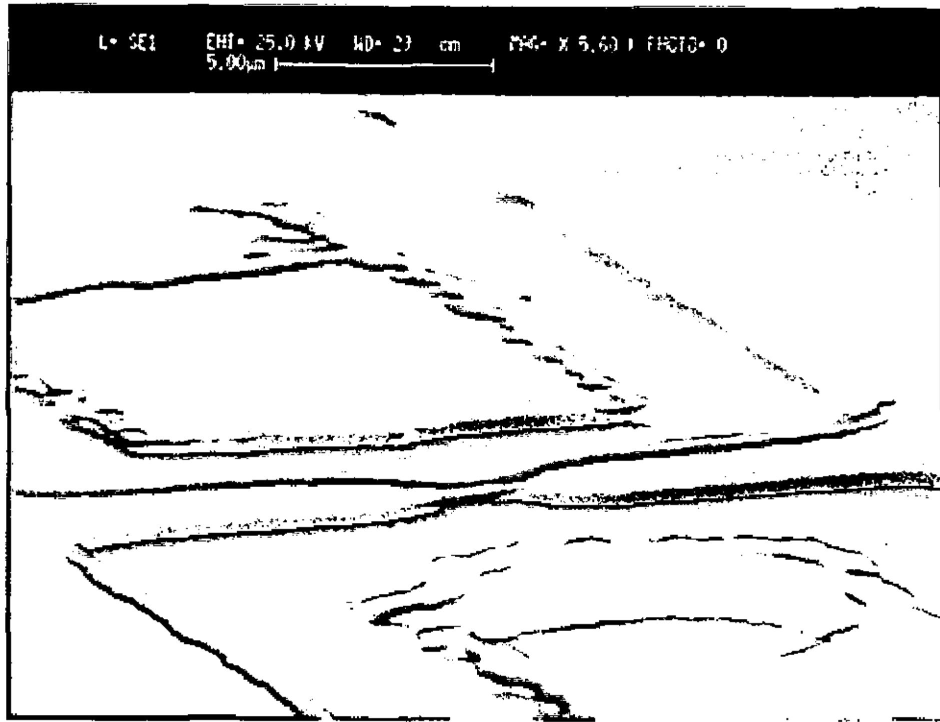


Figure 6.10 A micrograph of a fine single crystal silicon wire fabricated in this work

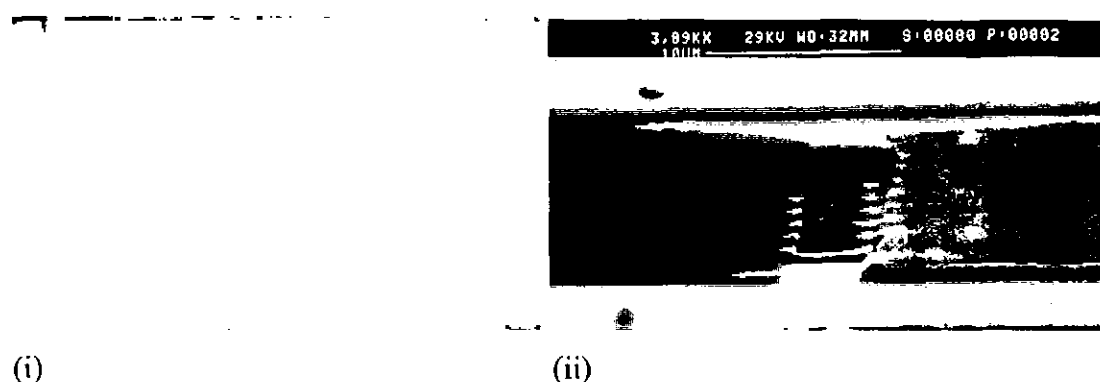
The structure fabricated from SIMOX shown in 6.10, has approximate dimensions of 2 x 0.2 x 0.2 µm. The wire can be seen as clearly suspended above the substrate and self supporting. Similar wires have been shown to withstand a current density in the region of 10^6 Am^{-2} [19]. The single crystal silicon material used for the device shown in figure 6.10 would be expected to show improved performance due to reduced scattering compared with equivalent devices which have been fabricated from polysilicon [22].

6.7 'BRIDGE OF HOLES'

This structure combines a one dimensional photonic crystal with a two dimensional waveguide through which light can travel by total internal reflection [23]. The design is a microbridge through which regularly spaced holes have been made. This design is expected to display reduced losses particularly around corners compared with conventional waveguides. Such a structure could be used to form the connections in optoelectronic circuitry with low losses. The benefits of optoelectronic circuits over

electronic ones are lower power and no resistance or heat generation problems at reduced dimensions, this could result in a faster information processing [23]. If one of the regular holes in the bridge were omitted to introduce an irregularity, light of a particular frequency could be confined. Such a structure could be implemented in lasers, photonic switches or waveguides [23].

Several 'bridge of holes' type structures were fabricated from SIMOX, a plan and side view are shown in figure 6.11.



(i) (ii)

Figure 6.11 Micrographs of a 'bridge of holes' fabricated in this work.

In figure 6.11 (i), the white area shows the area of undercut, figure 6.11 (ii) confirms the full release of these areas. The 'holes' and bridging sections can be clearly seen. The bridge dimensions are approximately 40 μm long by 4 μm wide, similar to reported structure dimensions [23].

If the holes are at a spacing comparable to the wavelength of light, ~0.5 μm, cavities with 100 % confinement efficiency are expected. By using different cavity designs, devices with tuneable frequency confinement could be achieved. These type of structures could be readily achieved in single crystal silicon as demonstrated by figure 6.11 which would offer improvements both optically and mechanically over the reported polysilicon design. The additional benefit is that the novel method of fabrication from SIMOX, developed in this thesis facilitates fabrication with only half the number of masking steps of the reported process [23], resulting in a reduction in fabrication complexity, time and cost.

6.8 SUMMARY

In the preceding sections a brief overview of several microstructures fundamental to microsystems has been given. In each case an example of such a structure made during this work using the novel SIMOX technology has been presented. Several of the microstructures have been modelled using simple calculations. These have demonstrated high theoretical performance resulting from features such as the monocrystalline material and small, controlled thicknesses characteristic of the SIMOX material. An illustration of the advantages of each device over reported designs has typically been given. It should be noted that the designs and in particular the processing times were not optimised for each microstructure and it is expected that further improvements could be achieved. Changes in lateral dimensions can be easily implemented by mask changes, while vertical dimensions can be varied by the use of different SIMOX material specifications. These two factors could be used to change the performance parameters of the structures to make them applicable to a different operational range.

The primary benefits of the novel technology developed in this work, to a range of 'building block' microstructures, are the excellent mechanical properties of single crystal silicon - virtually no hysteresis or creep, the ease of fabrication - reduced number of mask steps, combined with one sided processing and temperature stability due to the all silicon design. This should result in improved performance and reduced fabrication costs. These benefits are similar to those apparent from the in depth study of the pressure sensor presented in chapters 3, 4 and 5. The illustration of the applicability of this work to a number of fundamental micrstructures adds to its significance.

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CHAPTER 7: CONCLUSION

7.1 PROJECT CONCLUSION
7.2 FURTHER WORK
7.3 REFERENCES

7.1 PROJECT CONCLUSION

The principle aim of this project was to design, fabricate and evaluate a novel capacitive pressure sensor. This was to be achieved using a combination of advanced, application specific micromachining techniques combined with SOI substrates. The importance of developing a technology by which cavities can be formed routinely lies in the extensive use of this structure in microsensors and microstructures based on suspended mass. To demonstrate this, some alternative microstructures have been fabricated as examples, to demonstrate the versatility and importance of this approach.

The incentives which drive this work come from a combination of the huge sensors market and the potential of the novel device developed in this work to provide improvements in performance over existing devices. Indeed there are reports [1] of inadequacies in the field of sensing, such as a continuing need for very small, accurate and highly sensitive pressure sensors for medical applications. The SIMOX pressure sensor is intended to address these needs. The anticipated benefits of the SOI device result from the use of monocrystalline silicon as the mechanical element material and the small, controlled plate thickness and separation, combined with the advantages of an array, such as high output and redundancy tolerance. There are in addition, several fabrication related benefits such as single-sided processing, resulting in shorter etch times and smaller, stronger chips and also the avoidance of bonding or implantation for etch stops which allows a dopant free diaphragm to be realised.

A review of current research, materials and technologies was initially conducted; this directed the work towards the use of SIMOX material due to its high mechanical quality, maturity and availability. Lithography techniques, a variety of wet and dry etchants and metallisation schemes, were experimentally evaluated. This allowed the identification of the most suitable procedure for each step of the process of SIMOX pressure sensor fabrication. The silicon etchant selected was a potassium permanganate solution with a composition of 0.6 g $KMnO_4$, 280 ml H_2O and 20 ml 50 %HF. Controlled underetching of the buried silicon dioxide was carried out with an buffered HF solution comprising 60 ml HF, 420 ml NH_4F. A series of low surface tension rinses was then introduced to overcome the effects of stiction and thus increase yield. Aluminium metallisation was then added to provide an electrical interface for measurement. Photoresist plugging was used to achieve a sealed diaphragm which would deflect under applied pressure.

Theoretical modelling of the sensor structure was carried out to determine the design of the device. Calculations indicated that the application of pressure would not result in diaphragm breakage. Temperature dependence resulting from air trapped in the cavity was shown to be insignificant within the expected temperature range of application. Also, calculations indicated that electrostatic effects resulting from the application of voltage would not affect performance at the voltages typically used for measurement. An interesting point arising from the analysis was that, for the dimensions used, the restriction of this technology to the fabrication of a circular diaphragm offers several benefits, compared to square diaphragms. These include a similar sensitivity and decreased levels of stress resulting in a higher rupture pressure.

Having established a viable sensor design, together with a well controlled high yield fabrication sequence, which included overcoming a number of problems specific to this structure, a range of pressure sensing diaphragm arrays was manufactured. To the author's knowledge, the devices developed here represent the first reported pressure sensors made from SIMOX and the first SIMOX microstructures to utilize the benefit of monocrystalline silicon for the manufacture of the mechanical element. These sensors were then evaluated for performance under conditions of applied pressure and temperature. It should be noted that the work presented here could be regarded as a first iteration of the design and the performance of the devices would inevitably be improved with further development. Furthermore, a degree of automation of the

process would be required for commercialisation of the sensor and this would in turn increase the fabrication repeatability for the device. The sensor was found to have a high sensitivity of 0.0027 pF/mmHg, non-linearity of 0.016 %FS, repeatability of 0.01 %FSO, and a hysteresis within the margins of measurement error. This compares well with the predicted performance based on the calculations and the material properties. Many of these performance parameters exceed those reported in the literature for similar devices; the sensitivity in particular is the highest yet reported.

In addition to the pressure sensor, a number of alternative microstructures have been fabricated using the same process sequence as the pressure sensor. These have been illustrated with the inclusion of several micrographs and a discussion of each structure to highlight the performance benefits offered by this novel SIMOX process.

In summary the aims have been achieved by the design, fabrication and evaluation of a capacitive, diaphragm array, pressure sensor from SIMOX material. It has been demonstrated that this can be fabricated with high yield and provides high performance in many respects, reflecting in particular the high mechanical quality of the monocrystalline diaphragm. The performance suggests that this sensor is suitable, with some further development, for use in medical applications where no appropriate device currently exists. The topics covered in this project have also created several opportunities for further work.

7.2 FURTHER WORK

This project has successfully achieved its aims, in so doing, it has raised several recommendations for further work. The sensors requires further evaluation in terms of failure analysis. This would determine the reliability and lifetime expectancy of the sensor. Packaging, suitable for the sensor application, also requires evaluation and development.

Within the bounds defined by the modelling and the limits of the underetching procedure, the sensor dimensions could be easily adjusted to extend the application of the sensor to alternative fields of pressure sensing which require different pressure ranges. Additions could be made to the current structure to increase performance, for

example a reference cavity could be included to allow 'normalization' and on chip electronics could be developed to enhance the measurement techniques.

The exploitation of this technology for the fabrication of the basic components of alternative structures has been touched on in this work and has demonstrated high potential. These possibilities could be pursued further by the fabrication and evaluation of complete devices for many other sensing and actuating applications.

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PRESENTATIONS AND PUBLICATIONS:

The following is a list of presentations and publications which have been made in connection with the work described in this thesis. A copy of each publication is included.

PRESENTATIONS:

Liverpool, UK	Anisotropy and Etching of Semiconductors
Boston, USA	International symposium on microelectronics
Budapest, Hungary	Multichip modules and sensor technologies
Bremen, Germany	Workshop on micromachining
London, UK	Solid state sensors -technology and applications

PUBLICATIONS:

'A capacitive pressure sensor fabricated by a combination of SIMOX (SOI) substrates and novel etching techniques'
Journal on Communications, volume XLVII, 6-8, May 1996.

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A CAPACITIVE PRESSURE SENSOR FABRICATED BY A COMBINATION OF SIMOX (SOI) SUBSTRATES AND NOVEL ETCHING TECHNIQUES

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Silicon technology has been employed for several years for the manufacture of pressure sensors for the vast world-wide market. However many popular designs suffer from process induced stresses. The structure described in this paper, has been designed from silicon on insulator (SOI) material. In addition to avoiding these traditional problems, circuitry can be readily incorporated due to the use of standard processing steps. The monocrystalline silicon diaphragm is expected to display improved performance over more common materials used for the sensing element. The fabrication process begins with the opening of a window in the top silicon by wet or dry etching. Through this opening, with the surrounding silicon acting as a mask, buffered hydrogen fluoride is used to isotropically etch the buried silicon dioxide to form a cavity. When a pressure is applied to the device, the diaphragm deflects, detected by an increase in the capacitance between the diaphragm and substrate. By avoiding back etching, chip size and etch time are reduced while mechanical strength is increased. The pressure sensor is designed to measure in the range 0–250 mmHg and to achieve this many single diaphragms are interconnected in a matrix arrangement. This novel fabrication technique can be applied to the manufacture of many microstructures for other sensing and actuating applications.

1. INTRODUCTION

Many pressure sensors exist with various measurement ranges and applications. Silicon technology has been successful in the precision and low cost (low accuracy) sectors of the market. The total pressure sensor sales in Western Europe are predicted to be 35.7 million units by 1977 [1]. There has been a recent trend towards capacitive devices [2], away from piezoresistive designs for several reasons including their inherent difficulties with long term stability, low pressure measurements, temperature drift and low yield [3]. Common methods for fabrication of capacitive pressure sensors include boron doping, silicon direct wafer bonding or bonding to pyrex substrates. The high boron doping acts as an etch stop but can result in high stress which is problematic for suspended structures. Silicon wafer bonding can cause diaphragm warping, require high temperature and the resulting films can have unbounded areas and trapped bubbles [7]. Pyrex bonding can lead to a mismatch in thermal expansion coefficients between diaphragm and substrate at high and low temperatures resulting in stress [6]. The undoped structure designed here does not suffer from these process induced stresses and allows the incorporation of circuitry in the structures [4], [5].

The design described below avoids these processing problems and incorporates a monocrystalline silicon diaphragm which has improved performance over polysilicon, silicon nitride and other material layers common in sensing elements. Further design benefits are provided by the SIMOX material producing a thin diaphragm and small cavity depth — both well controlled; resulting in high stability and reproducibility and the provision of natural etch stops without necessitating implantation for high doping levels or electrochemical control.

The fabrication procedure is simple, using few masking steps and front side only processing. This increases the mechanical strength of the chip and reduces the size and process time over back, or front and back etched designs. The metal contacts and bonding pads can be formed using aluminium deposition. A window is then dry etched through the top silicon layer and using the same photoresist mask this is then underetched to form a diaphragm suspended above a cavity. This is achieved by the removal of a section of the buried silicon dioxide in buffered hydrogen fluoride, using etch time to control the diaphragm diameter and ultimately pressure measurement range.

The production of this performance pressure sensor demonstrates the feasibility of SIMOX technology. The significance is increased by the applicability of this technology to the fabrication of other microstructures for sensing and actuating applications.

2. FABRICATION AND DISCUSSION

The simple process sequence from the initial SIMOX wafer is shown in Fig. 1. A small window is etched through the top silicon layer to expose the buried oxide, using a photoresist mask. For this, a silicon etchant with a slow etch rate and with silicon:silicon dioxide selectivity was required. Both wet and dry (RIE) etching procedures have been investigated for this step and currently a potassium permanganate based wet etch has been implemented.

The buried oxide is then etched from below the silicon to form a cavity. A number of possible etchants were investigated and an appropriate solution and etching procedure was determined and characterized for the controlled lateral etching of silicon dioxide. The important criteria being a high etch rate and high selectivity over silicon to minimize effects on the silicon top layer. There is a linear relationship between etch time and underetch distance, which

is independent of the size of the etch window within the experimental range used.

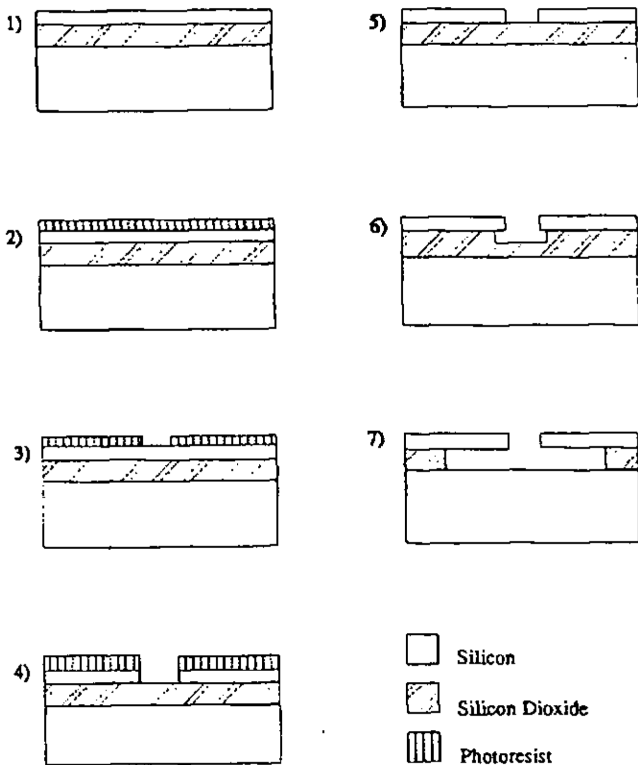
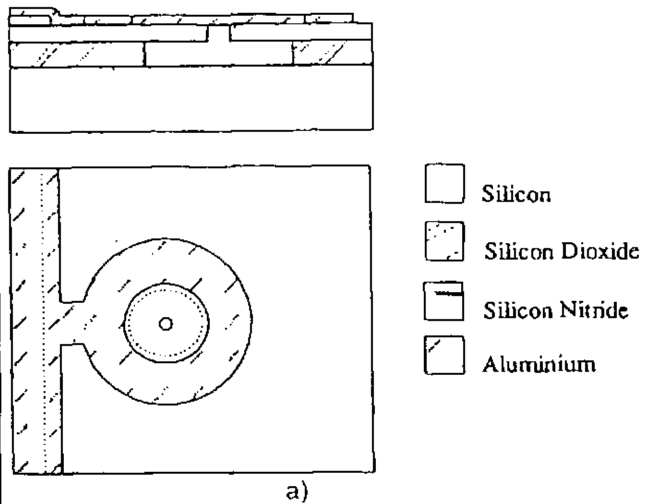


Fig. 1. The fabrication procedure

The challenge of retaining metallization through a long hydrogen fluoride etch, was addressed and overcome either by using a thick metallization layer which could be retained unprotected through etching or by application of the metal as a final step, subsequent to diaphragm formation and protection. In either case the metal layer is deposited by magnetron sputtering and defined by photolithography and etching. It is then sintered to form interconnects and contact pads.

The access window and therefore, diaphragm are circular, this increases sensitivity and eliminates cracking from stress concentration at sharp corners of the access windows, a problem which was initially experienced. A series of low surface tension rinses was developed to reduce the likelihood of stiction, another common cause of diaphragm collapse and therefore device failure, often seen in early fabrications [8]. Stiction is common in microstructure fabrication. It is an effect thought to be caused by a combination of van der Waals and other forces which pull the suspended element into contact with the substrate where it becomes stuck, ultimately resulting in device failure. This occurs as the rinse water, trapped under or inside a structure dries following etching. Finite element modelling has been used to confirm the feasibility of this structure and aid its design. Results indicate that the maximum diaphragm stress occurs around the central etch window but is well below the fracture stress for silicon.

A single diaphragm device was then successfully fabricated using the optimized fabrication routine described above (Fig. 2). To increase the device output with respect to parasitic capacitances, an interconnected matrix of these single diaphragms has now been designed and fabricated. The matrix comprising of 2500 single sensing membranes has an expected full scale capacitance change of 10 pF. It is believed that single device failure will be relatively insignificant (Fig. 3).



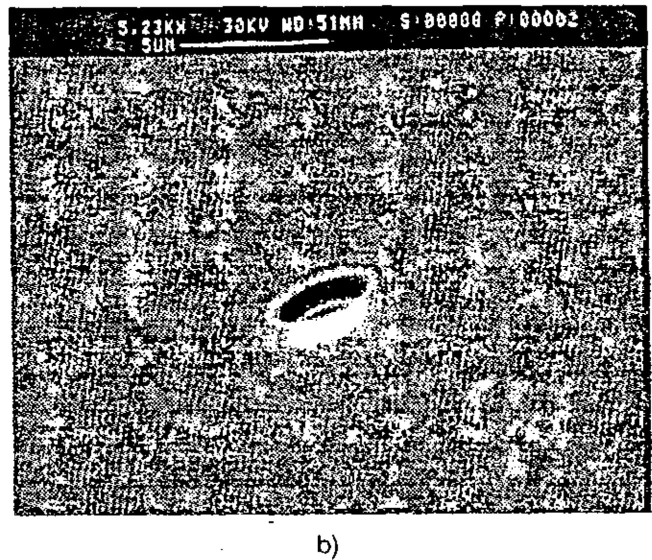


Fig. 2. The single diaphragm design
a) Device design with interconnection; b) SEM image of a device

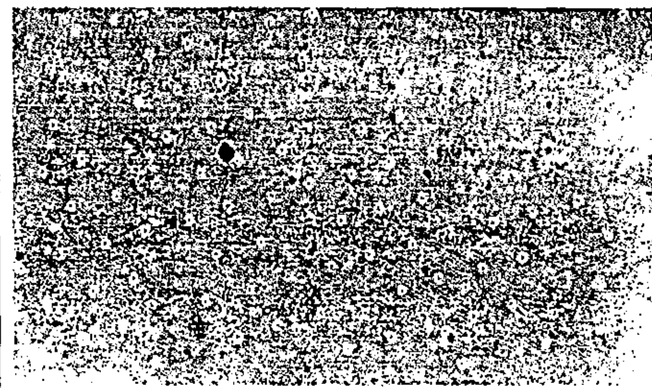


Fig. 3. A matrix of devices

Simple 'functionality' tests were then carried out using a nitrogen stream directed at the diaphragm. A small change in capacitance could be detected, coinciding in time with the application of flow and not present in the absence of nitrogen flow or with virgin SIMOX sample (unetched). This has been attributed to the deflection of the diaphragms by the pressure of the nitrogen stream. More quantitative testing will follow.

3. CONCLUSION

Diaphragm arrays have been fabricated with a high yield (98 % in 2500 membranes successfully manufactured). This demonstrates that it is plausible, using conventional processing steps in conjunction with SIMOX substrates, to fabricate capacitive pressure sensors which are expected to show operational advantages over traditional devices. These benefits include high sensitivity and ease of processing. Furthermore this method of fabrication can also be applied to the formation of various other sensing structures and capacitive devices. To demonstrate this several examples of alternative structures have been fabricated including bridges, cantilevers, resonators and gear wheels.

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Alison Medler graduated from DeMontfort University in 1990 with 2(i)Hons, from a sandwich degree in Physics/Chemistry. This included a project fabricating silicon sensors. Following a period of world travel, she begun work at Middlesex University Microelectronics Centre (MUMEC), England, developing microminiature, advanced performance sensors from silicon-on-insulator. This Ph.D. work is now entering its third year.

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J. Butcher is Dean of the Faculty of Technology at Middlesex University, London. He graduated in Physics and Electrical Engineering from Cambridge University in 1960 and subsequently completed a Ph.D. in Solid State Physics at London University. In 1968 he founded the Microelectronics Research Centre at Enfield College (now Middlesex University) and was its Head until 1993 when he took up his present post. Professor Butcher has held numerous consultancies, including nine years with the GEC Hirst Research Centre working in the field of semiconductor device physics and technology. He is a Fellow of the Institution of Electrical Engineers and a Fellow of the Institute of Physics. He has published over 60 papers on microelectronics technology and engineering education, and has given invited papers at numerous conferences worldwide.

Research Into Novel Sensors on Silicon Substrates

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Abstract

A number of sensor types are being researched at Middlesex University Microelectronics Centre (MUMEC):
- a prototype silicon anemometer has the diffused resistors operating at 110°C, as the sensor elements implemented in CMOS technology, which enables efficient implementation of high performance analogue electronics suitable for sensor interfaces in a low cost standard IC fabrication process.
- a prototype capacitive Si-insulator-Si, based on implanted silicon substrates, allow selective etching with controlled etch-stops to create well defined and stable micro machined structures for precision pressure sensors.
- silicon is again the substrate on which 1μm thin-film gold fine-line patterns have been constructed for interconnection of the subsequent deposition of a pattern of twelve polypyrrole sensors (by another organisation).
The examples of research into sensor technologies demonstrate the continuing opportunities afforded by adapting silicon substrate technologies. Sensors built into silicon substrates can take advantage of the ability to create passive sensitive elements in the silicon and also of the opportunity to integrate them with measurement and control circuits in order to achieve automatic control and create "Smart" sensors.

1. Introduction

A number of sensor types are being researched at Middlesex University Microelectronics Centre (MUMEC):
(a) an integrated silicon anemometer intended to replace the more expensive hot wire anemometer to improve the accuracy of medical diagnosis of patients suffering from obstructory pulmonary diseases;
(b) a micro machined pressure sensor in silicon-on-insulator substrates for medical applications requiring miniature, robust and reliable structures
(c) microstructures on silicon substrates as a base for arrayed polypyrrole aroma sensors.

Each of these devices makes use of the capabilities of the researchers at MUMEC to create designs and constructions of miniature devices on silicon and, subsequently, to exploit the opportunity to integrate the sensor elements with control and signal processing circuits using VLSI design technology.

2. Principles of the intended sensors

2. (a) Anemometer for peak flow measurement

Anenometers measure wind speed or velocity. Single wire Hot Wire Anemometers (HWAs) are used to measure a point velocity. Typical industrial HWAs have a frequency response of many hundred kilohertz and are useful for measuring localised turbulent flow. Conventional HWAs are usually constructed in a Wheatstone Bridge configuration. Typically, a tungsten wire mounted on the tip of a probe forms one element of a bridge and a second, variable, element is used to set the operating point[1]. In constant current mode, the bridge supply current is maintained and an imbalance voltage is developed under flow conditions, which can be converted to a flow value from a calibration curve. The response is slow because of the delay in establishing a potential difference across the bridge for a given signal change. The alternative, constant temperature operation uses a feedback controller to maintain the sensor at a constant temperature. During flow and resultant cooling, the controller increases the current to re-balance the bridge. The increased current is the measure of the flow. This method gives a faster response than constant current.

HWA Wheatstone Bridge configurations can be implemented in silicon[2] (Figure 1). Integrated with the sensor and bridge is a comparator which compares the temperature dependent feedback from the measurement bridge with a reference voltage. The error signal so obtained, is power amplified and drives the heater bridge which heats the measurement bridge. Flow then results in constant average resistance in the measurement bridge. The response is fast, but a larger part of the heater current flows in the cooler side, so decreasing the temperature gradient and consequently the sensitivity. The alternative, constant heating mode, described earlier, gives a higher

output signal, but which is now a function of the power supply.

The number of sensing elements in the bridge governs the maximum signal level possible. For maximum sensitivity in the Wheatstone Bridge:

$$Z_1=Z_2 \text{ and } Z_3=Z_4 \quad (1)$$

If $Z(1+\delta)$ denotes the change in bridge element resistance, then the potential developed across the bridge is

$$V_{AB} = V_1.\delta/(2+\delta) = V_1.\delta/2 \quad (2)$$

The highest signal output is obtained by having two elements as sensors. The manner in which the sense elements are interconnected can also improve the output. If all resistors have a high positive temperature coefficient and the bridge elements are cross connected as in Figure 2b, then the two sensing elements are effectively on the same side of the bridge as in Figure 2c. Now the signal is the sum of ΔZ_2 and ΔZ_4 and not the difference. This principle is embodied in the research prototypes described in Section 3.

2. (b) Micro-machined capacitor pressure sensor

The intention of this sensor research is to develop a sensing element by creating microstructures in silicon. The micro-structure is to be created by researching and developing a novel etching system, appropriate to the fabrication of diaphragms, micro-bridges and cantilevers from silicon-on-insulator (SOI) starting material. The sensing element itself is mono-crystalline silicon, giving mechanical properties and sensitivity improvements over traditional structures, resulting in a device combining high performance with low cost. The potential of this technique is being demonstrated by creating a miniature capacitive pressure sensor. The pressure sensor is intended for biomedical applications where devices must be small, accurate and highly sensitive. The required pressure range to be measured with this device is 66-330 millibar.

A capacitive pressure sensor is potentially more accurate than other devices such as piezo-resistive sensors (which use the change in strain to indicate the applied pressure). These suffer high temperature drift, and the diaphragm thickness may not be below about 1 micron because of the junction depth required for the diffused resistors. This limits the lower pressure range of such sensors.

In constructing the diaphragm of the present sensor using SOI starting material, a special benefit is the single crystal silicon top layer. This is ideally suited for the realisation of well defined ultra thin diaphragms above a cavity formed within the silicon dioxide layer, all on a silicon substrate. Most current devices use a diaphragm composed of either polycrystalline silicon or silicon dioxide. However, when grown, the oxide tends to form in layers. When the structure is then employed as a mechanical component, the layers shift over one another, so distorting the strain in the silicon, resulting in non-calibrated outputs. For capacitive and vibration sensors, the consequence can be sudden changes in the apparent zero position, which is a most difficult error to compensate. Mono-crystalline silicon has greater mechanical strength, which is not degraded with repeated stress, and its mechanical and thermal properties are not dependent on the process. Also, there is no mismatch of thermal expansion coefficients between diaphragm and substrate materials, which can cause defects due to strain.

Deflection of the diaphragm under applied pressure (Figure 3), causes capacitance changes between this top capacitive plate and the substrate, i.e. the bottom capacitive plate. An additional benefit of this structure is that the small, controlled plate separation can be utilised such that the cavity floor acts as a stop when over-pressures are applied. Devices employing this feature can withstand over-pressures of up to 5000 psi [3]. Furthermore, this plate contact could actually be exploited as the sensory feature for certain device types, e.g. switches. An array of identical structures can be constructed [4] and the capacitance variations can be converted to voltage shifts, amplified and signal processed to produce a map of local pressure variation. It is important to minimise parasitic capacitances in both the sensing element and interfacing circuitry as the changes in device capacitance with applied pressure will be extremely small.

2. (c) Microstructures for "Soiffer" sensors

Silicon is again the base substrate on which 1μm thin-film gold fine-line patterns have been constructed for interconnection of the subsequent deposition of a pattern of twelve polypyrrole sensors (by another organisation). The composition of each of the polypyrroles is tuned to absorb different combinations of ingredients of an aroma. The conductivity changes in each of the 12 elements is different and produces a unique "fingerprint" response for each aroma.

The substrates are made by standard silicon processing techniques, having the advantages of a mature technology and the opportunity for mass production of the sensing units. The structure is relatively simple and the fabrication process has a small number of masking stages and therefore gives a high yield, which is important because an array of sensors are incorporated together to produce one sensing head.

3. Realisation of preliminary sensor structures

3. (a) Monolithic integrated intelligent flow sensors

Integration of the readout and signal processing electronics achieves a compact module designed in the same suite and fabricated in the same process as the sensor elements. Using an operational amplifier as the basic building block, the sensor current or voltage can be amplified and the signal filtered and linearised. As the circuits operate hot, about 110°C, the circuit and technology must be relatively temperature insensitive. This

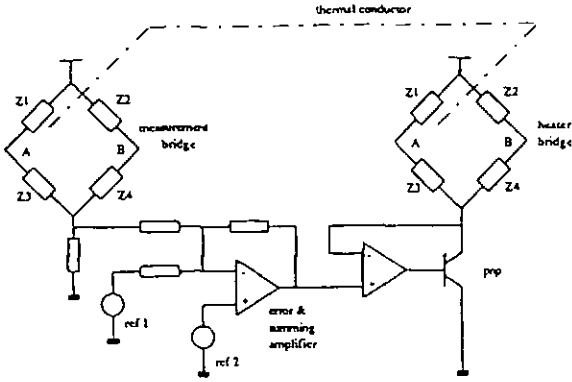


Figure 1. Anemometer Wheatstone Bridge Configuration

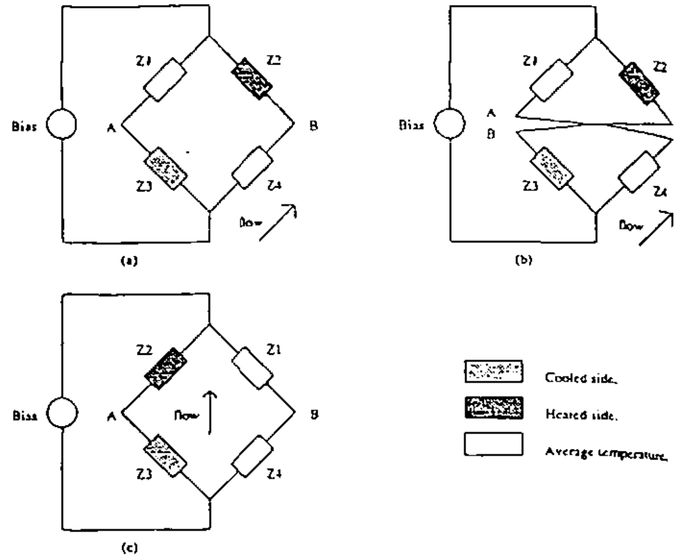


Figure 2. Alternative Positioning of Sensing Resistors
a). On Opposite Arms of Wheatsone Bridge
b) Cross-connected to be on
c) Adjacent Arms of the Wheatstone Bridge

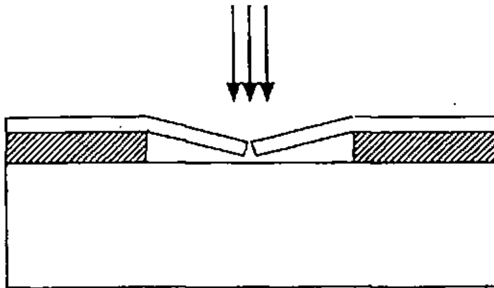


Figure 3. Schematic of Deflection of Diaphragm Over Micromachined Cavity

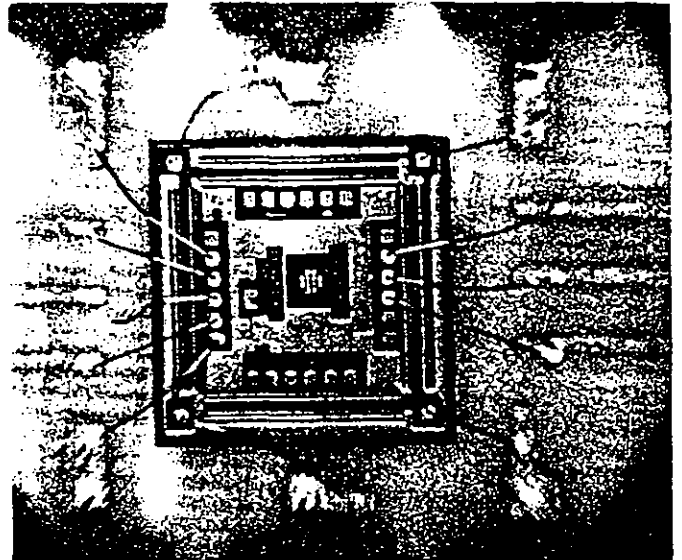


Figure 4. Prototype Monolithic Silicon Anemometer with Sensing and Heating Wheatsone Bridges Assembled on Ceramic Substrate With Thick Film Interconnections

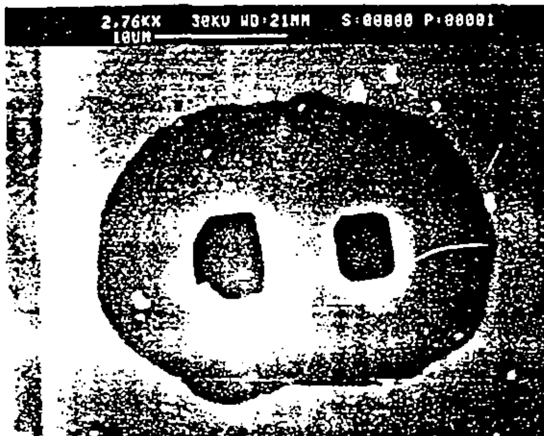


Figure 5. Scanning Electron Micrograph Showing Diaprhragm Over Micromachined Cavity

is achieved in CMOS operational amplifiers by biasing the gain stages at their zero temperature coefficient (ZTC) points. Biasing the current sources for each stage at their respective gate-source voltages in the saturation region is a simple way to achieve this [5].

Two different sensor designs configured according to Figures 2a and 2b have been fabricated. Thus the sensors are in opposite arms of the bridge(Figure 2a) or on the same side of the bridge (Figure 2b). An inner bridge makes up the heater and uses resistors with aspect ratios identical to those in the measurement bridge. The sensor elements are 41 ohm n-well diffused resistors with a sheet resistance of 2000 ohms per square. The temperature coefficient of the resistors is given by

$$R_T = R_0\{(1+\alpha(T_1-T_0)\} \qquad (3)$$

where R_0 is the resistance at reference temperature T_0, R_T is the resistance at an elevated temperature T_1, and α is the temperature coefficient of the material.

Electromigration of the metalisation is avoided by using wide metalisations. The opportunity has been taken also to use the central part of the chip to include some test structures to experiment with the eventual "smart" design. These include operational amplifiers with and without a bias chain, different bias circuits, active and passive components for temperature coefficient measurements and an automatic ZTC bias generator cell. Because of the unconventional use of the chip periphery to fabricate a sensor, a second ring of bonding pads has been laid out between the sensor and test circuits.

The sensor chips have been mounted on 14 pin ceramic dual-in-line substrates in order to provide external electrical connections and place the sensors into a flow stream. Each die has been raised 50-100 microns above the substrate surface by using a printed thick-film dielectric on top of which the die has been glued with a non-conductive epoxy adhesive at each corner. The die size of 10 mm^2 had less than 1 mm^2 in thermal contact with the substrate. Thick-film gold tracks provided wire bonding pads on the substrate. The assembly is shown on Figure 4. For flow measurements, the substrates were mounted on a printed circuit board at the end of a stainless steel tube.

3. (b) Micro-machined diaphragm

The use of a composite, monolithic, silicon-insulator-silicon material allows fabrication using only one side of the wafer. This avoids complexities of front-to-back mask alignment, the large chip size and processing time required for etching from the back. One sided wafer processing also results in a wafer of increased mechanical strength.

The layering of the SOI material provides natural etchstops, avoiding the need for: a) doping - which results in large lattice strains in the membrane owing to the high dopant concentrations required; and b) electrochemically controlled etching which requires either a long diffusion time or the epitaxial growth of a thick polysilicon layer. Additionally, accurate control of the diaphragm thickness leads to a high sensitivity in the final device, good pressure range control with freedom from hysteresis and creep. The vertical dimensions of the SIMOX (silicon on ion-implanted oxide) starting material, which determines the diaphragm thickness and plate separation, is another constraint. The basic parameters for design are diaphragm length, thickness and plate separation. The optimum structure size for high sensitivity and miniaturisation has been determined by calculation. Currently, the diaphragm dimensions being used are approximately 20 microns for the diaphragm diameter and 3 microns for the access window.

Processing steps

The cavity is created by lateral etching of the silicon dioxide through a small opening in the top silicon layer, over which the thin silicon then remains suspended as a fine membrane diaphragm. In order to open up the etch window in the top silicon, all other areas must first be masked. For dry etching, positive photoresist is the mask material. The window is etched with a suitable gas which is anisotropic and ceases to etch at the oxide boundary. The next stage is to etch the cavity by removing the silicon dioxide below the top silicon layer through this window using an isotropic etchant, which selectively etches silicon dioxide and not silicon. The diameter of the diaphragm is controlled by controlling the time of etching. The resulting structure is a flexible diaphragm above a cavity (Figure 5).

3. (c) Microstructures for "Sniffer" Sensors

The silicon wafers, which take no active part in their operation. This allows standard three inch diameter silicon wafers to be used and keeps down the material and processing costs.

A stable insulating base is provided by oxidising the silicon wafers in a steam ambient at 1050°C. Thus a sufficiently thick oxide layer may be grown in a reasonable time scale.

Silicon nitride passivation is used to avoid silicon particle impairment of wafer sawing. Photolithography of the passivation is used to define the active areas and the bonding pads.

Photomask fabrication is done with care because the small features are difficult to achieve over the entire area of the photomask. Photolithography is done with positive resist and contact alignment. Wafers are conditioned in an oven prior to surface silylation. The initial photolithograpy defines the contact metalisation layer which is provided by a thin layer of gold with a standard refractory metal adhesion layer. The integrity and definition of the structure the metal layer is processed using a standard lift-off technique. This overcomes the problem of etch control when etching gold patterns in a mixture of potassium iodide and iodine where the etch rate can be difficult to control.

Metals are deposited by electron beam evaporation to minimise the deposition of metal on the side wall of the features. This helps to reduce the generation of filaments which produce potential shorts when the metal is lifted off.

4. Experimental results

4. (a) Monolithic integrated intelligent flow sensors

The resistances of the sensor and the heater are the same at 41.6 ohms. The high sheet resistance of the well resistors gives rise to the necessary positive temperature coefficient, as shown in the calibration measurement (Figure 6). The equivalent resistance of the bridge is approximately doubled at 140°C.

Air flow measurements have been carried out by relative measurement, at room temperature ambient, using a calibrated hot film anemometer mounted the same distance into the test chamber as the sensor under test. With the gain of the constant temperature controller set at 150 000, the transient response time of the heater is 3 ms, with no overshoot. The resultant heater current variation with flow, and controlled constant sensor current are illustrated in Figures 7 and 8.

The control circuit uses a fully differential current to voltage converter to maintain the null deflection of the measurement bridge whilst allowing a good common mode rejection ratio. Both chip designs have been measured using both constant heater current and constant temperature modes. With the gain set at 560 V/A, the zero offset voltage for both sensors is 2 mV. The differential output voltages from the current-to-voltage converter for chip 1 for air flow in the range 3 to 15 m.sec^{-1} are plotted in Figure 9. Operation with constant heater current gives a higher signal output than with constant temperature. The observations confirm that the sensor output at constant heater current increases with temperature, and that negative feedback (i.e. lower temperature differential) reduces the signal in constant temperature mode. The results obtained with chip 2 showed a tenfold increase as a result of the layout according to Figure 2b. While significant power is consumed in these early devices, it was because of the use of an unmodified mixed-mode CMOS process. Power can be traded against cost by design and process adjustments, for instance by thinning the back of the silicon. Future designs will make use of available BiCMOS technology.

4. (b) Micro-machined diaphragm

A reliable and repeatable wet etching system has been established by undertaking a survey of several different etchants, comparing the etched features and determining the etch rate, undercut rate and profile. The etchant composition has been optimised and characterised. A glass plate mask prepared with several variations on the design enables comparison of results. The effects of reducing the window size and the minimum size limit for successful etching have been determined. The lateral etch rate is substantially slower than the vertical rate, due to diffusion limitation and problems of transporting reaction product away from, and reactants to, the site.

Single cell devices fabricated in this way demonstrate the feasibility of the fabrication method in SIMOX substrates. But, practical problems which reduce device yield are: (i) the corners of the square diaphragms and access windows caused points of weakness due to stress concentrations; and (ii) stiction between diaphragm. The solutions are:

- Circular etch holes leading to circular diaphragms giving an expected reduction in the cracking. To achieve this the diaphragm diameter must be greater than the side length of the square diaphragm initially tested. Currently a diaphragm diameter of 20 mm is being used.
- Reactive ion etching instead of wet etching to eliminate stiction [6,7].

In order to operate the device in capacitive mode and to characterise the structure, the task of overlayer doping and then metalising to form ohmic contacts is in hand, using an alloying furnace. Devising a suitable means of mechanically testing the structures is also proving challenging due to their very small dimensions.

4. (c) Microstructures for "Sniffer" Sensors

A number of runs have been undertaken to ensure that the process sequence allows device fabrication by standard processes and will ultimately provide working devices. Optimisation of the performance parameters of the device may require a further development of the manufacturing process and the potential exists for further development of the manufacturing materials so that the effectiveness of other semiconductor materials can be assessed.

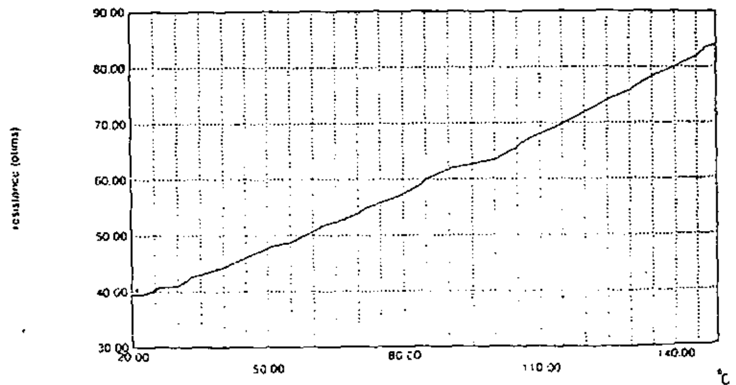


Figure 6. Calibration of Sensing Resistors in Silicon

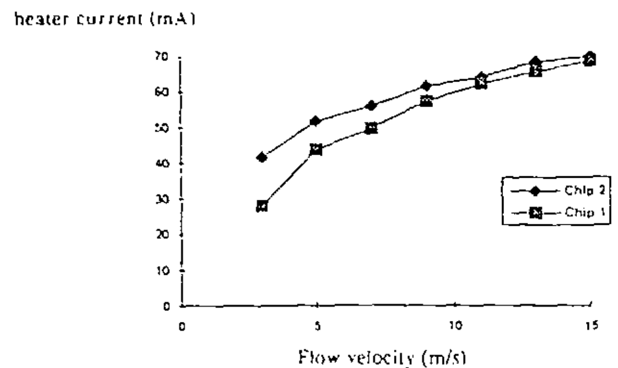


Figure 7. Heater Currents of Anemometer With Constant Temperature Control.

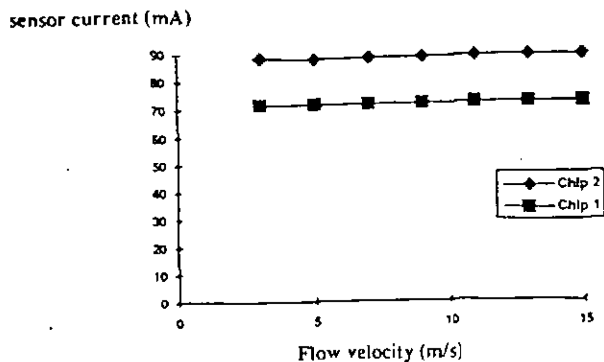
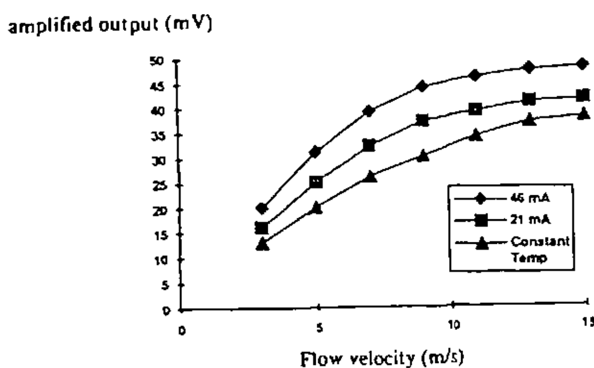
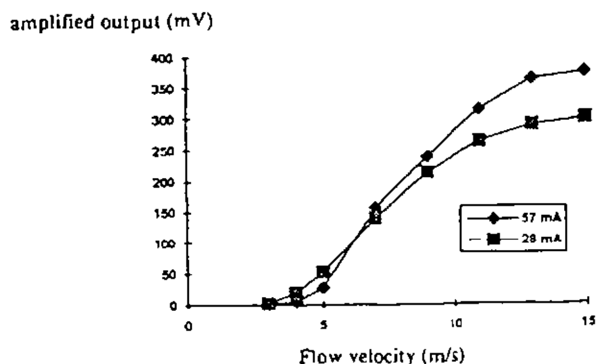


Figure 8. Heater Currents of Anemometer With Constant Current Control



igure 9a. Differential Output Voltages of Chip 1 - onnected With Sensing Resistors on Opposite Arms of he Wheatstone Bridge - With Constant Current and Constant Temperature Operation.



ure 9b. Differential Output Voltages of Chip 2 - nnected With Sensing Resistors on Adjacent Arms of Wheatstone Bridge - With Constant Current and nstant Temperature Operation.

5. Outlook and Conclusions

5. (a) Monolithic integrated intelligent flow sensors

The ability to design and fabricate viable integrated Wheatstone bridge flow sensors has been demonstrated. The cross-connected configuration clearly achieves significantly higher output. Power dissipation and response speed can be decreased by thinning the substrates and alternative layouts and technologies. Temperature effects on the operational amplifiers may be avoided by biasing them close to their ZTC bias point.

5. (b) Micro-machined diaphragm

The project has so far demonstrated that it is possible to fabricate suspended mass microstructures using the combination of SIMOX material and undercutting. A wet etching method has been characterised and used to fabricate these although the yield was low. As a result Reactive Ion Etching is being investigated as an alternative and should allow greater control and smaller device geometry's to be realised.

This is a novel fabrication technique which will enable the benefits of mono-crystalline silicon to be fully utilised resulting in high performance sensors for various parameter measurement.

Valuable experience has already been gained into both the practical and theoretical aspects of microstructures and SOI based fabrication.

5. (c) Microstructures for "Sniffer" Sensors

The design for a sensor that is sensitive to molecules in the vapour phase has been enabled by fabrication techniques compatible with standard semiconductor process techniques up to the point at which the polypyrrole sensor layers are applied.

These examples of research into sensor technologies demonstrate the continuing opportunities afforded by adapting silicon technologies.

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